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High Temperature Masked ROM MCUs

Z86C08 MCU

Advance Product Specification

PS030701-0413

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Revision History

Each instance in the following revision history table reflects a change to this document from its previous version. For more details, refer to the corresponding pages or appropriate links provided in the table.

Date	Revision Level	Description	Page Number
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Table of Contents

Revision History iii
List of Figures vi
List of Tables vii
Architectural Overview 1
Z86C08 High Temperature MCU Features 1
Block Diagram 3
Pin Description 5
Electrical Characteristics 8
Absolute Maximum Ratings 8
Standard Test Conditions 9
Capacitance 9
DC Electrical Characteristics 10
AC Electrical Timing Characteristics 14
Standard Mode at High Temperature 15
Low Noise Mode at High Temperature 16
Low-EMI Emission Mode 17
Pin Functions 18
Functional Description 23
RESET 23
Power-On Reset (POR) 23
Watch-Dog Timer Reset 24
Program Memory 25
Register File 26
Stack Pointer 28
General-Purpose Registers (GPR) 28
Counter/Timer 28
Interrupts 29
Clock 31
Halt Mode 33
Stop Mode 33
Watch-Dog Timer (WDT) 34
Op Code WDT (5Fh) 35
Op Code WDH (4Fh) 35

Permanent WDT 35
Auto Reset Voltage (VLV) 35
Mask ROM Option Bit Description 37
Control Registers 38
Timer/Counter Registers 39
Port Registers 42
Interrupt Registers 43
General Control Registers 46
Ordering Information 49
Part Number Description 49
Precharacterization Product 50
Application Precautions 50
Customer Support 51

List of Figures

Figure 1. Z86C08 High Temperature Masked ROM MCU Block Diagram 3
Figure 2. 18-Pin DIP/SOIC Configuration, Standard Mode 5
Figure 3. 20-Pin SSOP Pin Configuration, Standard Mode 6
Figure 4. Test Load Diagram 9
Figure 5. AC Electrical Timing 14
Figure 6. Port 0 Configuration 19
Figure 7. Port 2 Configuration 20
Figure 8. Port 3 Configuration 21
Figure 9. Internal Reset Configuration 23
Figure 10. Program Memory Map 25
Figure 11. Register File 26
Figure 12. Register Pointer 27
Figure 13. Counter/Timers Block Diagram 29
Figure 14. Interrupt Block Diagram 30
Figure 15. Oscillator Configuration 32
Figure 16. Typical Auto Reset Voltage (VLV) vs. Temperature 36

List of Tables

Table 1. Z86C08 High Temperature MCU Features 1
Table 2. Power Connections 2
Table 3. 18-Pin DIP/SOIC Pin Identification, Standard Mode 5
Table 4. 20-Pin SSOP Pin Identification, Standard Mode 6
Table 5. Absolute Maximum Ratings 8
Table 6. Capacitance 9
Table 7. DC Characteristics, High Temperature Range 10
Table 8. AC Electrical Timing: Standard Mode at High Temperature 15
Table 9. AC Electrical Timing: Low Noise Mode at High Temperature 16
Table 10. Z8 Control Registers Reset Values* 24
Table 11. Interrupt Types, Sources, and Vectors 31
Table 12. Typical Frequency vs. RC Values: VCC = 5.0 V @ 25°C 32
Table 13. Typical Frequency vs. RC Values, VCC = 3.3 V @ 25°C 33
Table 14. R241 Timer Mode Register (TMR) 39
Table 15. Counter/Timer 1 Register (T1), R242 40
Table 16. Prescaler 1 Register (PRE1), R243; Write Only 40
Table 17. Counter/Timer 0 Register (T0), R244 41
Table 18. Prescaler 0 Register (PRE0), R245; Write Only 41
Table 19. Port 2 Mode Register (P2M), R246; Write Only 42
Table 20. Port 3 Mode Register (P3M), R247: Write Only 42
Table 21. Port 0 and 1 Mode Registers (P01M), R248; Write Only 43
Table 22. Interrupt Priority Register (IPR), R249; Write Only 43
Table 23. Interrupt Request Register (IRQ), R250; Read/Write 44
Table 24. Interrupt Mask Register (IMR), R251; Read/Write 45
Table 25. Flag Register (Flags), R252; Read/Write 46
Table 26. Register Pointer (RP), R253; Read/Write 47
Table 27. General Purpose Register (GPR), R254; Read/Write 47
Table 28. Stack Pointer Low (SPL), R255; Read/Write 48
Table 29. Z86C08 High Temperature MCU Ordering Information 49

Architectural Overview

Zilog's Z86C08 High Temperature Masked ROM MCU is suitable for applications that require a general-purpose MCU to operate at sustained elevated temperatures. Unlike Flash-based MCUs that are guaranteed to operate at 150°C for only 40 to 310 days, the High Temperature Z86C08 MCU can operate at a prolonged temperature of 150°C for many years without experiencing program memory data retention issues. Such applications can include under-the-hood automotive applications, aircraft propulsion systems, HVAC applications, high-power motor/generator systems, industrial, instrumentation, and distributed control applications (e.g., natural resources exploration & production), as well as military applications.

For applications demanding high temperature and powerful I/O capabilities over prolonged durations, the Z86C08 High Temperature MCU's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals or parallel I/O.

Two on-chip counter/timers, with a large number of user-selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Z86C08 High Temperature MCU Features

Table 1 presents the memory and frequency features of the Z86C08 High Temperature Masked ROM MCU.

Table 1. Z86C08 High Temperature MCU Features

Device	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z86C08	2.0	125	12

Note: *General-Purpose RAM.

The following list presents the general feature set of the Z86C08 High Temperature Masked ROM MCU.

- 14 Input/Output lines
- Six vectored, prioritized interrupts (3 falling edge, 1 rising edge, 2 timers)
- Two analog comparators
- Program options:

- Low Noise
- ROM Protect
- Auto Latch
- Watch-Dog Timer (WDT)
- RC Oscillator

- Two programmable 8-bit counter/timers, each with 6-bit programmable prescaler
- WDT/ Power-On Reset (POR)
- On-chip oscillator that accepts crystal, ceramic resonance, LC, RC, or external clock
- Low power consumption (50mW, typical)
- Fast Instruction Pointer (1µs @ 12MHz)
- RAM Bytes (125)

Note: All signals with an overline, "‾", are active Low, for example: B/$\overline{W}$ (WORD is active Low); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions, as noted in Table 2.

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Block Diagram

Table 1 shows a functional block diagram of the Z86C08 High Temperature Masked ROM MCU.

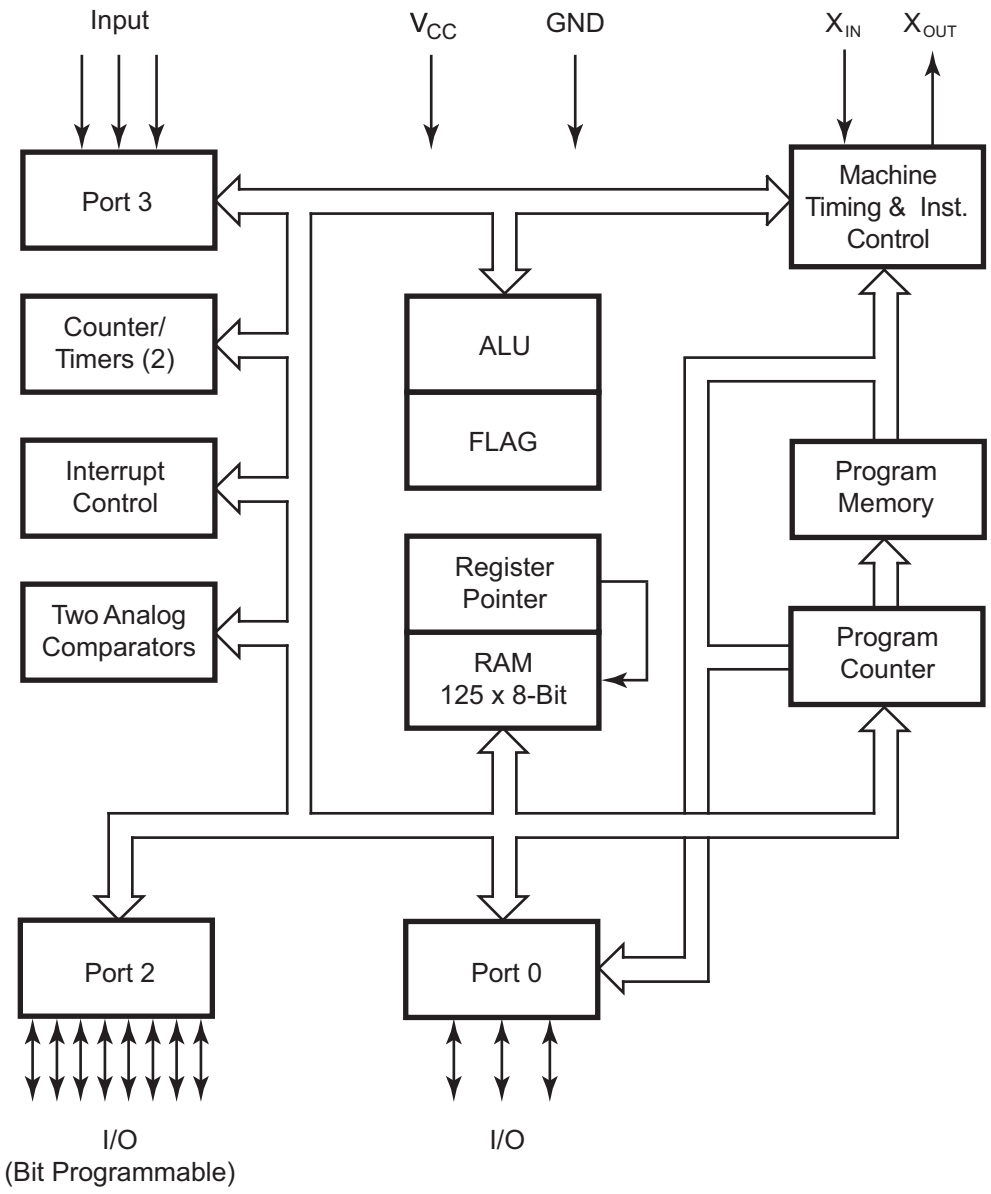


Figure 1. Z86C08 High Temperature Masked ROM MCU Block Diagram

Pin Description

A pin diagram of the 18-pin DIP and SOIC packages is shown in Figure 2, and their pins are identified in Table 3.

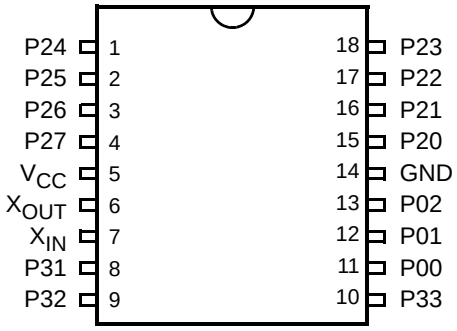


Figure 2. 18-Pin DIP/SOIC Configuration, Standard Mode

Table 3. 18-Pin DIP/SOIC Pin Identification, Standard Mode

Pin #	Symbol	Function	Direction
1	P24	Port 2, Pin 4	Input/Output
2	P25	Port 2, Pin 5	Input/Output
3	P26	Port 2, Pin 6	Input/Output
4	P27	Port 2, Pin 7	Input/Output
5	V_{CC}	Power Supply	
6	X_{OUT}	Crystal Oscillator Clock	Output
7	X_{IN}	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11	P00	Port 0, Pin 0	Input/Output
12	P01	Port 0, Pin 1	Input/Output
13	P02	Port 0, Pin 2	Input/Output
14	GND	Ground	
15	P20	Port 2, Pin 0	Input/Output
16	P21	Port 2, Pin 1	Input/Output

Table 3. 18-Pin DIP/SOIC Pin Identification, Standard Mode (Continued)

Pin #	Symbol	Function	Direction
17	P22	Port 2, Pin 2	Input/Output
18	P23	Port 2, Pin 3	Input/Output

A pin diagram of the 20-pin SSOP package is shown in Figure 3, and its pins are identified in Table 4.

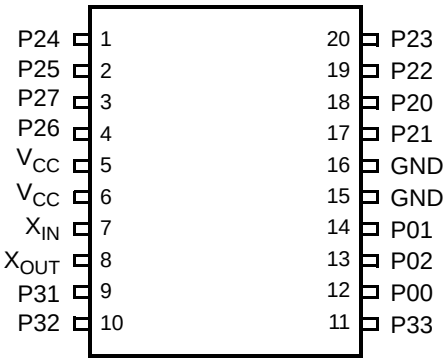


Figure 3. 20-Pin SSOP Pin Configuration, Standard Mode

Table 4. 20-Pin SSOP Pin Identification, Standard Mode

Pin #	Symbol	Function	Direction
1	P24	Port 2, Pin 4	Input/Output
2	P25	Port 2, Pin 5	Input/Output
3	P27	Port 2, Pin 7	Input/Output
4	P26	Port 2, Pin 6	Input/Output
5	V_{CC}	Power Supply	
6	V_{CC}	Power Supply	
7	X_{IN}	Crystal Oscillator Clock	Input
8	X_{OUT}	Crystal Oscillator Clock	Output
9	P31	Port 3, Pin 1, AN1	Input
10	P32	Port 3, Pin 2, AN2	Input
11	P33	Port 3, Pin 3, REF	Input
12	P00	Port 0, Pin 0	Input/Output
13	P02	Port 0, Pin 2	Input/Output
14	P01	Port 0, Pin 1	Input/Output

Table 4. 20-Pin SSOP Pin Identification, Standard Mode

Pin #	Symbol	Function	Direction
15	GND	Ground	
16	GND	Ground	
17	P21	Port 2, Pin 1	Input/Output
18	P20	Port 2, Pin 0	Input/Output
19	P22	Port 2, Pin 2	Input/Output
20	P23	Port 2, Pin 3	Input/Output

Electrical Characteristics

The data in this chapter is prequalification and precharacterization and is subject to change. Additional electrical characteristics can be found in the individual chapters.

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. See Table 5. Power dissipation is calculated as follows:

Total Power Dissipation = V_{CC} x [I_{CC} – (sum of I_{OH})] + sum of [(V_{CC}–V_{OH}) x I_{OH}] + sum of (V_{OL} x I_{OL})

Table 5. Absolute Maximum Ratings

Parameter	Min	Max	Units	Note
Ambient junction temperature under Bias (T_{JA})	–40	+150	C	
Storage temperature	–65	+150	C	
Voltage on any pin with respect to V_{SS}	–0.7	+12	V	1
Voltage on V_{DD} pin with respect to V_{SS}	–0.3	+7	V	
Voltage on X_{IN} pin with respect to V_{SS}	–0.3	V_{DD}+0.3	V	2
Total power dissipation		462	mW	
Maximum allowable current out of V_{SS}		84	mA	
Maximum allowable current into V_{DD}		84	mA	
Maximum allowable current into an input pin	–600	+600	µA	3
Maximum allowable current into an open-drain pin	–600	+600	µA	3.4
Maximum allowable output current sinked by any I/O pin		12	mA	
Maximum allowable output current sourced by any I/O pin		12	mA	
Total maximum output current sinked by Port 2		70	mA	
Total maximum output current sourced by Port 2		70	mA	

Notes:
1. Applies to all pins except where otherwise noted. Maximum current into or out of pin must be ±600µA.
2. There is no input protection diode from pin to V_{CC}.
3. Excludes pins 6 and 7.
4. Device pin is not at an output Low state.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin See Figure 4.

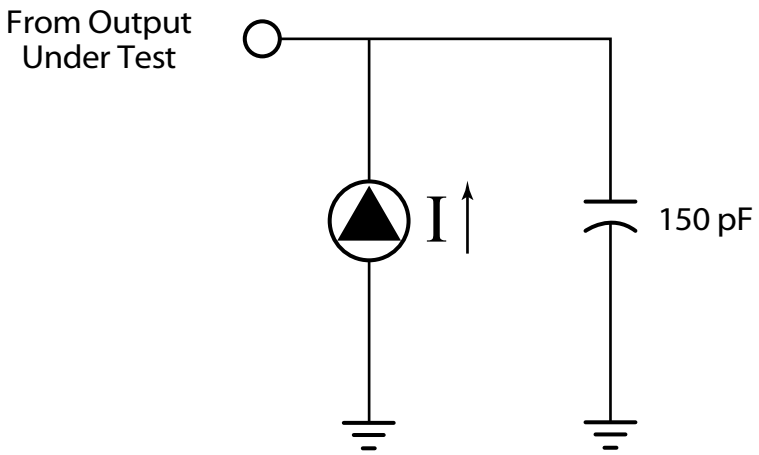


Figure 4. Test Load Diagram

Capacitance

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0MHz, unmeasured pins returned to GND. See Table 6.

Table 6. Capacitance

Parameter	Min	Max
Input capacitance	0	15pF
Output capacitance	0	20pF
I/O capacitance	0	25pF

DC Electrical Characteristics

Table 7 lists direct current characteristics for the Z86C08 High Temperature MCU at a temperature range of –40ºC to 150ºC.

Table 7. DC Characteristics, High Temperature Range

Sym	Parameter	V_{CC}	T_A = –40°C to +150°C Min	T_A = –40°C to +150°C Max	Typical @ 25°C[1]	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	0.8 V_{CC}	V_{CC}+0.3	2.1	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	V_{SS}–0.3	0.2 V_{CC}	1.0	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3	2.0	V		2
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		2
V_{IL}	Input Low Voltage	3.5V	V_{SS}–0.3	0.2 V_{CC}	1.0	V		2
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		2
V_{OH}	Output High Voltage	3.5V	V_{CC}–0.4		3.3	V	I_{OH} = –2.0mA	3
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0mA	3
		3.5V	V_{CC}–0.4		3.3	V	Low noise @ I_{OH} = –0.5mA	
		5.5V	V_{CC}–0.4		4.8	V	Low noise @ I_{OH} = –0.5mA	

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. Standard Mode (not Low EMI Mode).
4. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
5. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
6. A protection Schottky diode is required between the X_{IN} and V_{CC} pins.

Table 7. DC Characteristics, High Temperature Range (Continued)

Sym	Parameter	V_{CC}	T_A = –40°C to +150°C Min	Max	Typical @ 25°C[1]	Units	Conditions	Notes
V_{OL1}	Output Low Voltage	3.5V		0.8	0.2	V	I_{OL} = +4.0 mA	3
		5.5V		0.8	0.1	V	I_{OL} = +4.0 mA	3
		3.5V		0.8	0.2	V	Low noise @ I_{OL} = 1.0 mA	
		5.5V		0.8	0.1	V	Low noise @ I_{OL} = 1.0mA	
V_{OL2}	Output Low Voltage	3.5V		1.2	0.3	V	I_{OL} = +10mA	3
		5.5V		1.0	0.3	V	I_{OL} = +10mA	3
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		1.5	3.1	2.6	V	Maximum internal clock frequency	
I_{IL}	Input Leakage (Input bias current of comparator)	3.5V	–2.0	2.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–2.0	2.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	–2.0	2.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–2.0	2.0		µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range			V_{CC}–1.5		V		

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. Standard Mode (not Low EMI Mode).
4. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
5. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
6. A protection Schottky diode is required between the X_{IN} and V_{CC} pins.

Table 7. DC Characteristics, High Temperature Range (Continued)

Sym	Parameter	V_{CC}	T_A = –40°C to +150°C Min	Max	Typical @ 25°C[1]	Units	Conditions	Notes
I_{CC}	Supply Current	3.5V		8.0	3.0	mA	All Output and I/O Pins Floating @ 8MHz	3,4
		5.5V		11.0	4.4	mA	All Output and I/O Pins Floating @ 8MHz	3,4
		3.5V		10.0	3.6	mA	All Output and I/O Pins Floating @ 12 MHz	3,4
		5.5V		15.0	9.0	mA	All Output and I/O Pins Floating @ 12MHz	3,4
I_{CC1}	Standby Current	3.5V		2.5	0.7	mA	Halt Mode V_{IN} = 0V, V_{CC} @ 2 MHz	3,4
		5.5V		4.0	2.5	mA	Halt Mode V_{IN} = 0V, V_{CC} @ 2MHz	3,4
		3.5V		4.0	1.0	mA	Halt Mode V_{IN} = 0V, V_{CC} @ 8MHz	3,4
		5.5V		5.0	3.0	mA	Halt Mode V_{IN} = 0V, V_{CC} @ 8MHz	3,4
		3.5V		4.5	1.5	mA	Halt Mode V_{IN} = 0V, V_{CC} @ 12MHz	3,4
		5.5V		7.0	4.0	mA	Halt Mode V_{IN} = 0V, V_{CC} @ 12MHz	3,4

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. Standard Mode (not Low EMI Mode).
4. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
5. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
6. A protection Schottky diode is required between the X_{IN} and V_{CC} pins.

Table 7. DC Characteristics, High Temperature Range (Continued)

Sym	Parameter	V_{CC}	T_A = –40°C to +150°C Min	Max	Typical @ 25°C[1]	Units	Conditions	Notes
I_{CC}	Supply Current (Low Noise Mode)	3.5V		3.5	1.5	mA	All Output and I/O Pins Floating @ 1MHz	4
		5.5V		7.0	3.8	mA	All Output and I/O Pins Floating @ 1MHz	4
		3.5V		5.8	2.5	mA	All Output and I/O Pins Floating @ 2MHz	4
		5.5V		9.0	4.0	mA	All Output and I/O Pins Floating @ 2MHz	4
		3.5V		8.0	3.0	mA	All Output and I/O Pins Floating @ 4MHz	4
		5.5V		11.0	4.4	mA	All Output and I/O Pins Floating @ 4MHz	4
I_{CC1}	Standby Current (Low Noise Mode)	3.5V		2.5	0.7	mA	Halt Mode V_{IN} = 0V, V_{CC} @ 2 MHz	4
		5.5V		4.0	2.5	mA	Halt Mode V_{IN} = 0V, V_{CC} @ 2 MHz	4
		3.5V		3.5	0.9	mA	Halt Mode V_{IN} = 0V, V_{CC} @ 4 MHz	4
		5.5V		5.0	2.8	mA	Halt Mode V_{IN} = 0V, V_{CC} @ 4 MHz	4
I_{CC2}	Standby Current	3.5V		20	2.0	µA	Stop Mode V_{IN} = 0V, V_{CC}; WDT is not Running	4,5,6
		5.5V		20	4.0	µA	Stop Mode V_{IN} = 0V, V_{CC}; WDT is not Running	4,5,6

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. Standard Mode (not Low EMI Mode).
4. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
5. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
6. A protection Schottky diode is required between the X_{IN} and V_{CC} pins.

Table 7. DC Characteristics, High Temperature Range (Continued)

Sym	Parameter	V_{CC}	T_A = –40°C to +150°C Min	Max	Typical @ 25°C[1]	Units	Conditions	Notes
I_{ALL}	Auto Latch Low Current	3.5V		16	12	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		32	24	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.5V	–10.0		–4.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V	–20.0		–10.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:
1. Typical values are read at a V_{CC} of 5.0V.
2. Port 2, Port 3, and Port 0 only.
3. Standard Mode (not Low EMI Mode).
4. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
5. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
6. A protection Schottky diode is required between the X_{IN} and V_{CC} pins.

AC Electrical Timing Characteristics

Figure 5 illustrates alternating current timing for the Z86C08 High Temperature MCU.

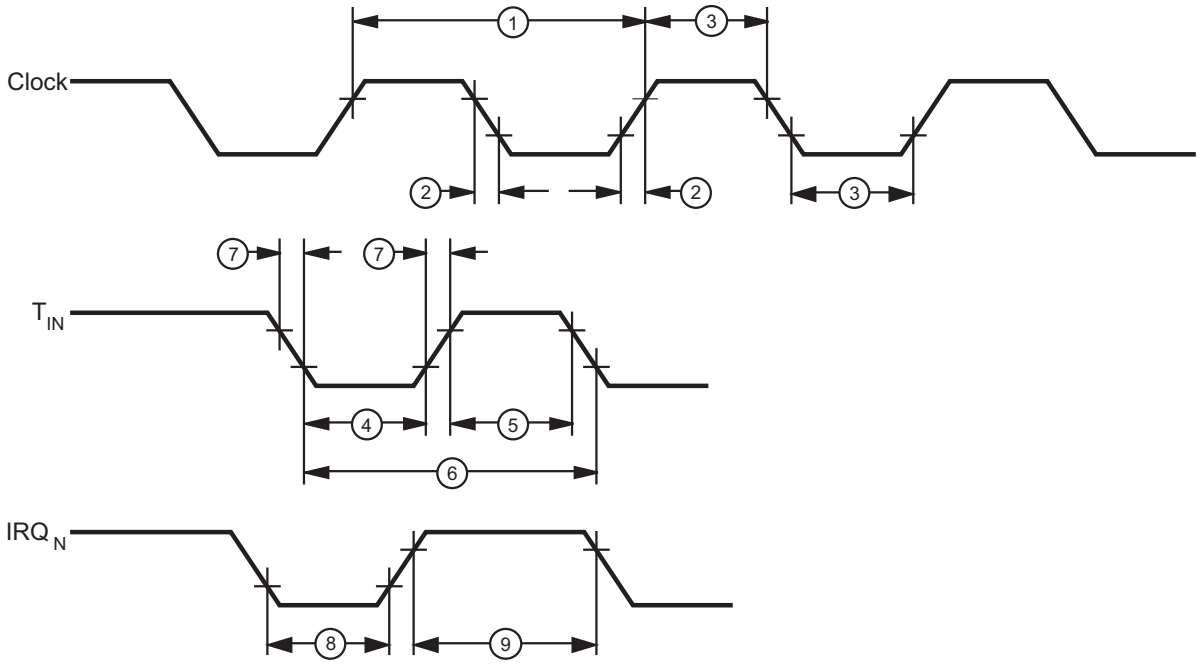


Figure 5. AC Electrical Timing

Standard Mode at High Temperature

Table 8 lists timing characteristics in Standard Mode at high temperature for the timing diagram noted in Figure 5 on page 14.

Table 8. AC Electrical Timing: Standard Mode at High Temperature

				T_A = –40ºC to +150ºC						
				8MHz		12MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	3.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	T_WC	Input Clock Width	3.5V		62		41	ns	1
			5.5V		62		41	ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	$5T_PC$		$5T_PC$			1
			5.5V	$5T_PC$		$5T_PC$			1
6	T_PT_{IN}	Timer Input Period	3.5V	$8T_PC$		$8T_PC$			1
			5.5V	$8T_PC$		$8T_PC$			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.5V	$5T_PC$		$5T_PC$			1,2
			5.5V	$5T_PC$		$5T_PC$			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.5V	23		23		ms	1,3
			5.5V	8		8		ms	1,3
11	T_{POR}	Power-On Reset Time	3.5V	46	180	46	180	ms	1,4
			5.5V	16	100	16	100	ms	1,4

Notes:
1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request made through Port 3 (P33–P31).
3. Typical T_{WDT} is 20msec @ 5.0V and 25ºC.
4. Typical T_{POR} is 40msec @ 5.0V and 25ºC.

Low Noise Mode at High Temperature

Table 9 describes timing characteristics in Low Noise Mode at high temperature for the timing diagram noted in Figure 5 on page 14.

Table 9. AC Electrical Timing: Low Noise Mode at High Temperature

				T_A = –40ºC to +150ºC						
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	3.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC, T_FC	Clock Input Rise and Fall Times	3.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	3.5V	500		125		ns	1
			5.5V	500		125		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	$2.5T_PC$		$2.5T_PC$			1
			5.5V	$2.5T_PC$		$2.5T_PC$			1
6	T_PT_{IN}	Timer Input Period	3.5V		$4T_PC$	$4T_PC$			1
			5.5V		$4T_PC$	$4T_PC$			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL Low Time	Interrupt Request Input Low Time	3.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH High Time	Interrupt Request Input High Time	3.5V	$2.5T_PC$		$2.5T_PC$			1,2
			5.5V	$2.5T_PC$		$2.5T_PC$			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time for Time-out	3.5V	23		23		ms	1,3
			5.5V	8		8		ms	1,3
11	T_{POR}	Power-On Reset Time	3.5V	46	180	46	180	ms	1,4
			5.5V	16	100	16	100	ms	1,4

Notes:
1. Timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Typical T_{WDT} is 20msec @ 5.0V and 25ºC.
4. Typical T_{POR} is 40msec @ 5.0V and 25ºC.

Low-EMI Emission Mode

The Z86C08 High Temperature MCU can be programmed to operate in a low-EMI emission mode by means of an OTP bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical
- Internal SCLK and TCLK operation limited to a maximum of 4 MHz–250 ns cycle time
- Output drivers typically exhibit resistances of 500Ω
- Oscillator divide-by-two circuitry eliminated

The Low EMI Mode is a mask option bit that can be selected by the customer at the time the ROM code is programmed into the masked ROM. The default condition is a disabled Low EMI Mode.

Pin Functions

The Z86C08 High Temperature MCU connects to external devices via the following pins.

X_{IN}, X_{OUT}. *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (12 MHz max) to the on-chip clock oscillator and buffer.

Auto Latch. The Auto Latch places valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch sets the ports to an undetermined state of 0 or 1. The default condition is *Auto Latches enabled*. The Auto Latch can be disabled by programming the Auto Latch Disable Mask option bit.

Port 0, P02–P00. Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs, as shown in Figure 6.

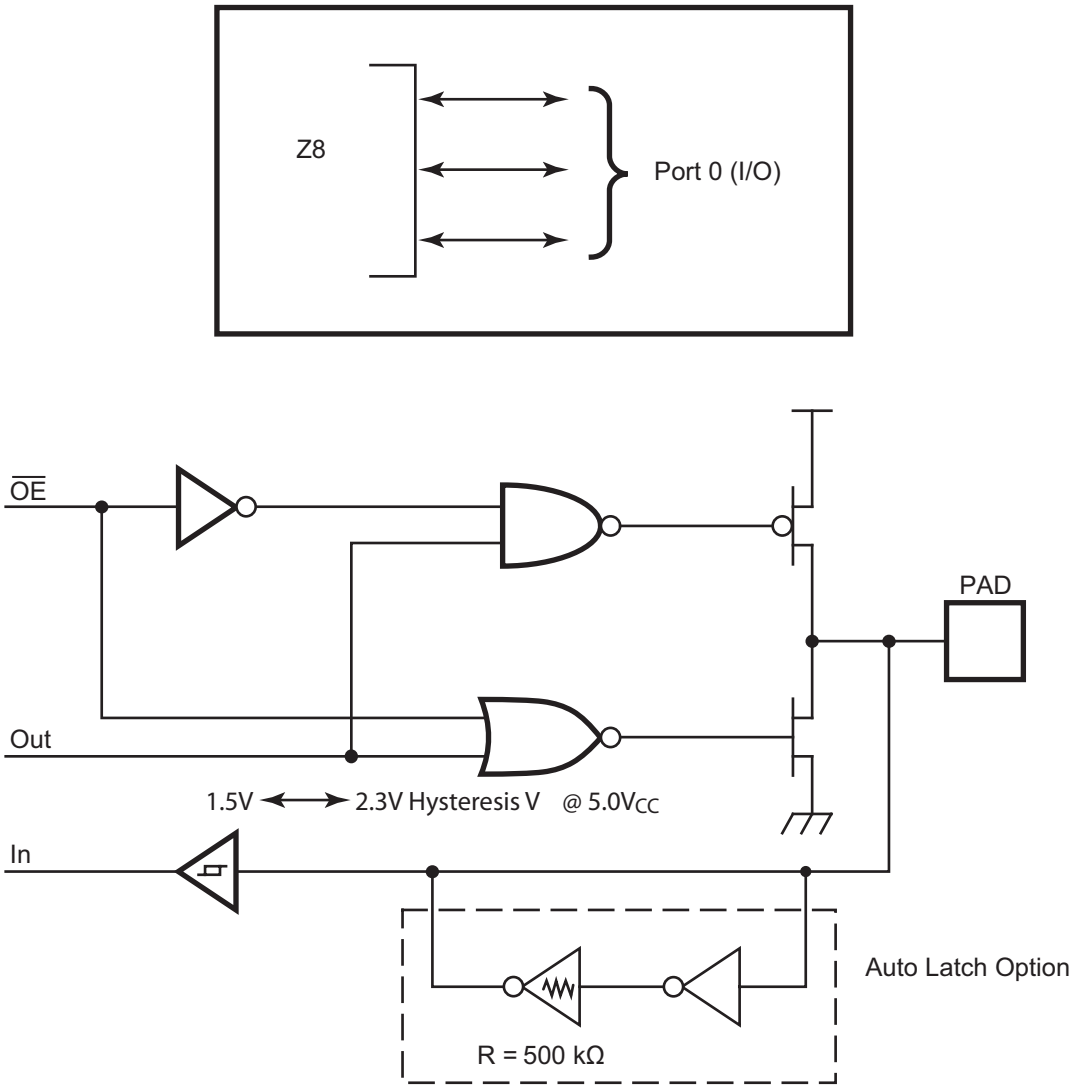


Figure 6. Port 0 Configuration

Port 2, P27–P20. Port 2 is an 8-bit, bit programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain, as shown in Figure 7.

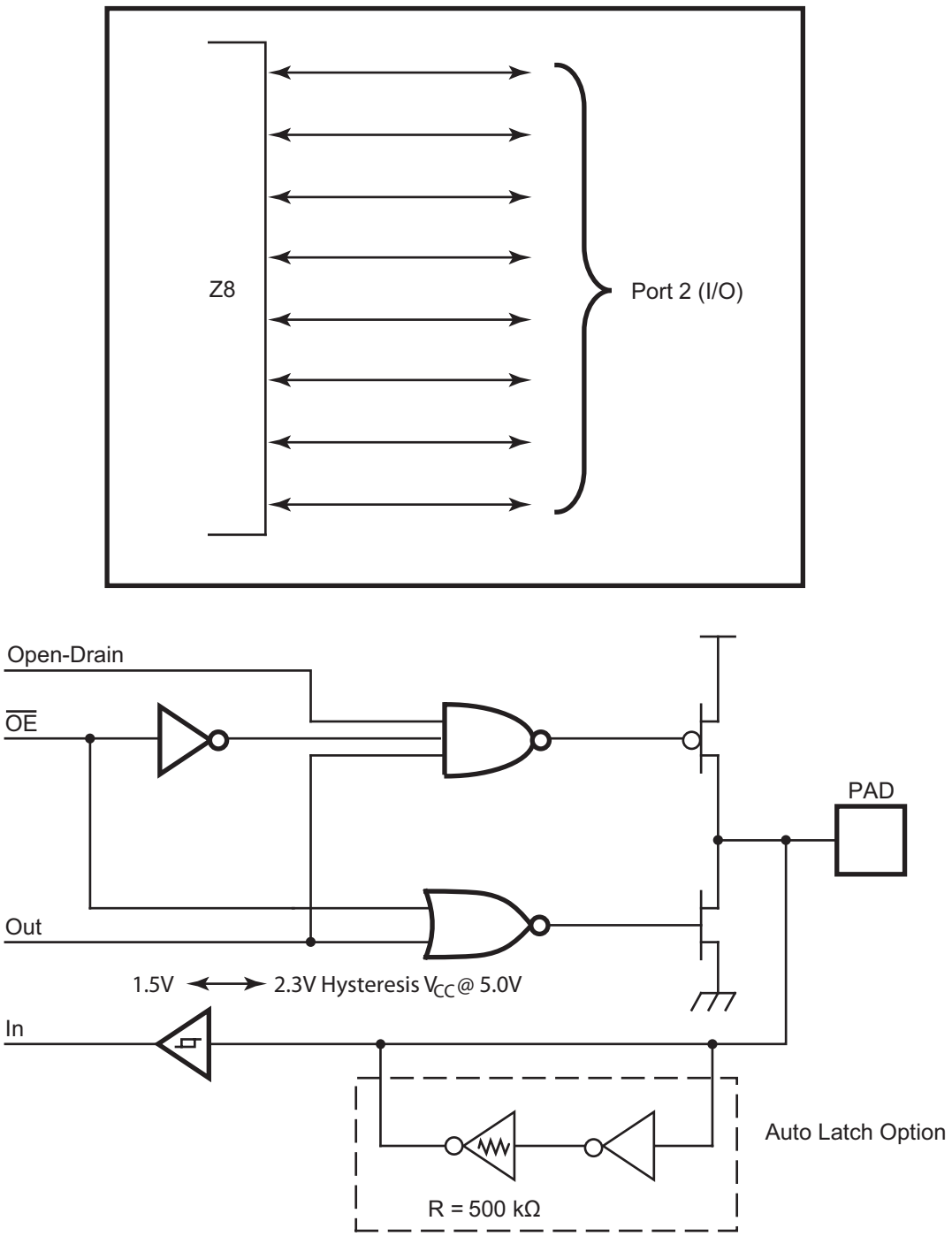


Figure 7. Port 2 Configuration

Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs.

These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN}, as shown in Figure 8.

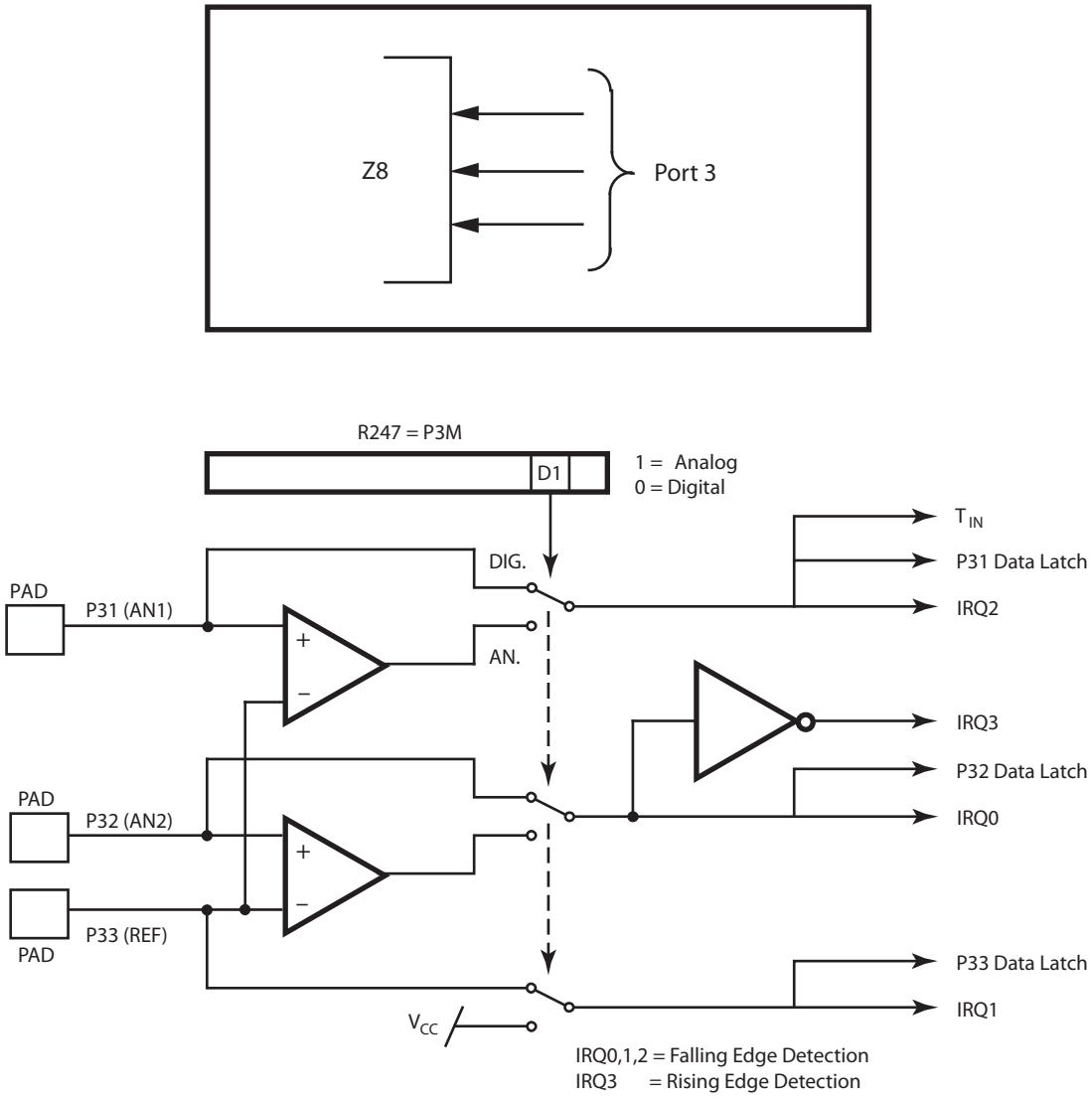


Figure 8. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; zero-crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in Stop Mode. At 25ºC , the common voltage range is 0–4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90dB and 60dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

The comparator requires two NOPs to be stable after setting its enable bit. Zilog recommends that interrupts IRQ0, IRQ1, and IRQ2 be disabled before setting the enable bit. After enabling the comparator, IRQ0, IRQ1, and IRQ2 should be cleared prior to reenabling these interrupts. Zilog also recommends clearing these interrupts when disabling the comparator.

Functional Description

The following special functions are incorporated into the Z8 devices to enhance the standard Z8 core architecture and to provide the user with increased design flexibility.

RESET

A RESET can be triggered in the following two ways:

- Power-On Reset
- Watch-Dog Timer Reset

Power-On Reset (POR)

Upon power-up, the Power-On Reset circuit waits for T_{POR} ms plus 18 clock cycles, then starts program execution at address `000Ch`, as shown in Figure 9. The Z8 control registers' reset value is indicated in Table 10. The V_{CC} supply voltage must be brought up to the specified V_{CC} operating voltage range before the T_{POR} expires.

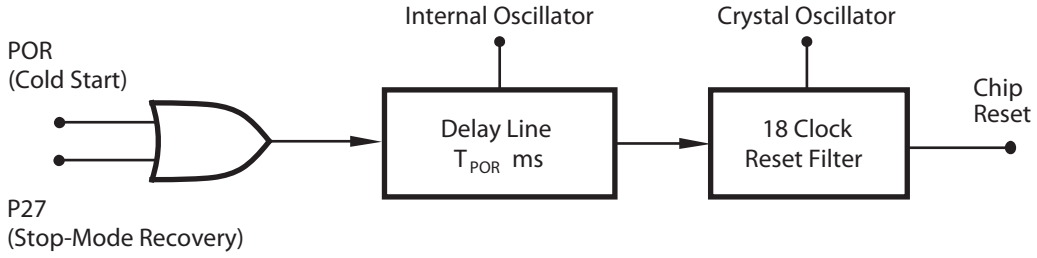


Figure 9. Internal Reset Configuration

Table 10. Z8 Control Registers Reset Values*

		Reset Condition								
Address	**Register**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
FFh	SPL	0	0	0	0	0	0	0	0	
FDh	RP	0	0	0	0	0	0	0	0	
FCh	FLAGS	U	U	U	U	U	U	U	U	
FBh	IMR	0	U	U	U	U	U	U	U	
FAh	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9h	IPR	U	U	U	U	U	U	U	U	
F8h*	P01M	U	U	U	0	U	U	0	1	
F7h*	P3M	U	U	U	U	U	U	0	0	
F6h*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5h	PRE0	U	U	U	U	U	U	U	0	
F4h	T0	U	U	U	U	U	U	U	U	
F3h	PRE1	U	U	U	U	U	U	0	0	
F2h	T1	U	U	U	U	U	U	U	U	
F1h	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a stop-mode recovery using P27 pin. A subsequent reset causes these control registers to be reconfigured as indicated in Table 10 and the user must avoid bus contention on the port pins or it may affect device reliability.

A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- *Power Bad* to *Power Good* status
- Stop-mode recovery
- WDT time-out
- WDH time-out

Watch-Dog Timer Reset

The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

Program Memory

The Z86C08 High Temperature MCU addresses up to 2.0KB of internal program memory, as shown in Figure 10. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–2047 are on-chip masked programmable ROM.

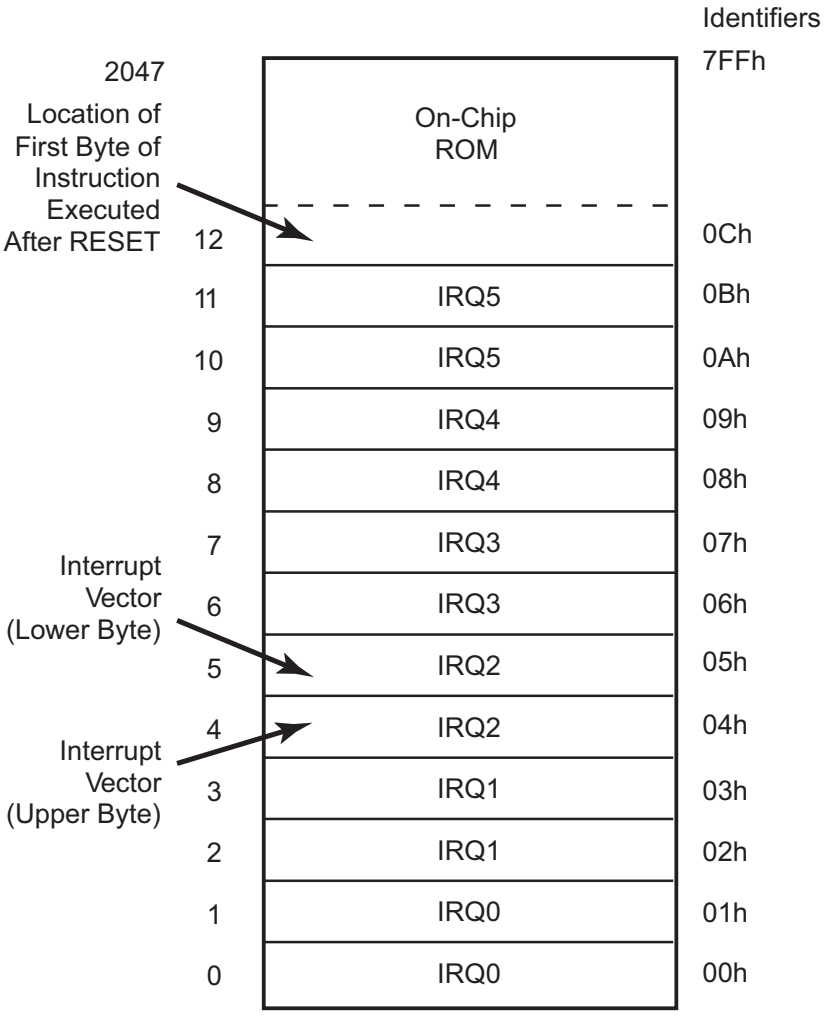


Figure 10. Program Memory Map

Register File

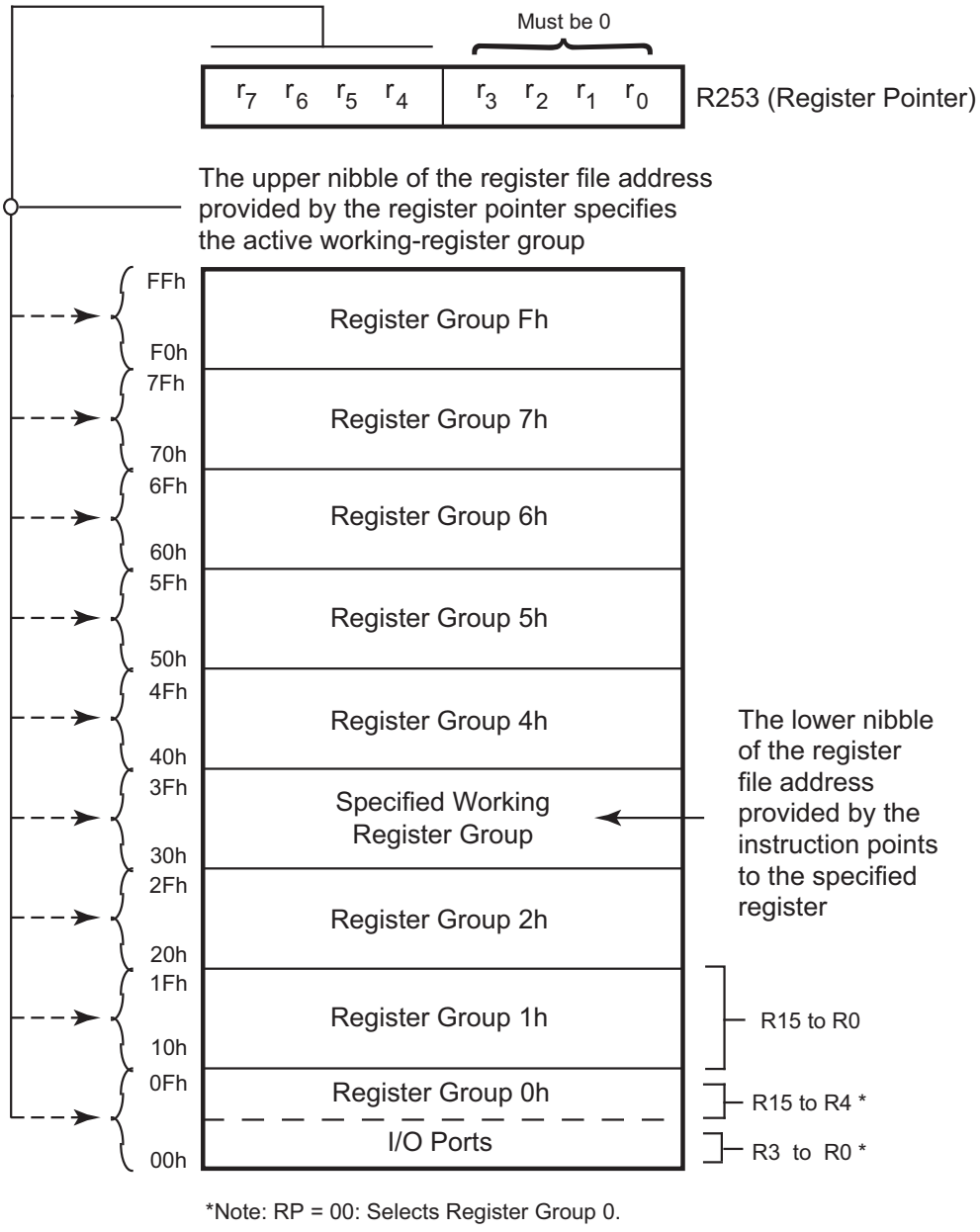
The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255, respectively, as shown in Figure 11. General-purpose registers occupy the 04h to 7Fh address space. I/O ports are mapped as per the existing CMOS Z8.

Location		Identifiers
255 (FFh)	Stack Pointer (Bits 7-0)	SPL
254 (FEh)	General-Purpose Register	GPR
253 (FDh)	Register Pointer	RP
252 (FCh)	Program Control Flags	FLAGS
251 (FBh)	Interrupt Mask Register	IMR
250 (FAh)	Interrupt Request Register	IRQ
249 (F9h)	Interrupt Priority Register	IPR
248 (F8h)	Ports 0–1 Mode	P01M
247 (F7h)	Port 3 Mode	P3M
246 (F6h)	Port 2 Mode	P2M
245 (F5h)	T0 Prescaler	PRE0
244 (F4h)	Timer/Counter0	T0
243 (F3h)	T1 Prescaler	PRE1
242 (F2h)	Timer/Counter1	T1
241 (F1h)	Timer Mode	TMR
240 (F0h) 128 (80h)	Not Implemented	
127 (7Fh) • • • 4 (04h)	General-Purpose Registers	
3 (03h)	Port 3	P3
2 (02h)	Port 2	P2
1 (01h)	Reserved	P1
0 (00h)	Port 0	P0

Figure 11. Register File

The Z8 instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing short 4-bit register addressing mode using the Register Pointer.

In the 4-bit address mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer, shown in Figure 12, addresses the starting location of the active working-register group.



*Note: RP = 00: Selects Register Group 0.

Figure 12. Register Pointer

Stack Pointer

The Z8 features an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 120 general-purpose registers from 04h to 7Fh.

General-Purpose Registers (GPR)

These registers are undefined after the device is powered up. The registers keep their most recent value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range.

Note: Register R254 is designated as a general-purpose register and is set to 00h after any reset or stop-mode recovery.

Counter/Timer

There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only, as shown in Figure 13 on page 29.

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode Register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or nonretriggerable, or used as a gate input for the internal clock.

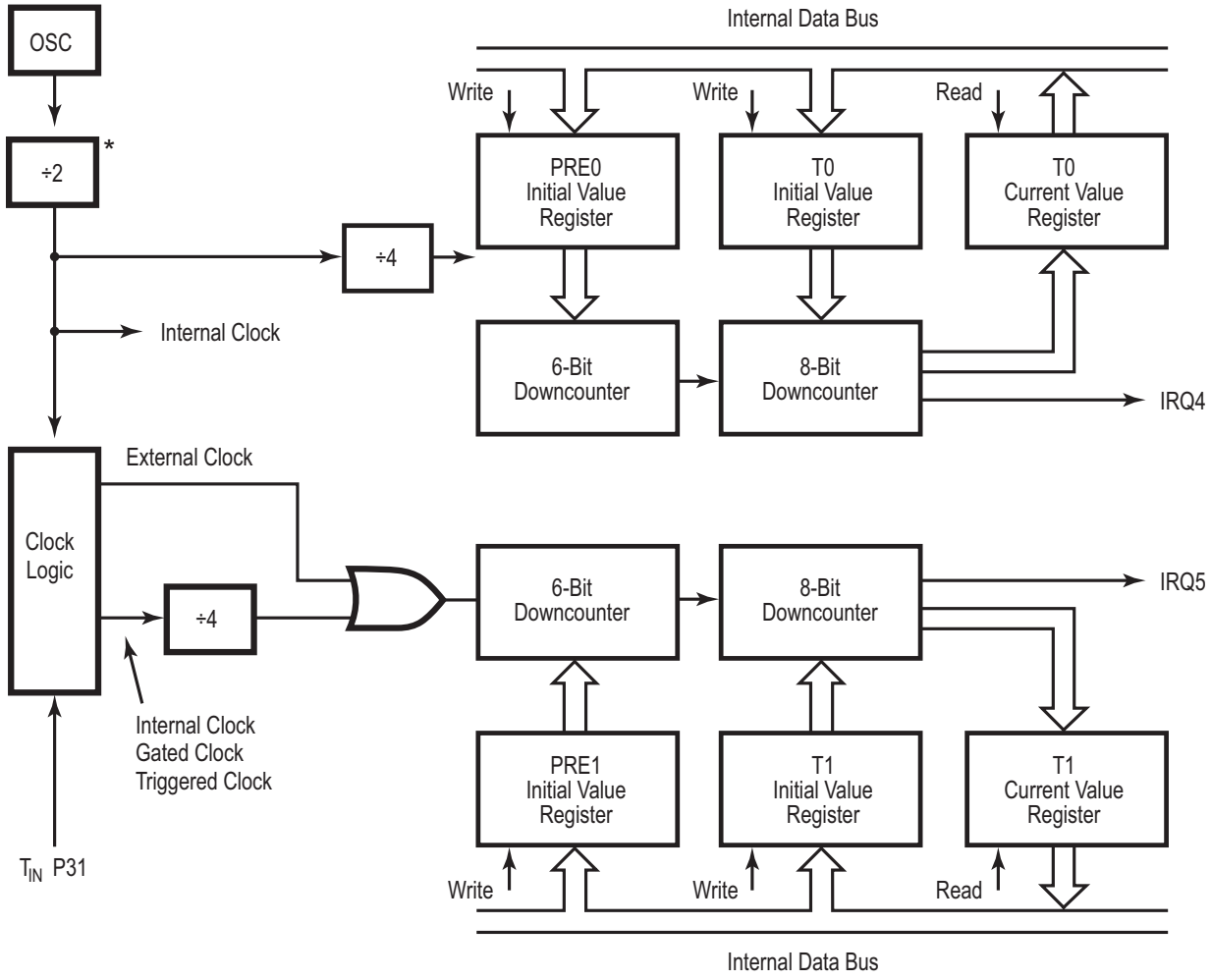


Figure 13. Counter/Timers Block Diagram

Note: *The divide-by-two step is bypassed if Low EMI Mode is selected.

Interrupts

The Z8 features six interrupts from six different sources. These interrupts are maskable and prioritized, as shown in Figure 14 on page 30. The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two

counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests, as indicated in Table 11.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an Interrupt Request is granted, thus disabling all subsequent interrupts, saving the Program Counter and Status Flags, and then branching to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests requires service.

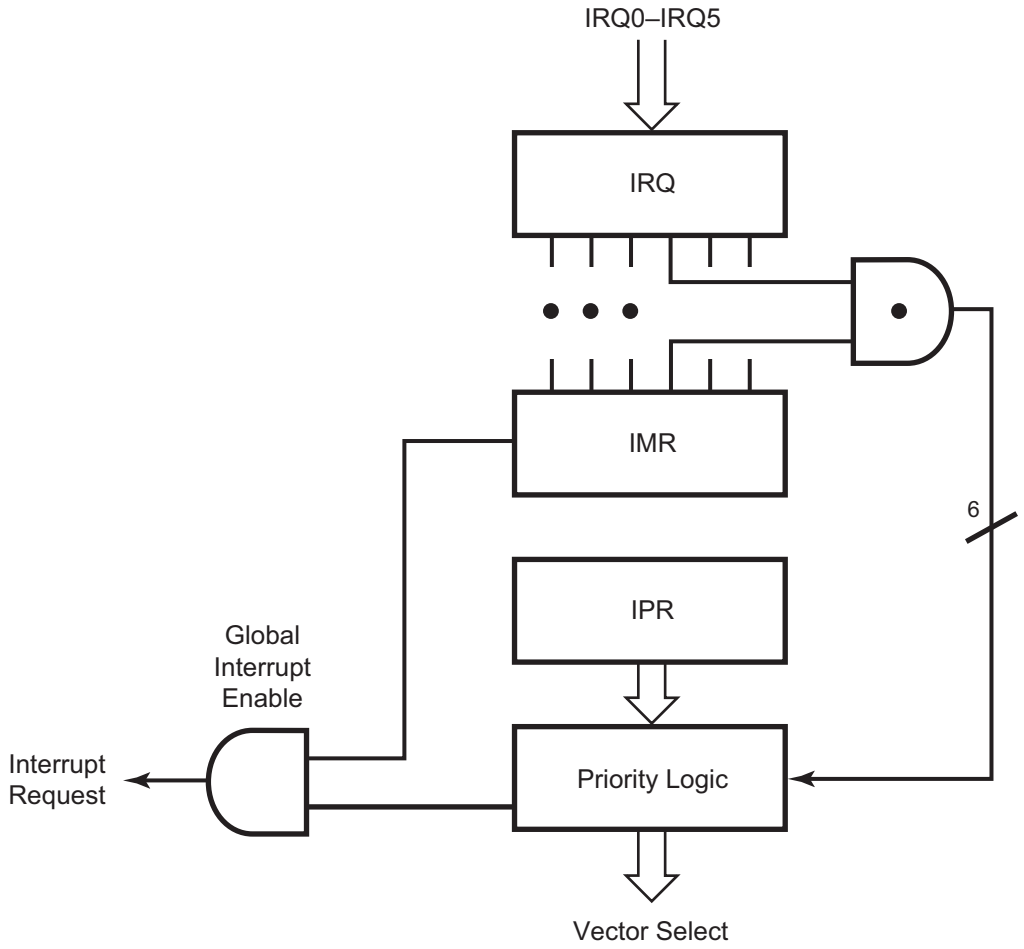


Figure 14. Interrupt Block Diagram

Note: The user must select any Z86E08 Mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

Table 11. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F) Edge
IRQ1	REF(P33)	2,3	External (F) Edge
IRQ2	AN1(P31)	4,5	External (F) Edge
IRQ3	AN2(P32)	6,7	External (R) Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Note: F = Falling edge triggered; R = Rising edge triggered.

Clock

The Z8 on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (X_{IN} = INPUT, X_{OUT} = OUTPUT). The crystal should be AT-cut, up to 12 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across X_{IN} and X_{OUT} using the vendor's crystal recommended capacitor values from each pin directly to device ground pin 14, as shown in Figure 15.

Note: The crystal capacitor loads should be connected directly to the V_{SS} pin to reduce Ground noise injection. They should not connect to system Ground.

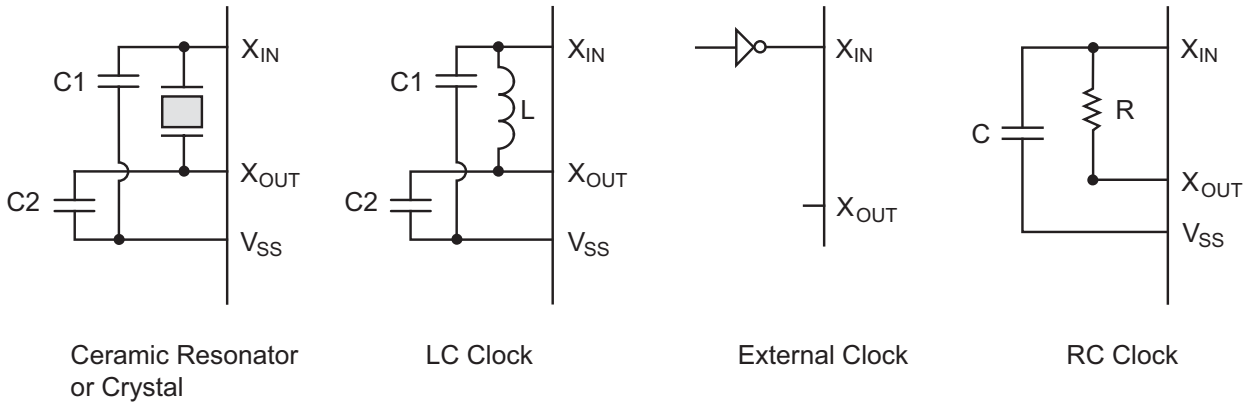


Figure 15. Oscillator Configuration

Table 12. Typical Frequency vs. RC Values: V_{CC} = 5.0 V @ 25°C

	Load Capacitor							
	33pF		56pF		100pF		0.001µF	
Resistor (R)	A	B	A	B	A	B	A	B
1.0MΩ	33kHz	31kHz	20kHz	20kHz	12kHz	11kHz	1.4kHz	1.4kHz
560KΩ	56kHz	52kHz	34kHz	32kHz	20kHz	19kHz	2.5kHz	2.4kHz
220KΩ	144kHz	130kHz	84kHz	78kHz	48kHz	45kHz	6kHz	6kHz
100KΩ	315kHz	270kHz	182kHz	164kHz	100kHz	95kHz	12kHz	12kHz
56KΩ	552kHz	480kHz	330kHz	300kHz	185kHz	170kHz	23kHz	22kHz
20KΩ	1.4MHz	1MHz	884kHz	740kHz	500kHz	450kHz	65kHz	61kHz
10KΩ	2.6MHz	2MHz	1.6MHz	1.3MHz	980kHz	820kHz	130kHz	123kHz
5KΩ	4.4MHz	3MHz	2.8MHz	2MHz	1.7MHz	1.3MHz	245kHz	225kHz
2KΩ	8MHz	5MHz	6MHz	4MHz	3.8MHz	2.7MHz	600kHz	536kHz
1KΩ	12MHz	7MHz	8.8MHz	6MHz	6.3MHz	4.2MHz	1.0MHz	950kHz

Notes:
A = Standard Mode frequency.
B = Low EMI Mode frequency.

Table 13. Typical Frequency vs. RC Values, V_{CC} = 3.5 V @ 25°C

Resistor (R)	Load Capacitor							
	33 pF		56 pF		100 pF		0.001 µF	
	A	B	A	B	A	B	A	B
1.0 MΩ	18 kHz	18 kHz	12 kHz	12 kHz	7.4 kHz	7.7 kHz	1 kHz	1 kHz
560 KΩ	30 kHz	30 kHz	20 kHz	20 kHz	12 kHz	12 kHz	1.6 kHz	1.6 kHz
220 KΩ	70 kHz	70 kHz	47 kHz	47 kHz	30 kHz	30 kHz	4 kHz	4 kHz
100 KΩ	150 kHz	148 kHz	97 kHz	96 kHz	60 kHz	60 kHz	8 kHz	8 kHz
56 KΩ	268 kHz	250 kHz	176 kHz	170 kHz	100 kHz	100 kHz	15 kHz	15 kHz
20 KΩ	690 MHz	600 kHz	463 kHz	416 kHz	286 kHz	266 kHz	40 kHz	40 kHz
10 KΩ	1.2 MHz	1 MHz	860 kHz	730 kHz	540 kHz	480 kHz	80 kHz	76 kHz
5 KΩ	2 MHz	1.7 MHz	1.5 MHz	1.2 MHz	950 kHz	820 kHz	151 kHz	138 kHz
2 KΩ	4.6 MHz	3 MHz	3.3 MHz	2.4 MHz	2.2 MHz	1.6 MHz	360 kHz	316 kHz
1 KΩ	7 MHz	4.6 MHz	5 MHz	3.6 MHz	3.6 MHz	2.6 MHz	660 kHz	565 kHz

Notes:
A = Standard Mode frequency.
B = Low EMI Mode frequency.

Halt Mode

This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit Halt Mode. After the interrupt service routine, the program continues from the instruction after the Halt.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of Halt Mode.

Stop Mode

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. Stop Mode is released by a RESET through a stop-mode recovery (pin P27). A LOW INPUT condition on P27 releases the Stop Mode. Program execution begins at location `000Ch`. However, when P27 is used to release Stop Mode, the I/O port mode registers are not reconfigured to their default power-on conditions. Therefore the I/O, configured as output when the Stop instruction was executed, is prevented from

glitching to an unknown state. To use this P27 release approach with Stop Mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
Stop
```

Note: X = Dependent on user's application.

Note: A Low level detected on pin P27 takes the device out of Stop Mode, even if it is configured as an output.

To enter Stop or Halt Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. The user must execute a NOP (Op Code = FFh) immediately before the appropriate SLEEP instruction, such as:

```
FFh     NOP     ; clear the pipeline
6Fh     Stop    ; enter Stop Mode
        or
FFh     NOP     ; clear the pipeline
7Fh     Halt    ; enter Halt Mode
```

Note: On the CCP emulator, a software workaround must be used to enable P27 as the stop-mode recovery source.

Watch-Dog Timer (WDT)

The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 T_{WDT} period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z = 1, S = 0, V = 0.

WDT = 5Fh

Op Code WDT (5Fh)

The first time Op Code 5Fh is executed, the WDT is enabled; subsequent execution clears the WDT counter. This clearing of the counter must be performed at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 crystal clock cycles. The software enabled WDT does not run in Stop Mode.

Op Code WDH (4Fh)

When this instruction is executed it enables the WDT during Halt. If not, the WDT stops when entering Halt. This instruction does not clear the counters – it just makes it possible to operate the WDT during Halt Mode. A WDH instruction executed without executing WDT (5Fh) yields no effect.

Permanent WDT

Selecting the hardware-enabled permanent WDT Mask ROM option bit automatically enables the WDT upon exiting reset. The permanent WDT always runs in Halt Mode and Stop Mode, and it cannot be disabled.

Note: On the CCP emulator, a software workaround must be used to enable the software- or hardware-enabled WDT.

Auto Reset Voltage (V_{LV})

The Z8 features an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV}. Figure 16 shows the Auto Reset Voltage versus temperature.

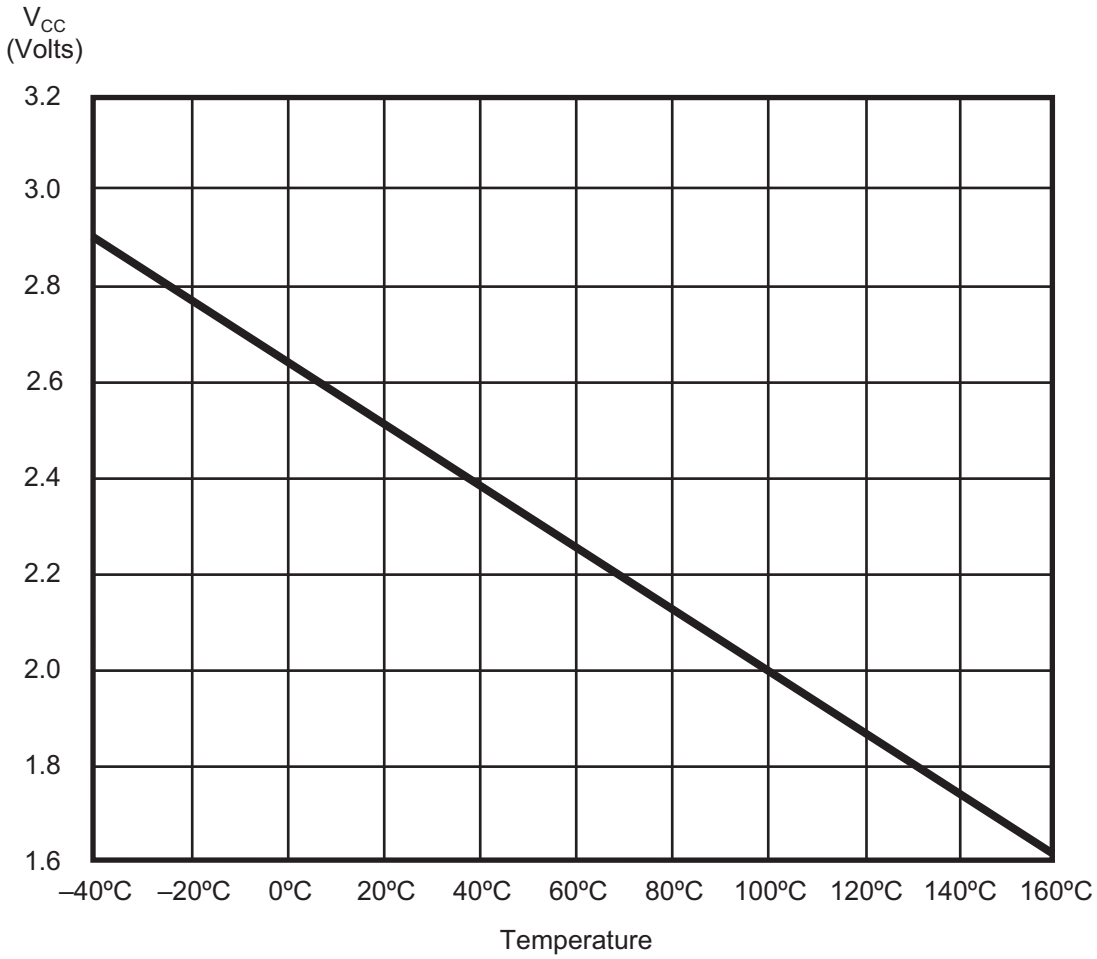


Figure 16. Typical Auto Reset Voltage (V_{LV}) vs. Temperature

Mask ROM Option Bit Description

Mask ROM option bits for the Z86C08 High Temperature MCU are described in this section. The options are selected by the customer at the time ROM code is submitted.

Low-EMI Emission. The Z8 MCU can be programmed to operate in a low-EMI emission (low-noise) mode by means of a Mask ROM bit option. Use of this feature results in:

- All drivers slew rates are typically reduced to 10 ns
- Internal SCLK and TCLK = crystal operation limited to a maximum of 4 MHz–250 ns cycle time
- Output drivers typically exhibit resistances of 500 ohms
- Oscillator divide-by-two circuitry eliminated

RC Oscillator. The RC Oscillator option bit, when selected, enables the internal RC oscillator to connect to the X_{OUT} and X_{IN} pins while disabling the internal crystal oscillator to X_{OUT} and X_{IN}.

ROM Protect. ROM Protect fully protects the Z8 ROM code from being read externally. When ROM Protect is selected, the LDC and LDCI instructions are supported; therefore, ROM look-up tables can be used (however, the Z86C08 High Temperature MCU does not support the LDE and LDEI instructions). When the device is programmed for ROM Protect, the Low-Noise feature is not automatically enabled.

Auto Latch Disable. Auto Latch Disable option bit, when programmed, globally disables all Auto Latches.

Permanent WDT Enable. The hardware-enabled permanent WDT Enable option bit, when programmed, enables the WDT permanently after exiting reset. Unlike software-enabled WDT, the hardware-enabled permanent WDT cannot be stopped in Halt or Stop modes.

32 kHz Enable. The 32 kHz Enable option bit enables the 32 kHz oscillator circuit and disables the high-frequency crystal oscillator circuit. This option bit is disabled if the RC oscillator option bit is programmed.

Control Registers

This chapter defines the following registers.

R241 Timer Mode Register (TMR) – see page 39

Counter/Timer 1 Register (T1), R242 – see page 40

Prescaler 1 Register (PRE1), R243; Write Only – see page 40

Counter/Timer 0 Register (T0), R244 – see page 41

Prescaler 0 Register (PRE0), R245; Write Only – see page 41

Port 2 Mode Register (P2M), R246; Write Only – see page 42

Port 3 Mode Register (P3M), R247: Write Only – see page 42

Port 0 and 1 Mode Registers (P01M), R248; Write Only – see page 43

Interrupt Priority Register (IPR), R249; Write Only – see page 43

Interrupt Request Register (IRQ), R250; Read/Write – see page 44

Interrupt Mask Register (IMR), R251; Read/Write – see page 45

Flag Register (Flags), R252; Read/Write – see page 46

Register Pointer (RP), R253; Read/Write – see page 47

General Purpose Register (GPR), R254; Read/Write – see page 47

Stack Pointer Low (SPL), R255; Read/Write – see page 48

Timer/Counter Registers

The Timer Mode Register is defined in Table 14.

Table 14. R241 Timer Mode Register (TMR)

Bit	7	6	5	4	3	2	1	0
Field	Reserved		TINMODE		T1COUNT	T1	T0COUNT	T0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F1h Bank 0h							

Bit	Description
[7:6]	**Reserved** These bits are reserved and must be programmed to 00.
[5:4] TINMODE	**T_{IN} Mode** 00: External Clock Input. 01: Gate Input. 10: Trigger Input (nonretriggerable). 11: Trigger Input (retriggerable).
[3] T1COUNT	**T1 Count** 0: Disable. 1: Enable.
[2] T1	**T1** 0: No Function. 1: Load T1.
[1] T0COUNT	**T0 Count** 0: Disable. 1: Enable.
[0] T0	**T0** 0: No Function. 1: Load T0.

The Counter/Timer 1 Register is defined in Table 15.

Table 15. Counter/Timer 1 Register (T1), R242

Bit	7	6	5	4	3	2	1	0
Field	T1							
RESET	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F1h Bank 0h							
Note: R = Read, W = Write, X = Indeterminate.								

Bit	Description
[7:0] T1	**Timer 1** R: T1 current value. W: T1 initial value; range = 1–256 decimal, 01h–00h.

The Prescaler 1 Register is defined in Table 16.

Table 16. Prescaler 1 Register (PRE1), R243; Write Only

Bit	7	6	5	4	3	2	1	0
Field	PRES						CLK	T1COUNT
RESET	X	X	X	X	X	X	0	0
R/W	W	W	W	W	W	W	W	W
Address	F3h Bank 0h							
Note: W = Write, X = Indeterminate.								

Bit	Description
[7:2] PRES	**Prescaler Modulo** Range = 1–64 decimal, 01h–00h; write only.
[1] CLK	**Clock Source** 0: T1 External Timing Input (T_{IN}) Mode. 1: T1 Internal.
[0] T1COUNT	**T1 Count Mode** 0: Single Pass. 1: Modulo N.

The Counter/Timer 0 Register is defined in Table 17.

Table 17. Counter/Timer 0 Register (T0), R244

Bit	7	6	5	4	3	2	1	0
Field	T0							
RESET	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F4h Bank 0h							
Note: R = Read, W = Write, X = Indeterminate.								

Bit	Description
[7:0] T0	**Timer 0** R: T0 current value. W: T0 initial value; range = 1–256 decimal, 01h–00h.

The Prescaler 0 Register is defined in Table 18.

Table 18. Prescaler 0 Register (PRE0), R245; Write Only

Bit	7	6	5	4	3	2	1	0
Field	PRES						Reserved	T0COUNT
RESET	X	X	X	X	X	X	X	0
R/W	W	W	W	W	W	W	W	W
Address	F5h Bank 0h							
Note: W = Write, X = Indeterminate.								

Bit	Description
[7:2] PRES	**Prescaler Modulo** Range = 1–64 decimal; 01h–00h.
[1]	**Reserved** This bit is reserved and must be programmed to 0.
[0] T0COUNT	**T0 Count Mode** 0: Single Pass. 1: Modulo N.

Port Registers

The Port 2 Mode Register is defined in Table 19.

Table 19. Port 2 Mode Register (P2M), R246; Write Only

Bit	7	6	5	4	3	2	1	0
Field	P2M							
RESET	1	1	1	1	1	1	1	1
R/W	W	W	W	W	W	W	W	W
Address	F6h Bank 0h							
Note: W = Write.								

Bit	Description
[7:0] P2M	**P20–P27 I/O Definition** 0: Defines bit as Output. 1: Defines bit as Input.

The Port 3 Mode Register is defined in Table 20.

Table 20. Port 3 Mode Register (P3M), R247: Write Only

Bit	7	6	5	4	3	2	1	0
Field	Reserved						P3I	P2O
RESET	X	X	X	X	X	X	0	0
R/W	W	W	W	W	W	W	W	W
Address	F7h Bank 0h							
Note: W = Write, X = Indeterminate.								

Bit	Description
[7:2]	**Reserved** These bits are reserved and must be programmed to 000000.
[1] P3I	**Port 3 Inputs** 0: Digital Mode. 1: Analog Mode.
[0] P2O	**Port 2 Outputs** 0: Open-Drain. 1: Push-Pull.

The Port 0 and 1 Mode registers are defined in Table 21.

Table 21. Port 0 and 1 Mode Registers (P01M), R248; Write Only

Bit	7	6	5	4	3	2	1	0
Field	Reserved						P0*x*	
RESET	X	X	X	0	X	X	0	1
R/W	W	W	W	W	W	W	W	W
Address	F8h Bank 0h							

Note: W = Write, X = Indeterminate.

Bit	Description
[7:3]	**Reserved** These bits are reserved and must be programmed to 00000.
[2]	**Reserved** This bit is reserved and must be programmed to 1.
[1:0] P0*x*	**P02–P00 Mode** 00: Output. 01: Input.

Note: *x* indicates bits 2 and 0.

Interrupt Registers

The Interrupt Priority Register is defined in Table 22.

Table 22. Interrupt Priority Register (IPR), R249; Write Only

Bit	7	6	5	4	3	2	1	0
Field	Reserved		IRQ3,5	INT		IRQ0,2	IRQ1,4	INT
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
Address	F9h Bank 0h							

Note: W = Write, X = Indeterminate.

Bit	Description
[7:6]	**Reserved** These bits are reserved and must be programmed to 00.
[5] IRQ*x*	**IRQ3, IRQ5 Priority (Group A)** 0: IRQ5 > IRQ3. 1: IRQ3 > IRQ5.

Note: *Selecting a reserved mode causes an undefined operation.

Bit	Description (Continued)
[4:3,0] INT	**Interrupt Group Priority** 000: Reserved.* 001: C > A > B. 010: A > B > C. 011: A > C > B. 100: B > C > A. 101: C > B > A. 110: B > A > C. 111: Reserved.
[2] IRQ0,2	**IRQ0, IRQ2 Priority (Group B)** 0: IRQ2 > IRQ0. 1: IRQ0 > IRQ2.
[1] IRQ1,4	**IRQ1, IRQ4 Priority (Group C)** 0: IRQ1 > IRQ4. 1: IRQ4 > IRQ1.
Note: *Selecting a reserved mode causes an undefined operation.	

The Interrupt Request Register is defined in Table 23.

Table 23. Interrupt Request Register (IRQ), R250; Read/Write

Bit	7	6	5	4	3	2	1	0
Field	Reserved		IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FAh Bank 0h							
Note: R = Read, W = Write.								

Bit	Description
[7:6]	**Reserved** These bits are reserved and must be programmed to 00.
[5] IRQ5	**Interrupt** IRQ5 = T1 1: Interrupt pending. 0: No interrupt pending.
[4] IRQ4	**Interrupt** IRQ4 = T0 1: Interrupt pending. 0: No interrupt pending.

Bit	Description
[3] IRQ3	**Interrupt** IRQ3 = P32 Input (rising edge) 1: Interrupt pending. 0: No interrupt pending.
[2] IRQ2	**Interrupt** IRQ2 = P31 Input 1: Interrupt pending. 0: No interrupt pending.
[1] IRQ1	**Interrupt** IRQ1 = P33 Input 1: Interrupt pending. 0: No interrupt pending.
[0] IRQ0	**Interrupt** IRQ0 = P32 Input (falling edge) 1: Interrupt pending. 0: No interrupt pending.

The Interrupt Mask Register is defined in Table 24.

Table 24. Interrupt Mask Register (IMR), R251; Read/Write

Bit	7	6	5	4	3	2	1	0
Field	MIE	Reserved	IRQ0–IRQ5					
RESET	0	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FBh Bank 0h							

Note: R = Read, W = Write, X = Indeterminate.

Bit	Description
[7] MIE	**Master Interrupt Enable** 1: Enables global interrupts.
[6]	**Reserved** This bit is reserved and must be programmed to 0.
[5:0] IRQ*x*	**IRQ0–IRQ5** 1: Enables IRQ0–IRQ5 (D0 = IRQ0).

Note: *x* indicates bits in the range 5–0.

General Control Registers

The Flags Register is defined in Table 25.

Table 25. Flag Register (Flags), R252; Read/Write

Bit	7	6	5	4	3	2	1	0
Field	CARRY	ZERO	SIGN	OVRFLW	DECIMAL ADJUST	HALF CARRY	FLAG2	FLAG1
RESET	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FCh Bank 0h							

Note: R = Read, W = Write, X = Indeterminate.

Bit	Description
[7] CARRY	**Carry Flag**
[6] ZERO	**Zero Flag**
[5] SIGN	**Sign Flag**
[4] OVRFLW	**Overflow Flag**
[3] DECIMAL ADJUST	**Decimal Adjust Flag**
[2] HALF CARRY	**Half Carry Flag**
[1] FLAG2	**User Flag F2***
[0] FLAG1	**User Flag F1***

Note: *Not affected by RESET.

The Register Pointer Register is defined in Table 26.

Table 26. Register Pointer (RP), R253; Read/Write

Bit	7	6	5	4	3	2	1	0
Field	WRP				Reserved			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDh Bank 0h							
Note: R = Read, W = Write.								

Bit	Description
[7:4] WRP	**Working Register Pointer**
[3:0]	**Reserved** These bits are reserved and must be programmed to 0000.

The General Purpose Register is defined in Table 27.

Table 27. General Purpose Register (GPR), R254; Read/Write

Bit	7	6	5	4	3	2	1	0
Field	GPR							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FEh Bank 0h							
Note: R = Read, W = Write, X = Indeterminate.								

Bit	Description
[7:0] GPR	**General Purpose Register**

The Stack Pointer Low Register is defined in Table 28.

Table 28. Stack Pointer Low (SPL), R255; Read/Write

Bit	7	6	5	4	3	2	1	0
Field	SPL							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FFh Bank 0h							

Note: R = Read, W = Write.

Bit	Description
[7:0] SPL	**Stack Pointer Lower Byte** SP0–SP7.

Ordering Information

Order the Z86C08 High Temperature MCU from Zilog using the part numbers listed in Table 29. For more information about ordering, please consult your local Zilog sales office. The Zilog website lists all regional offices and provides additional Z8 MCU product information.

Table 29. Z86C08 High Temperature MCU Ordering Information

Pin Count	Package	Size (KB)	Description
18	DIP	2	Z86C0812PPG
	SOIC	2	Z86C0812SPG
20	SSOP	2	Z86E0812HPG

For fast results, contact your local Zilog Sales offices for assistance in ordering the part(s) required. Contact your local Zilog Sales office by navigating to Sales Office on www.zilog.com.

Part Number Description

Zilog part numbers consist of a number of components. For example, part number Z86C0812PPG is a 12 MHz 18-pin DIP that operates in the –40ºC to +150ºC temperature range, with Plastic Standard Flow. The Z86C0812PPG part number corresponds to the code segments indicated in the following table.

Z	Zilog Prefix
86	Z8 Product
C	ROM Product
08	Product Number
12	Speed (MHz)
P	Dual In-line Processor
P	High Temperature
G	Environmental Flow (No Lead)

Precharacterization Product

The products represented by this document are newly introduced; hence Zilog has not completed a full characterization of the product. This document states what Zilog knows about this product at this time; however, additional features or nonconformance with some aspects of this document may be found, either by Zilog or its customers, in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Application Precautions

Users should be aware of the following issues when developing with the Z86C08 High Temperature MCU.

- The Z86CCP0xZEM emulator does not support 32 kHz operation.
- The WDT only runs in Stop Mode if the permanent WDT option is selected.
- The %FE (GPR) and %FF (SPL) registers are reset to 00h after a stop-mode recovery or any reset.
- After enabling Analog Mode, a period of two NOPs must occur before the analog comparator outputs are valid.
- When switching from Digital Mode to Analog Mode, interrupts must be disabled, the analog comparator must be enabled, and IRQ3 to IRQ0 must be cleared.

Customer Support

To share comments, get your technical questions answered, or report issues you may be experiencing with our products, please visit Zilog's Technical Support page at http://support.zilog.com.

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