Application Note

Migration from Z8 Encore! XP® F082A Series to Z8 Encore!® F0830 Series

AN024204-0508

Abstract

This application note highlights the differences between Zilog's Z8 Encore! XP® F082A Series and Z8 Encore!® F0830 Series, and reviews the key features when migrating an application/design from Z8 Encore! XP F082A Series to Z8 Encore! F0830 Series. It also mentions silicon differences between Z8 Encore! XP F082A Series and Z8 Encore! F0830 Series from block-level perspective and, software and register-level perspective.

In addition, it also gives an example application along with snippets of source code for accomplishing the analog-to-digital converter (ADC) functionality in Z8 Encore! F0830.

Note: *The source code file associated with this application note,* `AN0242-SC01.zip`*, is available for download on* www.zilog.com.

Z8 Encore!® F0830 Series Overview

Z8 Encore! family of products are the first in line of Zilog® microcontroller products, based on the 8-bit eZ8™ CPU. Z8 Encore! F0830 series expand on Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows the faster development time and program changes in the field (customer applications). The new eZ8 CPU is upward compatible with existing Z8® CPU instructions. The rich peripheral set of Z8 Encore! F0830 series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

Features

The key features of Z8 Encore! F0830 series include:

- 20 MHz eZ8 CPU
- Up to 12 KB Flash memory with in-circuit programming capability
- 256 B register RAM
- 64 B non-volatile data storage (NVDS)
- Up to 25 I/O pins
- Internal precision oscillator with accuracy of +/-4% full voltage/temperature range
- External crystal oscillator
- Two enhanced 16-bit timers with capture, compare, and pulse-width modulation (PWM) capability
- Watchdog Timer (WDT) with dedicated internal RC oscillator
- On-chip debugger (OCD)
- Optional eight channel, 10-bit ADC
- On-chip analog comparator
- Eighteen vectored interrupts
- Voltage Brownout (VBO) protection
- Power-On Reset (POR)
- 2.7 V–3.6 V operating voltage
- Thirteen 5 V tolerant input pins
- 20- and 28-pin packages
- 0 °C to +70 °C standard temperature ranges and -40 °C to +105 °C extended operating temperature ranges

Discussion

Figure 1 displays an overview of the modules that are different between Z8 Encore! XP® F082A Series and Z8 Encore!® F0830 Series. The changes occur in the following blocks:

Removed Blocks

Modules in this category are removed. Application designs are impacted by this feature (that is, if the application uses the removed blocks, then the application has to be re-written, otherwise it does not work).

Modified and Enhanced

Modules in this category contain some modified and/or enhanced features. Application designs are impacted by this feature.

No Change

Modules in this category contain identical features, and are functionally compatible and the application design is not impacted.

Blocks Different

Modules in this category contain a new implementation of the block, and are not functionally compatible. The application design is impacted.

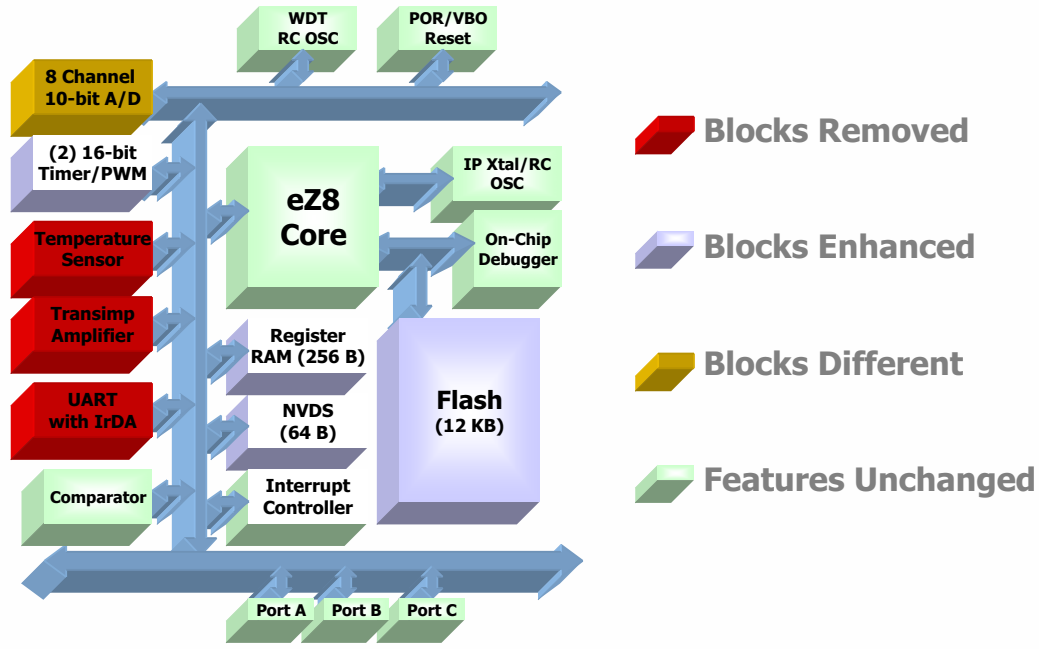

Figure 1. Z8 Encore!® F0830 Series Block Diagram

Table 1 summarizes the feature differences and impact in the existing design/application note when migrating from Z8 Encore! XP F082A Series to Z8 Encore! F0830 Series.

Table 1. Feature Differences Between Z8 Encore! XP® F082A Series and Z8 Encore!® F0830 Series

Feature	Z8 Encore! F0830 Series	Z8 Encore! XP F082A Series	Difference	Description	Existing Design Impact
eZ8 CPU			No change	20 MHz operation	No impact
GPIO	Up to 25 I/O	Up to 25 I/O	No change	No change	No impact
Interrupts	Up to 18	Up to 18	No change	No change	No impact
Pin Compatibility			No change except for signals of blocks removed	Pin-to-pin compatible	No impact
Assembly compatibility			No change	Assembly code compatible	No impact
Packaging	PDIP, QFN, SOIC, SSOP	PDIP, SSOP, SOIC		20- and 28-pin packages	
PWM	Fast shutdown	Regular PWM	Modified and/or enhanced	In PWM single/dual mode, the comparator output can disable the timer	No impact
Comparator			No change		No impact
Flash	Up to 12 KB	Up to 8 KB	Modified and/or enhanced	More Flash for application code	No impact
RAM	Up to 256 B	Up to 1 KB	Modified and/or enhanced	Less RAM space, 256 B	Yes, need to use variables that are able to fit in 256 B
NVDS	64 B	0 to 128 B	Modified and/or enhanced	Non-Volatile Data Storage	No impact
ADC	Successive Approximation Register (SAR)	Sigma-Delta	Different	A fast ADC with a conversion time of 11.9 µs	Rewrite the software for ADC
UART	No	Up to 1	Removed	UART has been removed	

Table 1. Feature Differences Between Z8 Encore! XP® F082A Series and Z8 Encore!® F0830 Series (Continued)

Temperature sensor	No	Yes	Removed	Temperature sensor has been removed
TIA	No	Yes	Removed	Transimpedance amplifier is removed

Modifications and Migration from Z8 Encore! XP® F082A Series to Z8 Encore! F0830 Series

This section describes the features that are different/enhanced/modified and changes to be done in the software while migrating from Z8 Encore! XP F082A Series to Z8 Encore! F0830 Series.

Table 2 describes a top level view of peripheral initialization and usage from software perspective.

Table 2. Top Level View of Peripheral Initialization and Usage

Peripheral Initialization and Usage	Software Initialization	Usage
GPIO	Same	Same
Flash	Same	Same
IPO	Same	Same
Comparator	Same	Same
ADC	Different (see, Dual Fan Controller Implementation on page 7)	Different
Timer	Same	Enhanced

Table 3 lists the Register/Flash option bit differences between Z8 Encore! XP F082A Series to Z8 Encore! F0830 series.

Table 3. Register/Flash Option Bit Differences Between Z8 Encore! XP® F082A Series and Z8 Encore! F0830 Series

	Z8 Encore! F0830 Series	Z8 Encore! XP F082A Series	Difference	Description	Design Impact
General Purpose RAM	000-0FF	000-3FF	Modified and/or Enhanced	Less RAM space, 256 B	Less RAM. Tighten the variable space
Special Function Registers					
Peripheral registers except ADC	Same		Same	None of the peripheral registers, other than ADC definitions has changed	No impact
ADC registers	Totally Different		Different	ADC now uses a Successive Approximation Register ADC. Refer to *Z8 Encore!® F0830 Series Product Specification (PS0251)*	Use the new ADC register definitions
Flash Option Bits					
Overdrive motor control protect	Yes	No	New	This bit helps in the comparator trigger shutdown of the PWM timers	No impact

Fast PWM Shutdown

This is a new feature and does not affect when an existing Z8 Encore! XP F082A series application is migrated to Z8 Encore! F0830 series.

In PWM single/dual mode, the comparator output can disable the timer. To use this feature, set the OCMP bit in the Flash information area.

Successive Approximation Analog-to-Digital Converter

When migrating from Z8 Encore! XP F082A Series to Z8 Encore! F0830 Series, all the peripherals are same except ADC. Z8 Encore! F0830 includes an eight channel SAR ADC. The ADC converts an analog input signal to a 10-bit binary number.

The features of SAR ADC include:

- Eight analog input sources multiplexed with general purpose I/O ports
- Fast conversion time, less than 11.9 µs
- Programmable timing controls
- Internal voltage reference generator

Rewrite the ADC software block when migrating from Z8 Encore! XP F082A Series to Z8 Encore! F0830 Series

Analog-to-Digital Converter Initialization Code

The sample code to initialize the SAR ADC for Analog Channel "1" is shown below.

```
////////////////////////////////////////////////////
// Initialize ADC for Analog Ch "1"
////////////////////////////////////////////////////

void init_adc(void)
{
     PBAF= 0x02;                    //0000 0010b PB1
     PBAFS1 |= 0x02;                //Select Alternate Function for Port
                                    //B1
                                    //(ANA1)

     PBAF       = 0x20;             //0010 0000b PB5
     PBAFS1 |= 0x20;                //Select Alternate Function for Port
                                    //B5 (Vref)

     ADCCTL0 = 0x31;                //0011 0001
                                    //Bit 5 = 1 Internal reference
                                    //voltage for ADC is Enabled
                                    //Bit 4 = 1 ADC is Enabled for normal
                                    //use
                                    //Bit [2:0] = 001 Conversion on ANA1
     ADCSST = 0x0F ;                //Sample Settling Time Register
     ADCST = 0x7F;                  //Sample Hold Time

}
```

Sample Code to Read ADC

Once the ADC channel is initialized, the sample code to read the initialized channel, is as shown below.

```
{
     ADCCTL0 |= 0x80;               //Start conversion

     while ( (ADCCTL0 & 0x80) == 0x80);
                                    //Wait until conversion is done

     ADC_CH1 = ADCD_H;              //Read in Speed Command
}
```

To switch between channels, modify the ADC control register least three significant bits to reflect the channel that needs to be sampled. For example, if channel '3' needs to be read, followed by channel '6', see the sample code below.

```
{
      ADCCTL0 &= 0xF8;
      ADCCTL0  |=  0x03;              //Assign channel-3
      ADCCTL0 |= 0x80;                //Start conversion

      while ( (ADCCTL0 & 0x80) == 0x80);
                                      //Wait until conversion is
                                      //done

      ADC_CH3 = ADCD_H;               //Read in Speed Command

      ADCCTL0 &= 0xF8;
      ADCCTL0  |=  0x06;              //Assign channel-6

      ADCCTL0 |= 0x80;                //Start conversion

      while ( (ADCCTL0 & 0x80) == 0x80);
                                      //Wait until conversion is
                                      //done

      ADC_CH6 = ADCD_H;               //Read in Speed Command
}
```

Dual Fan Controller Implementation

The following I/O configurations are used:

- One PWM output for Fan 1, PWM0 - T0OUT(PA1).
- One PWM output for Fan 2, PWM1 - T1OUT(PA7).
- One Fan Select, PB0.
- One Current Sense Input, Comparator Positive Input, and CINP (PC0).
- One ADC input for speed, ANA1 (PB1).

Tools Used

The 28-pin Z8 Encore!® F0830 series is used with ZDS II v4.9.6 on the Dual Fan Controller board. Fan Controller board with Z8 Encore! F0830 series is used to test the final application.

Testing the Application

Testing of Dual Fan Controller application uses the demo board as per the schematic provided using the 28-pin Z8 Encore! F0830 series and Zilog developers suite for Z8 Encore!—ZDS II v4.9.6.

Some of the settings in the application code are as follows:

- ADC (Channel 1 with Pre-scale = 1, and default values used for Sampling Hold/Settling Time registers).
- Comparator (internal 0.2 V used as negative input for comparator).
- Both PWMs (in single mode) with automatic shutdown.

Automatic shutdown of PWM when the over current/ comparator was tested by setting/enabling the Flash

option bit overdrive motor control protect bit (OMPB) and is working as per the specification.

Summary

This application note highlights the differences between Z8 Encore! XP F082A Series and Z8 Encore! F0830 Series. The code snippets for some of the changed blocks provide an easy migration path. The Dual Fan Controller application with the schematic and the complete source code is provided as a demo to highlight some of the functionality of the Z8 Encore! F0830 series.

References

The documents associated with eZ8 CPU, Z8 Encore! XP®, and Z8 Encore!® F0830 Series available on www.zilog.com are provided below:

- eZ8™ CPU User Manual (UM0128)
- Z8 Encore! XP® F082A Series Product Specification (PS0228)
- Z8 Encore!® F0830 Series Product Specification (PS0251)

Appendix A—Schematics

Figure 2 displays the schematic of Dual Fan Controller.

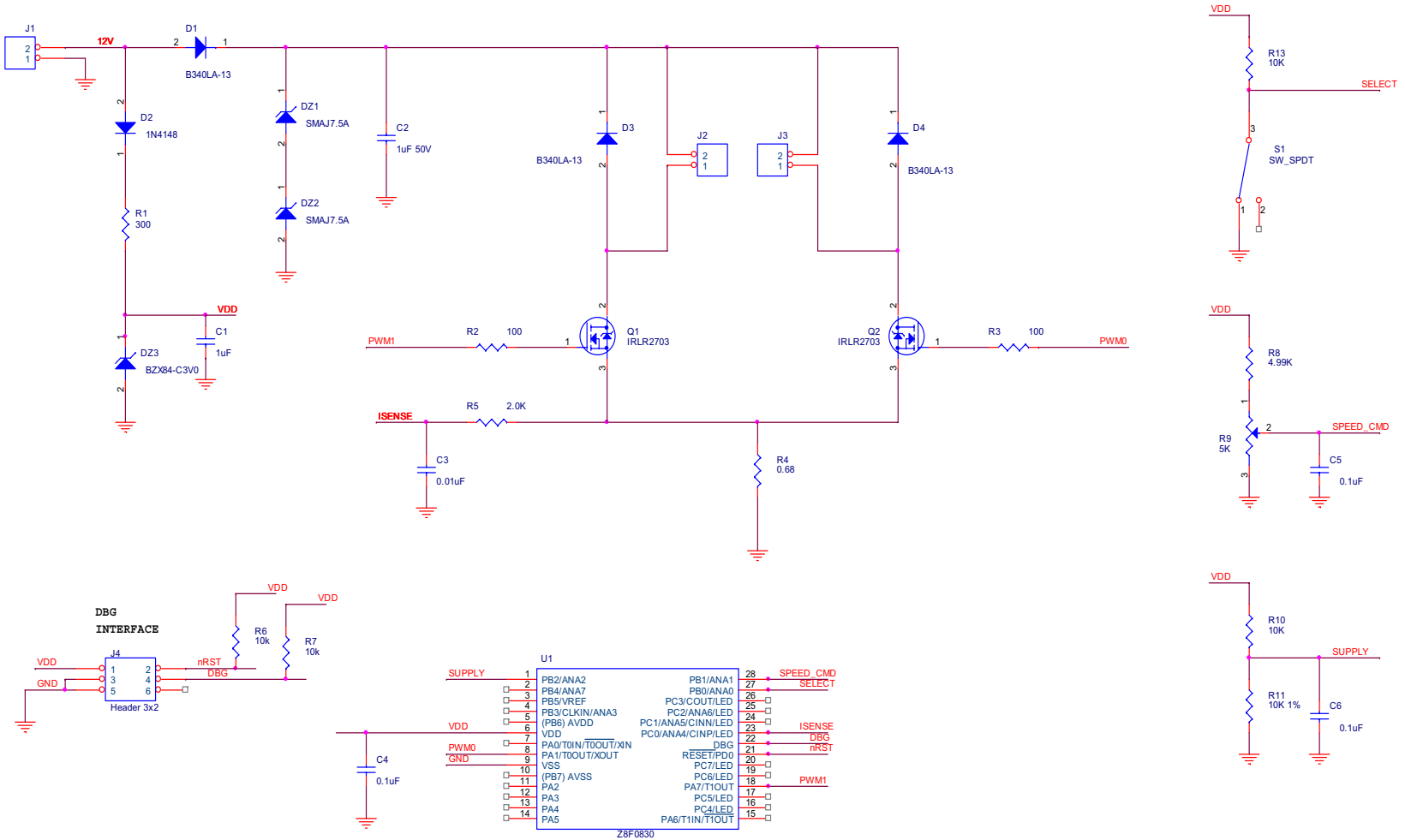

Figure 2. Schematic of Dual Fan Controller

Appendix B—Flowcharts

Figure 3 displays the flowchart for the Dual Fan Controller application code.

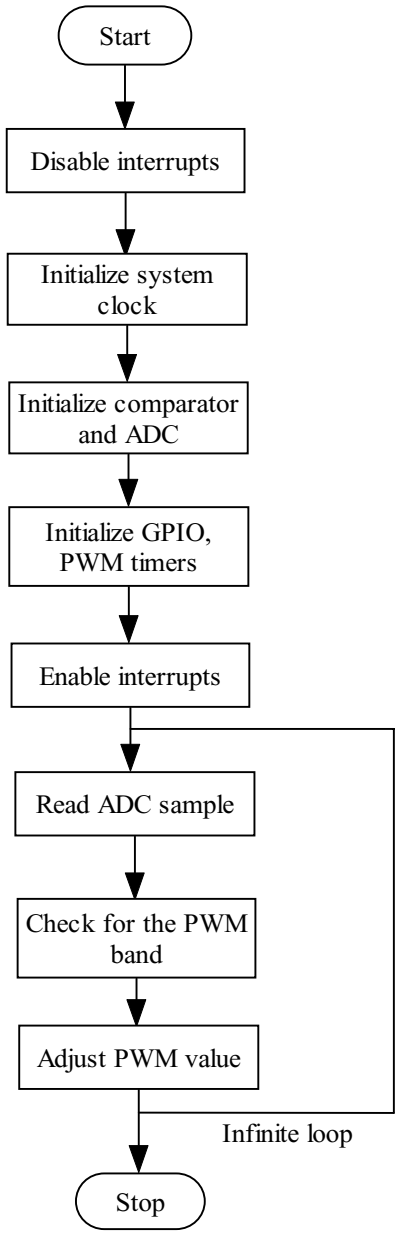

Figure 3. Flowchart for the Dual Fan Controller Application Code

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