Z8 Encore!® Z8F083A Series MCU Programmers Reference Chart

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Program Memory Map

Flash Memory Configurations

Part Number	Flash Size KB (Bytes)	Number of Pages	Program Memory Addresses	Flash Sector Size (bytes)
Z8F083A	8 (8196)	16	0000h-1FFFh	1024
Z8F043A	4 (4096)	4	0000h-0FFFh	512

Program Memory Address (Hex)	Function
0000-0001	Flash Option Bits
0002-0003	Reset Vector
0004-003D	Interrupt Vectors
003E-0FFF	Program Memory (Z8F043A)
003E-1FFF	Program Memory (Z8F083A)

Comparator Registers

Comparator Control Register
(CMPO = F90h)

7		Reserved
6	INNSEL	0 = internal reference disabled, GPIO pin used as negative comparator input 1 = internal reference enabled as negative comparator input
5.2	REFLVL	0000 = 0.0 V 0001 = 0.2 V 0010 = 0.4 V 0011 = 0.6 V 0100 = 0.8 V 0101 = 1.0 V (Default) 0110 = 1.2 V 0111 = 1.4 V 1000 = 1.6 V 1001 = 1.8 V 1010–1111 = Reserved
1.0		Reserved

A/D Converter Registers

ADC Control Register 0
(ADCCT0 = F70h)

7	START	0 = Writing to 0 has no effect. Reading a 0 indicates the ADC is available to begin a conversion. 1 = Writing to 1 starts a conversion. Reading a 1 indicates a conversion is currently in progress.
6		Reserved
5	REFEN	0 = Internal reference voltage is disabled allowing an external reference voltage to be used by the ADC. 1 = Internal reference voltage for the ADC is enabled. The internal reference voltage can be measured on the VREF pin.
4	ADCEN	0 = ADC is disabled for low power operation 1 = ADC is enabled for normal use
3		Reserved
2:0	ANAIN	000 ANA0 input is selected for analog to digital conversion 001 ANA1 input is selected for analog to digital conversion 010 ANA2 input is selected for analog to digital conversion 011 ANA3 input is selected for analog to digital conversion 100 ANA4 input is selected for analog to digital conversion 101 ANA5 input is selected for analog to digital conversion 110 ANA6 input is selected for analog to digital conversion 111 ANA7 input is selected for analog to digital conversion

ADC Data High Byte Register
ADCD_H = F72h

7:0	ADCD_H	00h–FFh The high byte of the last conversion output is held in the data registers until the next ADC conversion has completed

ADC Data Low Bits Register
ADCD_L = F73h

7:6	ADCDL	00–11b These bits are the 2 least significant bits of the 10-bit ADC output. The low bits are latched into this register whenever the ADC Data High Byte Register is read.
5:0		Reserved

ADC Clock Prescale Register
ADCCP = F76h

7:3		Reserved
2	DIV8	0 = Clock is not divided 1 = System Clock is divided by 8 for ADC Clock
1	DIV4	0 = Clock is not divided 1 = System Clock is divided by 4 for ADC Clock
0	DIV2	0 = Clock is not divided 1 = System Clock is divided by 2 for ADC Clock

Sample and Setting Time
ADCSST = F74h

7:4		Reserved
3:0	SST	Sample settling time in number of system clock periods to meet 0.5 μs minimum.

Sample Hold Time
ADCST = F75h

7:6		Reserved - Must be 0
5:0	ST	Sample hold time in number of system clock periods to meet 1μs minimum.

GPIO Registers

Port A through D GPIO Address Registers (Use subregister address)

PAADDR = FD0h

7:0	PAADDR	Port A GPIO Address Register

PBADDR = FD4h

7:0	PBADDR	Port B GPIO Address Register

PCADDR = FD8h

7:0	PCADDR	Port C GPIO Address Register

PDADDR = FDCh

7:0	PDADDR	Port D GPIO Address Register

Port A through D Control Register (Value in this register is loaded in subregister identified by GPIO address register)

PACTL = FD1h

7:0	PACTL	Port A Control Register

PBCTL = FD5h

7:0	PBCTL	Port B Control Register

PCCTL = FD9h

7:0	PCCTL	Port C Control Register

PDCTL = FDDh

7:0	PDCTL	Port D Control Register

Port A through D Input Data Register

PACTL = FD2h

7:0	PINA	Port A Input Data Register

PBCTL = FD6h

7:0	PINB	Port B Input Data Register

PCCTL = FDAh

7:0	PINC	Port C Input Data Register

PDCTL = FDEh

7:0	PIND	Port C Input Data Register

Port A through D Output Data Register

PACTL = FD3h

7:0	POUTA	Port A Output Data Register

PBCTL = FD7h

7:0	POUTB	Port B Output Data Register

PCCTL = FDBh

7:0	POUTC	Port C Output Data Register

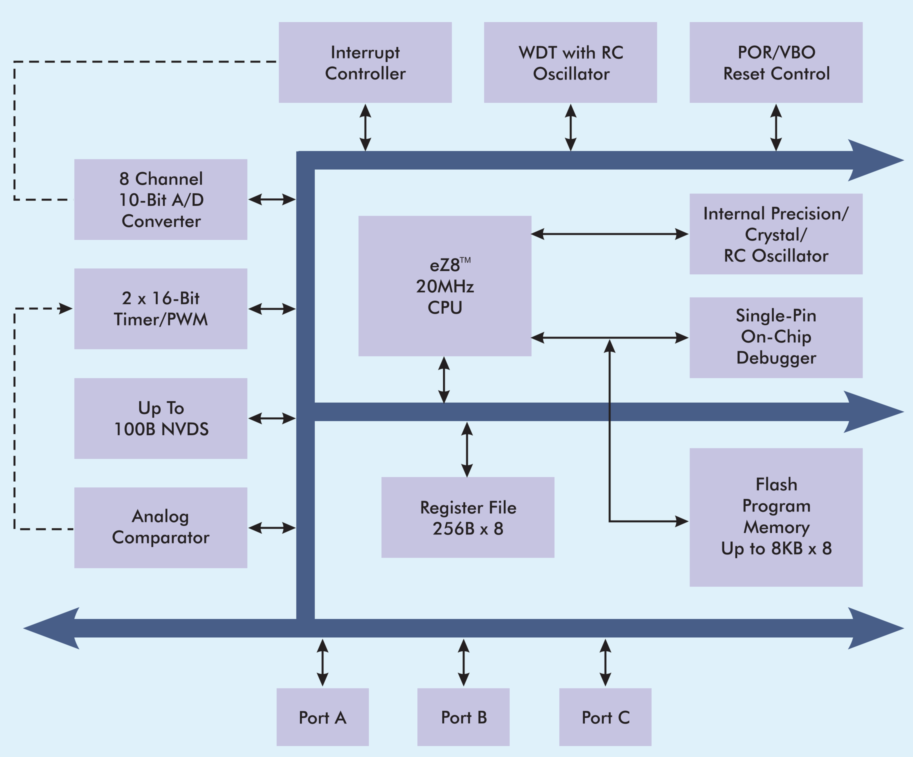
PDCTL = FDFh

7:0	POUTD	Port D Output Data Register

Subregisters by Port Address (used in GPIO Address register)

00h		No Function
01h	PxDD	Data direction. 0=output, 1=input
02h	PxAF0	Alternate Function Set 0. 0=not selected, 1=selected
03h	PxOC	Output Control. 0=drain enabled, 1=open-drain
04h	PxHDE	High Drive Enable. 0=standard drive, 1=high drive
05h	PxSMRE	Stop-Mode Recovery Source. 0=disabled, 1=enabled
06h	PxPUE	Pull-up enable. 0=disabled, 1=enabled
07h	PxAFSI	Alternate Function Set 1. 0=not selected, 1=selected
08h	PxAFS2	Alternate Function Set 2. 0=not selected, 1=selected
09h-FFH		No Function

Functional Block Diagram



General Purpose Timer Registers

Timer 0 1 High Byte Register
TxH = F00h, F08h

7:0	TH	The high byte of the Timer0 count

Timer 0 Low Byte Register
TxL = F01h, F09h

7:0	TL	The low byte of the Timer0 count

Timer 0 1 Reload High Byte Register
TxRH = F02h, F0Ah

7:0	TRH	The high byte of the reload value for Timer0

Timer 0 1 Control 0 Register
TxCTL0 = F06h, F0Eh

7	TMODEHI	Used with TMODE field in TxCTL1
6:5	TICONFIG	0x = Timer interrupt occurs on all the defined reload, compare and input events 10 = Timer interrupt occurs only on defined input capture deassertion events 11 = Timer interrupt occurs on defined reload/ compare events
4		Reserved
3:1	PWMD	000 = No delay 001 = 2 cycles delay 010 = 4 cycles delay 011 = 8 cycles delay 100 = 16 cycles delay 101 = 32 cycles delay 110 = 64 cycles delay 111 = 128 cycles delay
0	INPCAP	0 = Previous timer interrupt is not a result of a timer input capture event 1 = Previous timer interrupt is a result of a timer input capture event

Timer 0 1 Reload Low Byte Register
TxRL = F03h, F0Bh

7:0	TRL	The low byte of the reload value for Timer0

Timer 0 1 PWH High Byte Register
TxPWMH = F04h, F0Ch

7:0	PWMH	The high byte of the PWM compare value of Timer0

Timer 0 1 PWH Low Byte Register
TxPWML = F05h, F0Dh

7:0	PWMH	The low byte of the PWM compare value of Timer0

Timer 0 1 Control 1 Register
TxCTL1 = F07h, F0Fh

7	TEN	0 = Timer is disabled 1 = Timer enabled
6	TPOL	Timer Input/Output Polarity
5:3	PRES	000 = Divide by 1 001 = Divide by 2 010 = Divide by 4 011 = Divide by 8 100 = Divide by 16 101 = Divide by 32 110 = Divide by 64 111 = Divide by 128
3:1	PWMD	Use with TMODEHI in previous register to define mode. 0000 = ONE-SHOT mode 0001 = CONTINUOUS mode 0010 = COUNTER mode 0011 = PWM SINGLE OUTPUT mode 0100 = CAPTURE mode 0101 = COMPARE mode 0110 = GATED mode 0111 = CAPTURE/COMPARE mode 1000 = PWM DUAL OUTPUT mode 1001 = CAPTURE RESTART mode 1010 = COMPARATOR COUNTER mode 111 = 128 cycles delay

Interrupt Controller Registers

Reset, System Exception, and Interrupt Vectors in Order of Priority

Priority	Program Memory Vector Base Address	Interrupt or Trap Source
	Reset and System Exceptions	
	0002h	Reset
	0004h	Watch-Dog Timer
	003AH	Primary Oscillator Fail Trap
	003CH	Watch-Dog Timer Oscillator Fail Trap
	0006h	Illegal Instruction Trap (not an interrupt)
	Interrupts (maskable)	
Highest	0008H	Reserved
	000AH	Timer 1
	000CH	Timer 0
	000EH	Reserved
	0010H	Reserved
	0012H	Reserved
	0014H	Reserved
	0016H	ADC
	0018H	Port A7, selectable rising or falling input edge
	001AH	Port A6, selectable rising or falling input edge or Comparator Output
	001CH	Port A5, selectable rising or falling input edge
	001EH	Port A4, selectable rising or falling input edge
	0020H	Port A3, selectable rising or falling input edge
	0022H	Port A2, selectable rising or falling input edge
	0024H	Port A1, selectable rising or falling input edge
	0026H	Port A0, selectable rising or falling input edge
	0028H	Reserved
	002AH	Reserved
	002CH	Reserved
	002EH	Reserved
	0030H	Port C3, both input edges
	0032H	Port C2, both input edges
	0034H	Port C1, both input edges
	0036H	Port C0, both input edges
	0038H	Reserved

Interrupt Request 0 Register
IRQ0 = FC0h

7		Reserved
6	T11	0 = No interrupt request is pending for Timer1 1 = Interrupt request from Timer0 is awaiting service
5	T01	0 = No interrupt request is pending for Timer0 1 = Interrupt request from Timer0 is awaiting service
4:1		Reserved
0	ADC	0 = No interrupt request is pending for analog - digital converter 1 = Interrupt request from analog - digital converter is awaiting service

Interrupt Request 1 Register
IRQ1 = FC3h

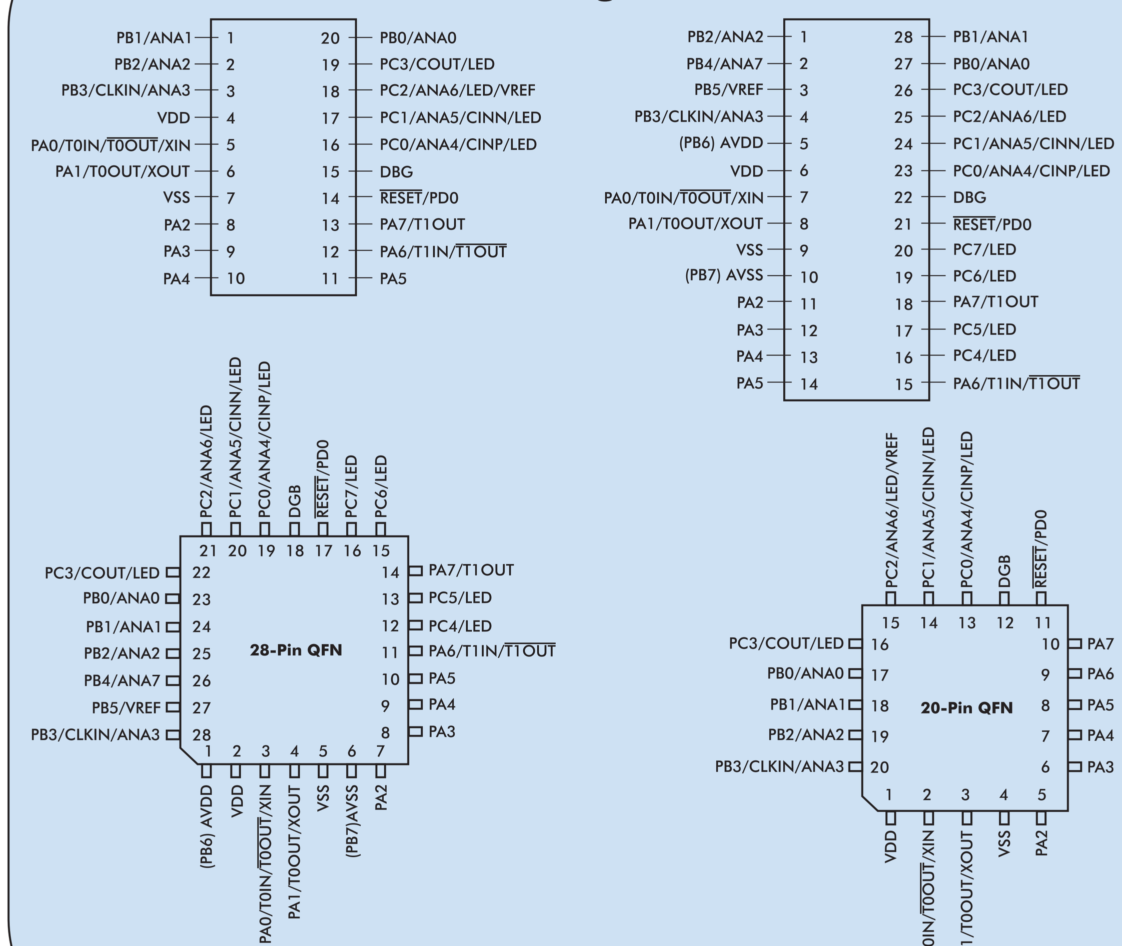
7	PA71	0 = No interrupt request is pending for GPIO port A. 1 = An interrupt request from GPIO port A.
6	PA6CI	0 = No interrupt request is pending for GPIO port A or comparator. 1 = An interrupt request from GPIO port A or comparator.
5	PA5I	0 = No interrupt request is pending for GPIO port A pin 5. 1 = An interrupt request from GPIO port A pin 5 is awaiting service.
4	PA4I	0 = No interrupt request is pending for GPIO port A pin 4. 1 = An interrupt request from GPIO port A pin 4 is awaiting service.
3	PA3I	0 = No interrupt request is pending for GPIO port A pin 3. 1 = An interrupt request from GPIO port A pin 3 is awaiting service.
2	PA2I	0 = No interrupt request is pending for GPIO port A pin2. 1 = An interrupt request from GPIO port A pin 2 is awaiting service.
1	PA1I	0 = No interrupt request is pending for GPIO port A pin 1. 1 = An interrupt request from GPIO port A pin 1 is awaiting service.
0	PA0I	0 = No interrupt request is pending for GPIO port A pin 0. 1 = An interrupt request from GPIO port A pin 0 is awaiting service.

Interrupt Request 2 Register
IRQ0 = FC6h

7:4		Reserved
3	PC3I	0 = No interrupt request is pending for GPIO port C pin 3. 1 = An interrupt request from GPIO port C pin 3 is awaiting service.
2	PC2I	0 = No interrupt request is pending for GPIO port C pin2. 1 = An interrupt request from GPIO port C pin 2 is awaiting service.
1	PC1I	0 = No interrupt request is pending for GPIO port C pin 1. 1 = An interrupt request from GPIO port C pin 1 is awaiting service.
0	PC0I	0 = No interrupt request is pending for GPIO port C pin 0. 1 = An interrupt request from GPIO port C pin 0 is awaiting service.

LEGEND Read/Write | Read Only | Reserved

Pin Diagram



Note: SOIC, PDIP, SSOP, and QFN packaging available

Pin Signal Descriptions

Signal Mnemonic	I/O	Descriptions
General Purpose	**I/O**	**Ports A-D**
PA[7:0]	I/O	Port A. General purpose I/O.
PB[7:0]	I/O	Port B. General purpose I/O.
PC[7:0]	I/O	Port C. General purpose I/O.
PD[0]	O	Port D. General purpose output only.
Timers		
T0OUT/T1OUT	O	Timer output 0-1.
$\overline{\text{T0OUT/T1OUT}}$	O	Timer complement output 0-1.
T0IN/T1IN	I	Timer input 0-1.
Comparator		
CINP/CINN	I	Comparator input.
COUT	O	Comparator output.
Anlog		
ANA[7:0]	I	Analog port. Input to ADC.
VREF	I/O	ADC reference voltage input.
Oscillators		
XIN	I	External crystal input.
XOUT	O	External crystal output.
Clock Input		
CLKIN	I	Clock input.
LED Drivers		
LED	O	Direct LED drive.
On-Chip Debugger		
DBG	I/O	Debug.
Reset		
RESET	I/O	Reset.
Power Supply		
V_{DD}	I	Digital power supply.
AV_{DD}	I	Analog power supply.
V_{SS}	I	Digital ground.
AV_{SS}	I	Analog ground.

The bar above indicates inverted or complemented signal

First Op Code Map

Lower Nibble (Hex) / Upper Nibble (Hex)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	1.1 BRK	2.2 SRP IM	2.3 ADD r1,r2	2.4 ADD r1,Ir2	3.3 ADD R2,R1	3.4 ADD IR2,R1	3.3 ADD R1,IM	3.4 ADD IR1,IM	4.3 ADDX ER2,ER1	4.3 ADDX IM,ER1	2.3 DJNZ r1,x	2.2 JR cc,x	2.2 LD r1,IM	3.2 JP cc,DA	1.2 INC r1	1.2 NOP
1	2.2 RCL R1	2.3 RCL Ir1	2.3 ADC r1,r2	2.4 ADC r1,Ir2	3.3 ADC R2,R1	3.4 ADC IR2,R1	3.3 ADC R1,IM	3.4 ADC IR1,IM	4.3 ADCX ER2,ER1	4.3 ADCX IM,ER1						See 2nd Opcode Map
2	2.2 INC R1	2.3 INC IR1	2.3 SUB r1,r2	2.4 SUB r1,Ir2	3.3 SUB R2,R1	3.4 SUB IR2,R1	3.3 SUB R1,IM	3.4 SUB IR1,IM	4.3 SUBX ER2,ER1	4.3 SUBX IM,ER1						1
3	2.2 DEC R1	2.3 DEC IR1	2.3 SBC r1,r2	2.4 SBC r1,Ir2	3.3 SBC R2,R1	3.4 SBC IR2,R1	3.3 SBC R1,IM	3.4 SBC IR1,IM	4.3 SBCX ER2,ER1	4.3 SBCX IM,ER1						
4	2.2 DA R1	2.3 DA IR1	2.3 OR r1,r2	2.4 OR r1,Ir2	3.3 OR R2,R1	3.4 OR IR2,R1	3.3 OR R1,IM	3.4 OR IR1,IM	4.3 ORX ER2,ER1	4.3 ORX IM,ER1						
5	2.2 POP R1	2.3 POP IR1	2.3 AND r1,r2	2.4 AND r1,Ir2	3.3 AND R2,R1	3.4 AND IR2,R1	3.3 AND R1,IM	3.4 AND IR1,IM	4.3 ANDX ER2,ER1	4.3 ANDX IM,ER1						1.2 WDT
6	2.2 COM R1	2.3 COM IR1	2.3 TCM r1,r2	2.4 TCM r1,Ir2	3.3 TCM R2,R1	3.4 TCM IR2,R1	3.3 TCM R1,IM	3.4 TCM IR1,IM	4.3 TCMX ER2,ER1	4.3 TCMX IM,ER1						1.2 STOP
7	2.2 PUSH R2	2.3 PUSH Ir2	2.3 TM r1,r2	2.4 TM r1,Ir2	3.3 TM R2,R1	3.4 TM IR2,R1	3.3 TM R1,IM	3.4 TM IR1,IM	4.3 TMX ER2,ER1	4.3 TMX IM,ER1						1.2 HALT
8	2.5 DECW RR1	2.5 DECW IRR1	2.5 LDE r1,Irr2	2.9 LDEI Ir1,Irr2	3.2 LDX r1,ER2	3.3 LDX Ir1,ER2	3.4 LDX IRR2,R1	3.5 LDX IRR2,IR1	3.4 LDX r1,rr2,x	3.4 LDX rr1,r2,x						1.2 DI
9	2.2 RL R1	2.3 RL IR1	2.5 LDE r2,Irr1	2.9 LDEI Ir2,Irr1	3.2 LDX r2,ER1	3.3 LDX Ir2,ER1	3.4 LDX R2,IRR1	3.5 LDX IR2,IRR1	3.3 LEA r1,r2,x	3.5 LEA rr1,rr2,x						1.2 EI
A	2.5 INCW RR1	2.5 INCW IRR1	2.3 CP r1,r2	2.4 CP r1,Ir2	3.3 CP R2,R1	3.4 CP IR2,R1	3.3 CP R1,IM	3.4 CP IR1,IM	4.3 CPX ER1,ER1	4.3 CPX IM,ER1						1.4 RET
B	2.2 CLR R1	2.3 CLR IR1	2.3 XOR r1,r2	2.4 XOR r1,Ir2	3.3 XOR R2,R1	3.4 XOR IR2,R1	3.3 XOR R1,IM	3.4 XOR IR1,IM	4.3 XORX ER2,ER1	4.3 XORX IM,ER1						1.5 IRET
C	2.2 RRC R1	2.3 RRC IR1	2.3 LDC r1,Irr2	2.4 LDC1 r1,Irr2	3.3 JP IR,R1	3.4 LDC Ir1,Irr2		3.4 LD R1,r2,x	4.3 PUSHX ER2							1.2 RCF
D	2.2 SRA R1	2.3 SRA IR1	2.5 LDC r2,Irr1	2.9 LDC1 Ir2,Irr1	2.6 CALL IR,R1	2.2 BSWAP R1	3.3 CALL DA	3.4 LD r2,r1,x	3.2 POPX ER1							1.2 SCF
E	2.2 RR R1	2.3 RR IR1	2.2 BIT p,b,r1	2.3 LD r1,Ir2	3.2 LD R2,R1	3.3 LD IR2,R1	3.2 LD R1,IM	3.3 LD IR1,IM	4.2 LDX ER1,ER1	4.2 LDX IM,ER1						1.2 CCF
F	2.2 SWAP R1	2.3 SWAP IR1	2.5 TRAP Vector	2.3 LD Ir1,r2	2.8 MULT RR1	3.3 LD R2,IR1	3.3 BTJ p,b,r1,x	3.4 BTJ p,b,Ir1,x								

Refer to the Product Specification for the 2nd Op Code Map

Watch-Dog Timer Registers

Watch-Dog Timer Reload Upper Byte Register
(WDTU = FF1h)

7:0	WDTH	00h to FFh = The WDT Reload High Byte is the most significant byte, or bits [23:16] of the 24-bit WDT reload value

Watch-Dog Timer Reload High Byte Register
(WDTH = FF2h)

7:0	WDTH	00h to FFh = The WDT Reload High Byte is the middle byte, or bits [15:8] of the 24-bit WDT reload value

Watch-Dog Timer Reload Low Byte Register
(WDTL = FF3h)

7:0	WDTL	00h to FFh = The WDT Reload Low Byte is the least significant byte, or bits [7:0] of the 24-bit WDT reload value

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