March 9, 1998

Dear Customer:

ZiLOG is pleased to advise that Z80182 Revision G has been upgraded to Revision K. Revision K is the enhanced version of the Z80182 Revision G currently being shipped in high volumes, and Revision K is completely compatible with Revision G. The following lists the changes made to the Z80182 Revision K device which distinguish it from the Z80182 Revision G device.

Table 1. Z80182 Revision K Features and Benefits

Features	Benefits
Enhanced UARTs	Up to 512Kbps @ 33MHz
Chain-Linked DMA channels	Less CPU Intervention
X2 Clock Multiplier Mode	Uses Slower, Less Expensive Crystals
Increased MIMIC Output Drive	Eliminates the need for ’245 drivers
Improved Memory Access Timings	Uses Slower, Less Expensive Memories
Revision Identification Register	Identifies Z182 Device Revision
$\overline{\text{INT0}}$ Assertion on MIMIC Access	Allows MIMIC Access to Wake Z182
Fixed ROM/RAM Chip Select Boundaries	Uses Slower, Less Expensive Memories
Low Noise Crystal Option	Reduces Oscillator Drive to 30%
PHI Output Disable	Reduces EMI
Low Voltage Support	3.3V @ 20MHz for Portable Apps
Extended Temperature Operation	Nonstandard Temperature Apps

Revision K samples are now available. Please contact the ZiLOG account representative in your area if you wish to receive samples for qualification. If you do not request samples for qualification, we will assume that production shipments of Z80182K can begin on 5-4-98 without sample evaluation.

Attachments 1 through 4 of this letter contain the following information concerning Z80182 Revision K: (1) Upgrade Notes, (2) Z80182 Rev. K Enhancements, (3) Z80182 Errata Comparison of Rev. H vs. Rev. K, and (4) Z80182 Device Errata Descriptions. If you have any questions concerning this material, please contact your local area representative.

Sincerely,

Alice Baluni
Vice President
Reliability & Quality Assurance

AB:ge:DC98-000001
Attachments (4)

Attachment 1

Upgrade Notes

The Z182K adds more value to Z182 designs. The Rev. K contains an enhanced Z8S180 MPU linked with a dual channel ESCC, a 16550 MIMIC, and 24 bits of parallel I/O. Improvements have been made to the S180 core and the 16550 MIMIC, while the ESCC remains unchanged from that of the existing Z182. In addition, there have been a number of errata fixed (detailed in attached document), which functionally correct errata encountered in using previous Z182 devices (Revision G and prior).

The Z80182K also fixes some issues that were present in the Z80180H silicon, which was sampled but did not reach volume production. Some customers that received Z182H samples in Q3 1996 noted problems with the programmable reload timer, among others, which is resolved with Z182K.

With the exceptions outlined in the errata, Z80182 Rev. K remains backward compatible with the current Z80182 Rev. G as the enhancements (software selectable) default back to the current Z80182 Rev. G state.

The Z182 Rev. K is processed in ZiLOG's 8" Mod III silicon fab in the Z6120 0.65 micron process.

Attachment 2

1. Enhanced UARTs (up to 512Kbps @ 33MHz)

   The two UART channels in the S180 have been enhanced from the current S180 core. The addition of a 16-bit down counter that divides the processor clock by the value in a 16-bit time constant register (identical to the BRG in the SC /ESCC) allows for programmability of up to 512Kbps @ 33 MHz. In addition, a 4-byte Receive FIFO has been added to buffer incoming data and reduce the chance of overrun errors.

2. Chain-Linked DMA Channels

   The two DMA channels in the S180 now have the capability to link both DMA channels to allow for non-stop DMA data transfer when the DMAs are programmed to take their request from the same peripheral device. This provides increased system performance while requiring less CPU intervention.

3. X2 Clock Multiplier Mode

   This feature, when enabled, doubles the internal clock from that of the external clock effectively for a crystal frequency range or 10-16MHz. This allows for the use of less expensive crystals resulting in a systems level cost savings.

   Note that if an oscillator is used in powerdown modes such as standby, it will consume power (the spec for the oscillator is “input current”). Instead of using an oscillator, a crystal with the X2 clock feature can be used. The crystal will not consumer any power, therefore, providing power savings.

4. Increased 16550 MIMIC Output Drive Capability

   The MIMIC in the Z182 Rev. K has increased MIMIC output drive capability to 16mA eliminating the need for an external ’245 transceiver.

5. Improved Memory Access Timings

   The memory access timing specs:Spec#8+Spec#15+Spec#71 have been reduced to allow for the use of slower memories, providing additional system cost savings. The target spec for the memory access time for the Z182K is 18ns. Previously for standard Z182 devices, the memory access time was 35ns.

   Z182 ROM memory Access Time Formula

   tacc (0 WS) = 1.5 (tcy) - T8 - T71 -T15

   tacc (1 WS) = 2.5 (tcy) - T8 - T71 -T15

   tacc (2 WS) = 3.5 (tcy) - T8 - T71 -T15

   tacc (3 WS) = 4.5 (tcy) - T8 - T71 -T15

Z182 RAM memory Access Time Formula

tacc (0 WS) = 2 (tcy) - T8 - T71 -T15

tacc (1 WS) = 3 (tcy) - T8 - T71 -T15

tacc (2 WS) = 4 (tcy) - T8 - T71 -T15

tacc (3 WS) = 5 (tcy) - T8 - T71 -T15

where:

	tcy	Spec#1	Clock Cycle Time
T8	tMED1	Spec#8	Clock Fail to $\overline{\text{MREQ}}$ Fall Delay
T15	TDRS	Spec#15	Data Read Setup Time
T71	TdCS	Spec#71	$\overline{\text{MREQ}}$ Valid to $\overline{\text{ROMCS}}$, $\overline{\text{RAMCS}}$ Valid Delay

6. Revision identification Register

   A revision identification register has been included in the 182K to allow for software differentiation (if needed) between Z80182 devices and previous revisions. This register was a feature not included in Z182 revisions prior to revision G. When the value in register oxDA is ox9F, the chip in question is a revision K.

7. $\overline{\text{INT0}}$ Assertion on MIMIC Access

   When the $\overline{\text{INT0}}$ Assertion on MIMIC Access bit is enabled, and the $\overline{\text{HALT}}$ is active (powerdown in effect), any Host access to the MIMIC will cause a low edge on $\overline{\text{INT0}}$. Since this interrupt source has no vector, INT MODE1 must be used when enabling this mode. This mode is disabled on powerup. $\overline{\text{INT0}}$ Assertion is released when $\overline{\text{HALT}}$ is deasserted.

8. Fixed ROM & RAM Chip Select Boundaries

   In addition to reducing the memory access timings for Spec#8+Spec#15+Spec#71, there is also an additional feature in the Z182K which improves the memory access timing requirements. With the Forced ROM & RAM Memory Boundaries feature, ROMCS will be asserted from00000H-7FFFFH. RAMCS will be asserted from 800000H-FFFFFH. The improved memory access time equation is:

   ACCESS time < (2+WS)*Clock Period-tAD-Tdrs

   where:

WS	Number of Wait States	
tAD	Spec#6	PHI Fall to Address Valid
tEXr	Spec#65	External Clock Rise Time (EXTAL)
TdCS	Spec#71	$\overline{\text{MREQ}}$ Valid to $\overline{\text{ROMCS}}$, $\overline{\text{RAMCS}}$ Valid Delay

9. Low Noise Crystal Option

   This feature when enabled will select a low noise option for the extal and xtal pins of the Z182K. This option reduces the gain, in addition to reducing the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications where the crystal may be driven too hard by the oscillator.

10. PHI Output Disable

    When this bit is set, the PHI output is not driven by the system clock. Rather the PHI output will be forced to a high state. On production boards that do not use the PHI output, this feature can be used to reduce EMI.

11. Low Voltage Support

    The Z80182 Rev. K device will be capable of supporting low voltage operation at 3.3 volts with a maximum operating frequency of 20MHz.

12. Extended Temperature Operation

    The Z80182 Rev. K device will be capable of extended temperature operation at temperature ranges of -40° to +100° C, but we currently do not support production testing over the extended temperature range.

Attachment 3

Z80182 Errata Comparison Rev. H versus Rev. K

Note that “Yes” means the errata exists. “FIXED” on Rev. H below refers to fixes to the Z80182 Rev. G and “N/A” means the errata does not apply.

Errata	Description	Rev. H	Rev. K
1	MIMIC DMA asserts DMA requests erroneously	Yes	Yes
2	Emulation Timer Lock	Yes	Yes
3	ESCC data transfers cannot be simultaneously set up for DMA and Interrupt mode on the Z182	Yes	Yes
4	Icc Low Power Mode Ramp Problem	FIXED	N/A
5	Fast MIMIC Interrupt Resolution is not functional	Yes	Yes
6	Clearing of MPU shadow bits during Host FCR write	Yes	Yes
7	ESCC Ch. B ceases to request interrupts in ESCC Phi/2	Yes	Yes
8	Interrupt Edge/Pin Mux Register	FIXED	N/A
9	Port B overrides RxA0	FIXED	N/A
10	RTO Enhancement Problem	Yes	Yes
11	Z180 DMA/MIMIC RBR	Yes	Yes
12	$\overline{\text{HRxRDY}}$ assertion error	Yes	Yes
13	ST Pin Problem	FIXED	N/A
14	Incorrect ST State	FIXED	N/A
15	LCR Register Addressing Problem	FIXED	N/A
16	DRAM Refresh Problem with the WSG	FIXED	N/A
17	WSG Problem	FIXED	N/A
18	$\overline{\text{IOCS}}$ Error on 16 Cycle Delay	Yes	Yes
19	HTxRDY Assertion Error	Yes	Yes
20	ESCC Errata	Yes	Yes
21	Inconsistent MS byte PRT Problem	Yes	FIXED
22	$\overline{\text{INT0}}$ Assertion on MIMIC Access Bit Inversion	Yes	FIXED
23	DMA Channel 0 problem	Yes	FIXED

Errata	Description	Rev. H	Rev. K
24	ASCI overrun operation discrepancy	No	Yes
25	ASCI - CTS1E bit	No	Yes
26	ASCI - TXS behavior	No	Yes

Attachment 4

Z80182 Device Errata Descriptions

1. MIMIC DMA on both MPU and {C interface has timing problems or asserts DMA requests erroneously. MIMIC DMA is not usable.

2. Changing ESCC TRxCB prescalar to emulation timers may cause MIMIC FIFOs to lock up.

   Workaround: User should avoid changing timer clocks on the fly. Timers should be disabled prior to any modification of timer registers.

3. ESXX data transfers cannot be simultaneously set up for DMA and Interrupt mode on the Z182. For example, if DMA is configured to transfer data to ESCC when Tx buffer is empty and Interrupts are enabled to transfer data to ESCC when Tx buffer is empty, conflict can occur. It is possible for ESCC to export data instead of interrupt vector. Avoid simultaneous enabling of DMA and Interrupt mode data transfers to the ESCC.

4. When the Z182 is put into a powerdown mode, the Icc power consumption current exhibits a ramping effect whereupon entering the low powerdown mode, the current starts at the initial value then proceeds to ramp up and finally lowers down to a final value that is not the same as the initial value, but greater. This problem has been seen in Standby, Sleep, Idle and system Stop modes. IS FIXED ON Z182.

5. The Fast MIMIC Interrupt resolution is not functional. The MIMIC highest IUS bit may become set if ESCC and MIMIC requests interrupt service simultaneously and ESCC processes requests interrupt service simultaneously and ESCC processes the Interrupt Acknowledge. Although interrupt priority selection should arbitrate which device processes the Interrupt Acknowledge, the MIMIC IUS bit can become set while the ESCC exports an interrupt vector. All MIMIC and lower priority interrupts will be disabled until the MIMIC highest IUS bit is cleared.

   Workaround: Keep bit D0 of MIMIC Modification Register (xxE9H) disabled. Place a reset highest MIMIC IUS command in the root program which will ensure that the MIMIC IUS resets when this bit is set erroneously.

6. When the PC writes to the FIFO control register and attempts to reset the RCVR or XMIT FIFO, the MPU shadow bits (RCVR and XMIT FIFO reset status) may clear before the status is read. This becomes more apparent when operating above 5.0 volts.

   Workaround: During an FCR interlope to the MPU, read the FCR register. If the FCR does not indicate a Rx threshold change or FIFO enable bit change, then assume RCVR and XMIT FIFO reset. Since the XMIT FIFO

reset will force TEMT bit to zero, you may need to manually set this bit. Unless you are using the TEMT emulation feature, set the TEMT bit after reading a byte out of the THR register.

7. When the ESCC is used in divide-by-two mode, there is a possibility for ESCC Ch. B to cease requesting interrupts. Due to clocked signal paths that are doubled with respect to Z180 system clock, the following software workarounds are suggested.

   Workaround: If INT mode 2 is used for the ESCC, there is a possibility for lower priority interrupts to remain pending without asserting internal interrupt request. If the ESCC clock divider is enabled, place the ESCC reset highest IUS commands in the main loop of code to kick interrupts, should this condition occur.

8. The specification states that bits 3 and 2 of the Interrupt Edge/Pin Mux register is set during Power-Up and Reset. It is possible that these bits will fail to set when powered-up. If MRD/MWR pins are being used, it is required that bit 3 is set before doing a memory write. Also, if IOCS pin is used, bit 2 should be set prior to an external IORQ access. This is apparent in normal and EV modes and affects internal testing for low voltage Z182 devices. IS FIXED AND Z182K.

9. When the system Configuration Register is configured for Port B Select (bits D6 and D5), ASCI CH 0 RxA0 will become disabled. ASCI Ch. 0 will then not be able to receive data. In addition, the specification for bit D6 of the System Configuration Register should be rewritten as Port PB7-PB4 Select, not Port PB7-PB5. IS FIXED AND Z182K.

10. The RTO Timeout Enhancement Feature (Bit 1 in the FSCR Register) is not functional.

11. Z180 DMA/MIMIC RBR

    In the MIMIC master Control Register, RxDMA (Bit D4) does not function. Program this bit as 0. While in 16450 non-FIFO mode, the RBR DMA request to the Z180 DMA fails to deassert and will cause RBR FIFO Overrun. While in 16550 FIFO mode, the RBR to Z180/DMA request deassertion is delayed. The extent of deassertion delay is worsened by operation at high speed, low voltage, or high temperature. Using this DMA Request in level triggered DMA mode may cause RBR overruns. The effects of the delay is reduced by adding I/O wait states in the DCNTL register, using the edge triggered DMA mode, or assuring 5.0 volt operation.

12. $\overline{\text{HRxRDY}}$ Assertion Error

    When using the MIMIC in conjunction with the Receive timers, $\overline{\text{HRxRDY}}$ may assert erroneously before the receive emulation timers elapses. This

may result in multiple reads of the RBR FIFO when the HOST DMA uses the HRxRDY signal for the DMA request.

13. ST Pin Problem–Internal Test Issue

    The ST Status Pin is normally an output pin. However, in ATE Test Mode it is forced low upon reset. On power-up, the Z182 goes into /1 mode instead of the normal /2 mode. The problem in this test mode is that 30-50mA of tester pulldown is needed to overdrive the ST signal, which requires about =2v of Vil (from a 50 Ohm driver). IS FIXED AND Z182K.

14. The ST pin will always be in output mode under the following conditions: Normal Mode, Emulation Adaptor Mode, Emulation Probe Mode, BUSACK Mode, and HALT Mode. The ST pin will only 3-state and an internal resistive pulllup will be enabled when the reset pin is pulled low. The expected status of the ST pin during the aforementioned modes is listed below.

Mode	Expected	Actual
Normal	Output	Output
Emul Adapter	Input	Output
Emul Probe	3-State	Output
Reset	1	3-State
BUSACK	3-State	Output
HALT	0	Output

    IS FIXED AND Z182K.

15. The MIMIC LCR register does not decode the addresses A7-A4. When reading I/O addresses in which A3-A0 equals `0011`, the contents of the LCR register is accessed causing contention. If an external I/O device is assigned address xxx3H, a read from this address may be invalid due to a simultaneous access from the MIMIC LCR register. Therefore, all external I/O should be assigned addresses in which A3-A0 does not equal `0011`. Note that the addresses from 00-3fH are excluded from this error because these registers are accessed within the internal bus of the Z180 core. IS FIXED AND Z182K.

16. Using the DRAM Refresh Control feature (RCR Register) along with the Wait State Generator feature in the Z182 WSG Chip Select Register will cause the Z182 to fail to insert the programmed wits for memory accesses.

    Workaround: Do not use the DRAM Refresh Control feature when using the Wait State Generator feature in the Z182 WSG Chip Select Register to gen-

erate memory wail states for the Z182. Note: The DRAM Refresh Enable Bit (Bit 7 of RCR Register) is enabled upon default. Thus, the bit will need to be disabled prior to programming the DMA/Wait Control Register. IS FIXED AND Z182K.

17. Access to memory addresses beyond $\overline{\text{ROMCS}}$ and $\overline{\text{RAMCS}}$ boundaries will cause WSG to fail to insert programmed waits.

    Workaround: do not access memory addresses beyond the programmed $\overline{\text{ROMCS}}$ and $\overline{\text{RAMCS}}$ boundaries in the DAMUBR, RAMLBR, and ROMBR registers. IS FIXED AND Z182K.

18. $\overline{\text{IOCS}}$ error on 16 Cycle Delay

    $\overline{\text{IOCS}}$ may be asserted erroneously during interrupt acknowledge cycle following wakeup from sleep modes. This error can occur when the 16 cycle delay on halt recovery feature is enabled (bit 0 if Int/Edge Mux register), $\overline{\text{IOCS}}$ is enabled, and slp address is within address boundary of $\overline{\text{IOCS}}$. Since the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ strobe does not go active during the interrupt acknowledge cycle, $\overline{\text{IOCS}}$ assertion will not cause problems under most circumstances.

19. The $\overline{\text{HTxRDY}}$ signal may have problems because of a possible glitch in the signal. The $\overline{\text{HTxRDY}}$ signal, known as the Host Transmit Ready signal is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. The glitch in the signal causes the $\overline{\text{HTxRDY}}$ signal to go active when there is still 1 byte of data left in the buffer, thus preventing data to be properly serviced.

20. The ESCC errata are the same for both devices. Please refer to the errata listings for the Z85230. There are seven of these errata listed.

21. The feature of the PRT's, whereby the MS byte is latched when the LC byte is read, so as to ensure a consistent and correct 16-bit value, is not reliable at all times.

    Workaround: A software workaround is to read both bytes twice, in the order L, H, L, H, and use the later pair if the H bytes are equal, but use the former pair if the H bytes differ. IS FIXED AND Z182K.

22. The INT0 Assertion on MIMIC Access Feature (Bit 2 of the Z80182 Enhancements Register) when enabled will cause a low edge on the INT0 pin during any HOST access to the MIMIC when the HALT is active (Powerdown). Bit 21 is found to be the opposite as that defined in the technical specification of the Z182H. Instead of enabling this feature by setting bit 2 to a 1, this bit will be enabled by resetting the bit to a 0. In the previous Z182 device, bit 2 of the Z80182 Enhancements Register was reserved at 0; therefore this feature will become enabled.

Workaround: If this feature is not desired, set Bit 2 of the Z80182 Enhancements Register to 1. IS FIXED AND Z182K.

23. The DMA channel will not initiate a DMA operation with the ASCI channel 0 if the source or destination address is in the FXXXX, BXXXX, 7XXXX, or 3XXXX range.

    Workaround: If the data is located in the middle of the range, a workaround would be to do the ASCI0 DMA transfer to a different memory location and then do a second memory to memory DMA to move the data into the desired location. Use similar logic to perform an ASCI0 transmit. IS FIXED AND Z182K.

24. ASCI overrun operation discrepancy.

    In previous 182 versions, when an ASCI overrun error occurs, the microprocessor would set the OVRN Error (bit 6 of STAT0 or STAT1). Once the FIFO space became available, the receiver would automatically start putting data into the FIFO. Any character that is completed while the FIFO is full would naturally be lost. Since the data transfer was automatically restarted, it was impossible to determine what data is missed.

    For SL1932 (rev. K), once an overrun occurs, the receiver does not place any further data in the FIFO until the “last good byte received” has come to the top of the FIFO so that the Overrun latch is set and software then clears the Overrun latch. Assembly of bytes continues in the shift registers, but this data is ignored until the byte with the overrun error reaches the top of the FIFO and is cleared with a write of 0 to the EFR bit. This allows the user to determine exactly which data bytes were lost.

    Workaround: To begin transmitting data into the FIFO, clear the overrun flag by resetting Error Flag Reset (bit 3 of CNTLA0 or CNTLA1).

25. When CTS1E is set (Bit 2 of Reg 05H), bit 5 of Reg 03H should reflect the state of the multiplexed rxs/ctsl pin. This bit always shows 0.

26. When the TE is set to 0 (bit r of CSIO control register), the txs pin is held high. The txs, therefore, is high before a transmit starts and returns high on the rising CKS edge after the 8th bit has been transmitted.

    This may become an issue if the last bit sent is a 0 and the data is being sampled on the rising edge of the cks clock, since an incorrect “high” state may be sampled rather than the actual correct 8th bit.