Product Update

Errata for UM0094 - Z16C30 USC™ User's Manual

04/04 Introduction

This errata corrects a typographical error located in Chapter 8, Software Summary, pages 8-15 and 8-29 of the Z16C30 Universal Serial Controller User's Manual, Publication Number UM0094.

8.8 Register Reference

On page 8-15 of this chapter there is an error in the Channel Mode Register (CMR) table. The description for Bit CMR5, RxSubmode, states:

0=strip received Syncs; 0=include them in RxFIFO and CRC calculation

The statement should read as follows:

1=strip received Syncs; 0=include them in RxFIFO and CRC calculation

On page 8-29 there is an error in the Receive Mode Register (RMR) table. The description for Bit RMR8, QAbort, states:

0=Use Abort/PE bit in RxFIFO, RCSR2 for Abort indication; 0=use it for Parity Error Indication

The statement should read as follows:

1=Use the Abort/PE bit in RxFIFO, RCSR2 for Abort indication; 0=use for Parity Error Indication

05/03 Introduction

This errata corrects a typographical error located in Chapter 5, Serial Modes and Protocols, Page 5-22 of the Z16C30 Universal Serial Controller User's Manual, Publication Number UM0094. This correction allows the referenced paragraph to meet CRC-CCITT Standards for SDLC/HDLC mode.

5.16 Cyclic Redundancy Checking

Third paragraph currently reads:

00 in either field selects the 16-bit CRC-CCITT polynomial $x^{15}+x^{12}+x^5+1$. In HDLC, HDLC Loop, and 802.3 modes, the Transmitter inverts each CRC before sending it, the Receiver checks for remainders of $F0B8_{16}$, and the TxCRCStart and RxCRCStart bits should be programmed as 1 to start the CRC generators with all ones. In other synchronous modes the Transmitter sends accumulated CRCs normally and the Receiver checks for all-zero remainders.

Third paragraph should read as follows:

00 in either field selects the 16-bit CRC-CCITT polynomial $x^{16}+x^{12}+x^5+1$. In HDLC, HDLC Loop, and 802.3 modes, the Transmitter inverts each CRC before sending it, the Receiver checks for remainders of $F0B8_{16}$, and the TxCRCStart and RxCRCStart bits should be programmed as 1 to start the CRC generators with all ones. In other synchronous modes the Transmitter sends accumulated CRCs normally and the Receiver checks for all-zero remainders.

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As used herein

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