Seven Signal Serial Control Interface to ZiLOG Modem Data Pumps

INTRODUCTION

Applications such as television set-top box use a low speed embedded modem to transfer small amounts of data over the telephone network. It may be desired to eliminate redundant silicon in such a system by connecting the modem data pump directly to a host processor in the application.

Some host processors, especially if included in an ASIC, may have a limited number of signal pins available to control the modem data pump. Normally host interface to Zilog data pumps is through the parallel port, which requires a interface of fifteen (15) signal pins. This application note will demonstrate how to connect ZiLOG modem data pumps to a host processor, with as few as seven (7) signal lines.

It is possible to interface a controller to the Z02201, Z02202, Z02922 or Z02923 Modem Data Pump in a serial fashion with as few as seven signals using a small number of standard TTL parts. This note describes an interface using six output signals (**/RD**, **/WR**, **CLK**, and address lines **A0**, **A1** and **A2**), and one bi-directional signal for serial data (**SERDAT**).

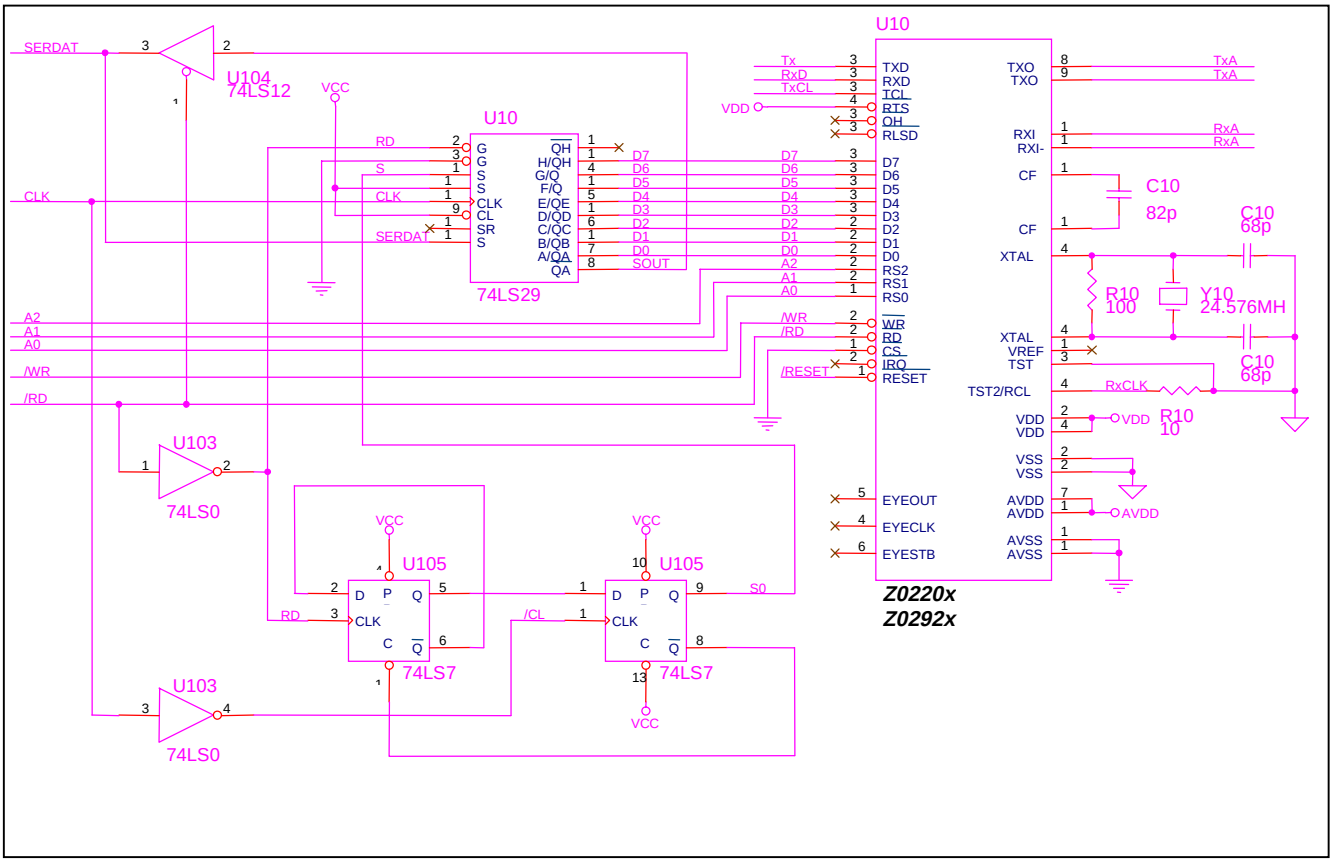

Figure 1. Seven Signal Serial Control Interface Schematic

OPERATIONAL OVERVIEW

The 74LS299 is a bi-directional shift register with tri-state parallel outputs. The shift-in and shift-out operations occur using the most significant bit first. To permit a common serial input/output line, the 74LS125 buffers the signal from the shift register. The bit order may be reversed by shifting the bit order of the data bus to the data pump.

Read Operation

Setting **/RD** causes the 74LS74's **S0** signal to place the shift register into load data mode on the next falling edge of **CLK**. The next rising edge of **CLK** then loads the shift register from the data pump. Data bits (**D7**, **D6**, etc.) are read on the following 8 falling edges of **CLK**. It is important to note that:

- Data can only be shifted out with **/RD** held low (active), and
- **SERDAT** must be set as an input on the host processor for the entire time **/RD** is low.

Write Operation

Data is loaded into the shift register via **SERDAT** on the rising edge of **CLK**. After the last bit (**D0**) is loaded, **/WR** strobes the data into the data pump. **SERDAT** must be set as an output on the host processor while data is loaded into the shift register.

Timing

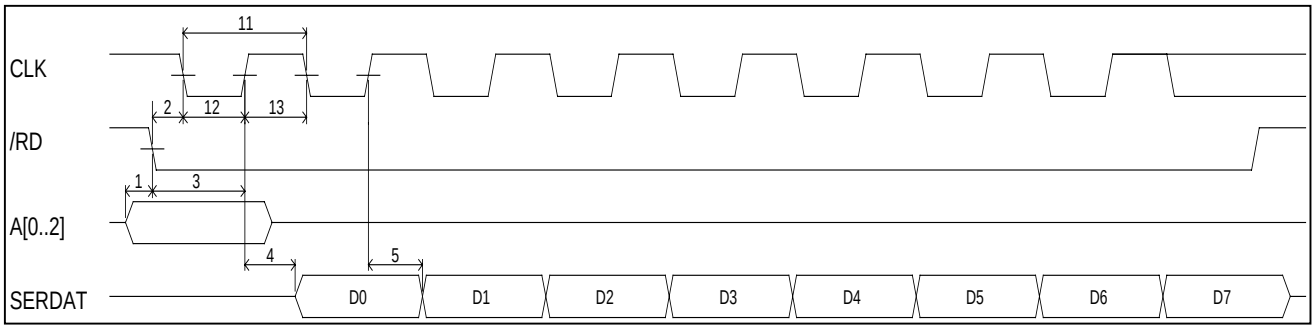

Figure 2: Read Timing

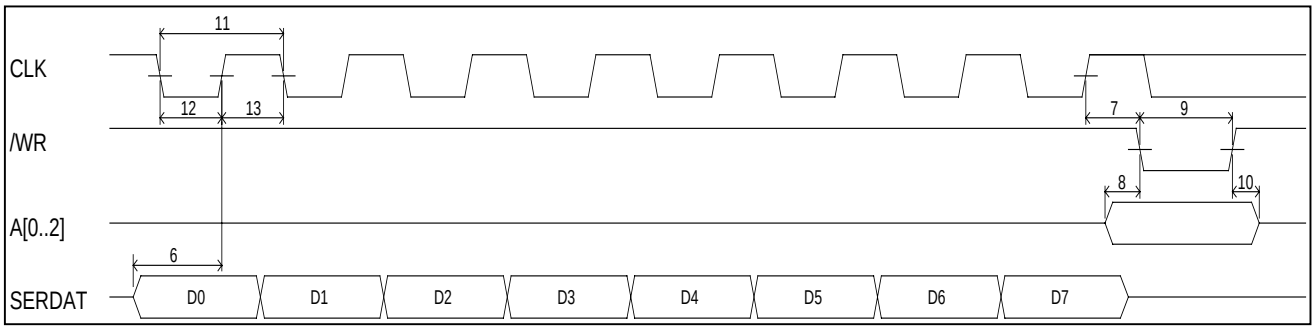

Figure 3: Write Timing

Description	*Parameter*	*Min*	*Max*	*Units*
Read Timing				
Address setup	1	0		ns
/RD to ***CLK*** low	2	60		ns
/RD to ***CLK*** high	3	225		ns
CLK to ***D7*** valid	4	20		ns
CLK to data delay	5	20		ns
Write Timing				
Data setup	6	20		ns
/WR delay from ***CLK***	7	75		ns
Address setup	8	70		ns
/WR width	9	25		ns
Address hold	10	10		ns
CLK Timing				
CLK frequency	11	0	3	MHz
CLK low	12	155		ns
CLK high	13	95		ns

Table 1: Signal Timing

CONCLUSION

ZiLOG's advanced V.22bis/ V.29 ZiLOG Modem Data Pumps can be connected to host processors with very few control signals and very little glue logic.

Information Integrity

The information contained within this document has been verified according to the general principles of electrical and mechanical engineering. Any applicable source code illustrated in the document was either written by an authorized ZiLOG employee or licensed consultant. Permission to use these codes in any form besides the intended application, must be approved through a license agreement between both parties. ZiLOG will not be responsible for any code(s) used beyond the intended application. Contact your local ZiLOG Sales Office to obtain necessary license agreements.

Document Disclaimer