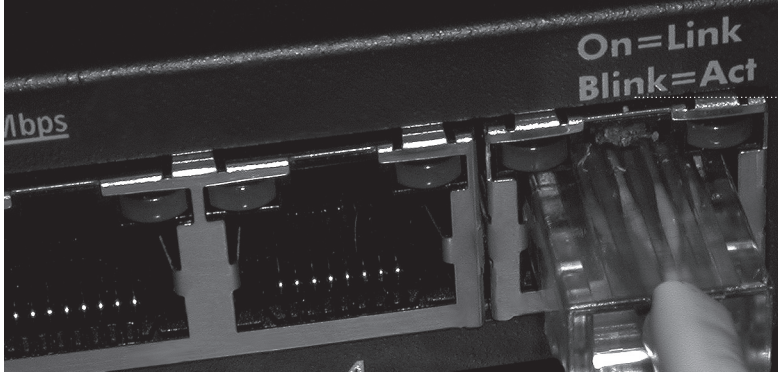


PB022002-0807

eZ80ACCLAIM*PLUS!* ADVANTAGE

SUMMARY

- 10% PERFORMANCE INCREASE
- UPDATED ZTP SOFTWARE SUITE
- VERSATILE Zdots® SBCs

TARGET APPLICATIONS

- INDUSTRIAL CONTROL
- COMMUNICATION DEVICES
- AUTOMATION
- SECURITY
- CONSUMER ELECTRONICS
- MEDICAL
- ENTERTAINMENT
- VENDING MACHINES
- EMBEDDED-INTERNET DEVICES

eZ80Acclaim*Plus!*™ High-Performance Connectivity ASSP

Overview

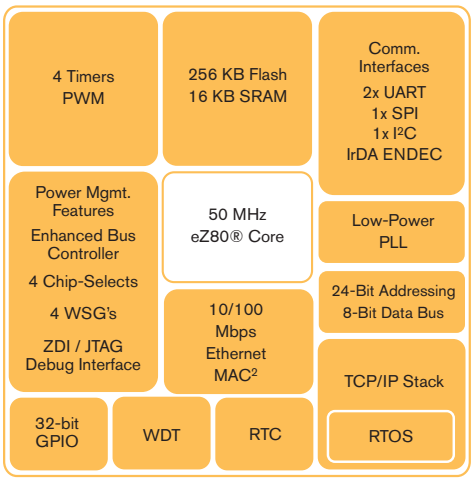
The eZ80Acclaim*Plus!* Connectivity ASSP is the latest in the award-winning eZ80Acclaim!® product family, which integrates a high-performance Flash ASSP core with a fast 10/100 BaseT EMAC. Our power-efficient, optimized pipeline architecture features a high performance core that operates up to a speed of 50 MHz, and offers on-chip Flash Memory, SRAM, an Ethernet MAC (EMAC), and rich peripherals. Adding to the existing eZ80Acclaim! feature set, the eZ80Acclaim*Plus!* touts an updated embedded internet software suite (ZTP), a flexible line of single-board computers (SBCs) named Zdots®, and an additional 10% system performance boost that equates to faster program execution and smaller memory space requirements over the current eZ80Acclaim! family.

The eZ80Acclaim*Plus!* Connectivity ASSP is a great time-to-market embedded solution for any device that needs Ethernet connectivity and is well-suited for industrial, communication, automation, security, consumer electronics, medical, entertainment, vending machines, and other embedded Internet applications.

eZ80Acclaim*Plus!* Key Feature Summary

- 50 MHz high-performance eZ80® CPU core
- On-chip 10/100BaseT Ethernet MAC
- 256 KB Flash Program Memory with an extra 512 Bytes of device configuration Flash
- 16 KB total on-chip high-speed SRAM
- 24-bit Addressing
- Low-power PLL and 32 KHz on-chip oscillator
- Zilog's ZTP Embedded Internet Software Suite with TCP/IP stack (PPPoE & USB 2.0 support available Q4 2007)
- Zilog's RZK Real-Time Operating System (RTOS) with up to 32 priority levels
- Interfaces supported: 32-bit GPIO, UARTs (x2), I^2C, SPI, and IrDA-compatible Infrared Endec
- Power management: HALT/SLEEP modes, with selective peripheral power-down controls

eZ80Acclaim*Plus!* Block Diagram



Electrical Characteristics

- Power supply: 3.3 V ± 0.3 V
- Standard temperature: 0 °C to 70 °C
- Extended temperature: –40 °C to +105 °C
- Supply current: 50 MHz; 137 mA (typical)
- Supply current in HALT mode with peripherals powered down: 75 mA (typical)
- Supply current in SLEEP mode: 2.5 µA (typical; VBO disabled)

eZ80Acclaim*Plus!* ASSP Detailed Feature Set

KEY HARDWARE FEATURES

- eZ80® CPU CORE
- ON-CHIP FLASH MEMORY
- 10/100 BASET EMAC
- PLL & ON-CHIP OSCILLATOR

eZ80 CPU CORE

The eZ80 CPU operates either in Z80®-compatible (64 KB) mode or full 24-bit (16 MB) linear address mode. With increased clock speed and processor efficiency, the processing power of the eZ80 CPU core rivals the performance of many 16-bit microprocessors. The eZ80 CPU core improves on the world-famous Z80 architecture, and like the Z80, this core features dual bank registers for fast context switching.

Block transfer instructions with expanded repeat capability are also added to the eZ80® CPU. They provide high-performance data transfer similar to hardware DMAs.

ON-CHIP FLASH MEMORY

Like the original eZ80Acclaim!®, the eZ80Acclaim*Plus!* Connectivity ASSP features 256 KB of Flash Program Memory. A separate page of 512- bytes Flash Memory is also available for general device configuration data. Other on-chip memory features include:

- Single power supply operation
- Page erase feature; 2048 bytes/page
- Fast page erase and byte program operation
- 78 ns minimum read cycle
- Endurance: 10,000 write cycles (typical)
- Data retention for more than 100 years at room temperature

In addition, 16 KB of high-speed, re-locatable SRAM is available, and 8 KB is for general-purpose use. Another 8 KB is used by the EMAC for Ethernet operation, but is also user-accessible when Ethernet functionality is not required.

10/100 BASET ETHERNET MAC (EMAC)

The Integrated IEEE 802.3 Ethernet controller has 8 KB of dynamically-configurable Tx/Rx frame buffer. It supports 10 Mbps and 100 Mbps, full duplex operation, and an industry-standard Media Independent Interface (MII) for simple connection to an external Physical Layer Interface (PHY) device.

The eZ80Acclaim*Plus!* family delivers high performance and overall cost effectiveness as an embedded network ASSP. High performance is achieved by optimizing the internal bus design of the eZ80® CPU with shared memories, dedicated Ethernet Tx/Rx DMAs, and Tx/Rx FIFOs. This bus design provides the highest data throughput over the Ethernet interface, yet requires minimum eZ80® CPU intervention and minimizes system loading.

PLL AND ON-CHIP CRYSTAL OSCILLATOR

The eZ80Acclaim*Plus!* Connectivity ASSP features a low-power, programmable PLL that can be selected to generate the system clock. Taking the input from the on-chip crystal oscillator, the PLL generates system clock speeds up to 50 MHz from low-cost, low-frequency external crystals in the range of 1 MHz to 10 MHz.

eZ80Acclaim*Plus*! ASSP Detailed Feature Set (continued...)

KEY SOFTWARE FEATURES
- ZILOG ZTP SOFTWARE SUITE
- ZILOG RTOS

ZTP

Zilog's **T**CP/I**P** solution (ZTP) is an integrated, pre-emptive multitasking OS and TCP/IP protocol software suite optimized for embedded systems. ZTP includes Zilog's RZK RTOS, and works in conjunction with the award-winning eZ80Acclaim! product family of Flash microprocessors to provide standard network connectivity in a wide range of applications, including industrial control, automation, facility management, IP appliances, and remote systems communication. The ZTP software suite is optimized for low-cost systems, and offers full-feature operating system services in addition to network services while occupying little program memory. User applications can be integrated with ZTP via an easy-to-use and well-documented Application Programming Interface (API).

The Internet standard for secure network communication is the Secured Socket Layer protocol (SSL). An optional SSL plug-in package for Zilog's TCP/IP software suite (ZTP) is available separately for the eZ80Acclaim! Flash products. To maintain export law compliance, a US version as well as an International version is available.

The ZTP software suite provides the following features:
- Industry standard, RFC compliant protocols
- Core protocols: IPv4, TCP, UDP, DHCP/BOOTP, ICMP, IGMP, ARP, RARP
- Additional protocols: HTTP, TFTP, SNMP, TELNET, SMTP, DNS, TIMEP, SNTP, PPP and HDLC
- Optional protocols: SSL server, SNMP V3 and HTTPS
- Interconnects: UART(x2), I^2C, SPI
- FTP server and client services using an embedded Flash file system supporting multiple disk volumes
- Local or remote runtime debugging OS command shell
- Dynamic memory allocation support

ZILOG RTOS

Zilog's real-time preemptive multitasking kernel, RZK, is designed for time-critical embedded applications. RZK is configurable, scalable, and modular in design; it provides a rich set of features via easy-to-use and well-documented APIs. Additionally, RZK features are highly optimized to the stringent memory and performance requirements of embedded applications.

AVAILABLE INTERFACES
- JTAG
- UARTS
- 32-BIT GPIO
- IR ENCODER/DECODER

JTAG INTERFACE

An IEEE 1149.1-compatible five-pin test access port (TAP) is provided to interface with the on-chip test logic defined by the IEEE standard. The TAP also includes Boundary Scan functions, and is used to control on-chip emulation/debugging capabilities. Some features include software break points, a 64-word trace buffer, complex break points using address and data masks, and cascadable triggers.

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

Each of the two UART channels contains a transmitter, a receiver, control logic/registers, and a Baud Rate Generator (BRG).

- The BRG produces a lower-frequency bit clock from the system clock. All standard baud rates up to 115 Kbps (and higher) are supported.
- The UART module implements the logic required to support asynchronous communications, hardware flow control, and 9-bit character format. The module also contains separate 16-byte-deep transmit and receive FIFOs.

eZ80Acclaim*Plus!* ASSP Detailed Feature Set (continued...)

GENERAL-PURPOSE INPUT/OUTPUT

There are 32 bits of GPIO. All GPIO pins are individually programmable, and support the following I/O modes: input, output, open drain, open source, level-triggered interrupts (High or Low), edge-triggered interrupts (High or Low), dual edge-triggered interrupts, and alternate function. Eight of the output pins can sink 10 mA each (Port A), while 16 other pins feature Schmitt-trigger input buffers (Port B and Port C).

INFRARED ENCODER/DECODER

- Supports IrDA SIR format
- Operates seamlessly with on-chip UART
- Interfaces with IrDA-compliant transceivers
- Supports transmit/receive to 115 Kbps

eZ80Acclaim*Plus!* Power Management Capabilities

The eZ80Acclaim*Plus!* Connectivity ASSP supports several power management features. Two peripheral Power-Down Registers allow independent clock gating of on-chip peripherals under software control while operating under normal conditions. The eZ80® CPU writes to the control registers to disable the clock from driving any one of the peripherals while they are inactive. In addition, execution of the HALT instruction suspends the eZ80 CPU operation and eliminates the clock power associated with the eZ80 CPU core. Normal operation is restored via external and peripheral interrupts or hardware reset. Execution of a sleep (SLP) instruction provides the lowest power consumption. In SLEEP mode, only the on-chip RTC 32 KHz crystal oscillator remains active to drive the RTC and the WDT. Other peripherals, like the system clock and the primary oscillator, are disabled. The user can reset the device by RTC alarm, a WDT time-out, or hardware reset.

Support Tools

The following development tools are available to program and debug the eZ80Acclaim*Plus!* ASSP:

Hardware

- Zdots® SBC for the eZ80Acclaim*Plus!*™ Connectivity ASSP

  Zilog's Zdots® are compact, high-performance single board computers (SBCs) specially designed for the rapid development and deployment of embedded systems. Our Zdots SBCs can be a quick development solution in embedded proof of concepts, provides easy design flexibility, and can even be dropped into production-level systems for faster time-to-market. Dot all your innovative ideas with Zdots SBCs from Zilog!

- eZ80Acclaim!® Full Development Kit
- eZ80Acclaim!® Cost-Effective Modular Development Kit

Software

- Zilog TCP/IP (ZTP) Software Suite
- Zilog RZK Real-Time Operating System (RTOS)
- Full ANSI C-Compiler
- Web Page-to-C Converter
- Web Authoring Tools
- Zilog Developer's Studio Integrated Development Environment (ZDS II IDE) including an assembler, linker, debugger, and simulator

Ordering Information

Order the eZ80Acclaim!® and eZ80Acclaim*Plus!*™ from your local Zilog sales representative by using the part numbers below. For more information, or to download product collateral and/or software, please visit us at www.Zilog.com.

Part Number	Description	Package
eZ80F91AZA50SG	50 MHz; Standard Temperature	144-LQFP
eZ80F91AZA50EG	50 MHz; Extended Temperature	144-LQFP
eZ80F91NAA50SG	50 MHz; Standard Temperature	144-BGA
eZ80F91NAA50EG	50 MHz; Extended Temperature	144-BGA
eZ80F910300ZCOG	eZ80Acclaim! Development Kit	
eZ80F910200KITG	eZ80Acclaim! Modular Development Kit	
eZ80F917050SBC	Zdots® SBC for the eZ80Acclaim*Plus!*	
ZUSBSC00100ZACG	USB Smart Cable Accessory Kit	
ZENETSC0100ZACG	Ethernet Smart Cable Accessory Kit	

Documentation

The collateral referenced below is just a sample of the documentation available for the eZ80Acclaim*Plus!* Connectivity ASSP. For a complete listing of all available application notes, product specifications, user manuals, and sample libraries, please visit us at www.Zilog.com/ez80acclaimplus.

Document Number	Description
PS0270	eZ80Acclaim*Plus!* Product Specification
PS0261	Zdots® SBC for the eZ80Acclaim*Plus!* Connectivity ASSP Product Specification

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