Technical Note

eZ80Acclaim!® Design for Debug

TN003503-0607

Introduction

The ZiLOG debug interface (ZDI) provides on-chip support for debugging software and programming Flash memory. ZDI supports all microcontrollers of Zilog's eZ80Acclaim!® family.

The Debug Connector

All ZiLOG debug tools, including ZPAK-II, USB Smart Cable, and the Ethernet Smart Cable require a 6-pin connector on the target system for debugging. This connector is a 3 by 2 header with standard 0.025 inch square posts on 0.100-inch centers, and is similar to the headers commonly used for jumper blocks. Figure 1 illustrates the connections between the debug connector and the eZ80Acclaim! microcontroller.

Note: *The connector pin arrangement is depicted as viewed from top.*

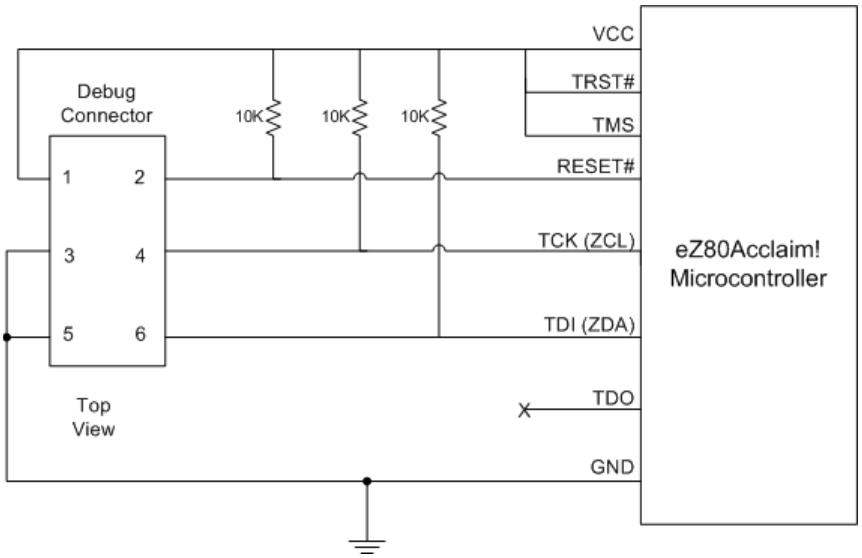

Figure 1. Target ZDI Connector Interface

ZDI Signals

The ZDI interface uses the microcontroller's JTAG pin TCK as the debug clock, ZCL. The JTAG pin TDI is used for bidirectional debug data, ZDA. If your design does not use JTAG, tie TRST# and TMS high to prevent unintentionally activating JTAG mode. TDO can be left unconnected.

The ZCL and ZDA signals require 10 K to 100 K pull-up resistors on the target board to pull them to their idle, high states when the debug tool is not connected. The ZDA driver on the microcontroller sinks a maximum of 8 mA, prohibiting smaller values for its pull-up resistor. In extreme cases, the ZCL pull-up resistor on the target could be reduced to lower the impedance of the receiver, keeping in mind that the debug driver is capable of sinking a maximum of 20 mA.

The ZCL and ZDA traces should be as short as possible on the target board, preferably no more than a few inches. Termination on the target system board is generally not required, and parallel termination is not recommended because the signals are open-drain and must have a high idle state. The ZDA signal is bidirectional, so a 33 Ω series resistor at the pin on the target system may be helpful when it is driving.

Figure 2 displays the debug tool ZDI interface. The ZCL and ZDA signals are both series terminated at the source in the debug tool by 33 Ω resistors. These signals are driven by the ZiLOG debug tool only when data is being transferred. When idle, the drivers are tristated and the pins held in the idle, high state by pull-up resistors.

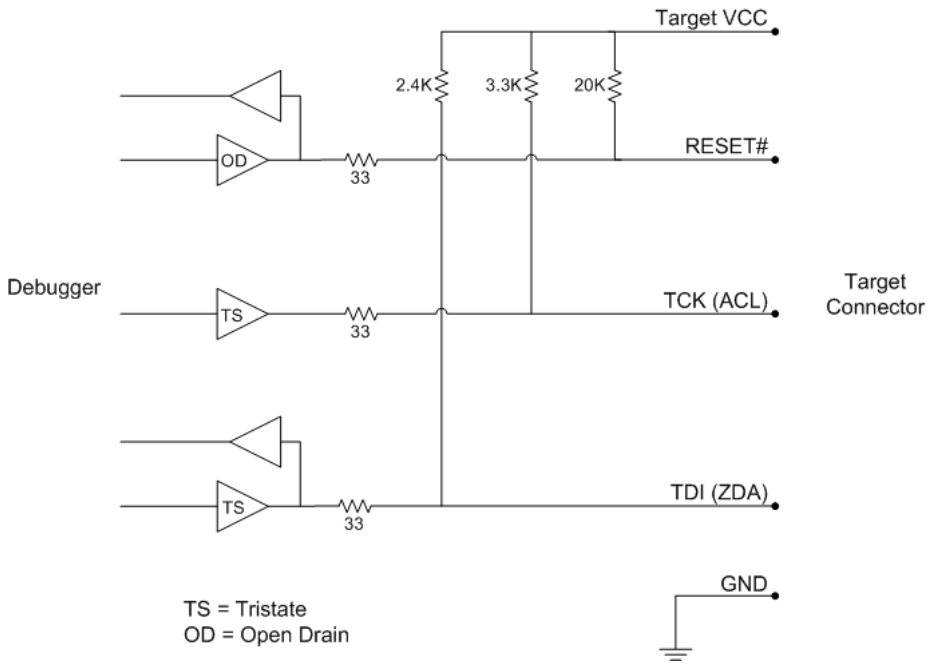

Figure 2. Debug Tool ZDI Interface

Reset

The eZ80Acclaim! RESET# pin is bidirectional and open-drain. RESET# must be connected to the debug header. An external circuit can drive the pin to generate a reset and the microcontroller continues to drive the RESET# pin for 1025 clocks after release. The microcontroller has a built-in power-on reset circuit, so the RESET# pin requires only a 10 K pull-up resistor for proper operation. If an external circuit is used to drive RESET#, it must be open-drain.

Target Power

The target system V_{CC} must be connected to the debug connector. This must be the same voltage level as supplied to the microcontroller. The ZPAK-II and the USB Smart Cable use less than 5 mA of target current to operate the debug drivers and receivers. The USB Smart Cable drivers and receivers automatically adapt to handle any target voltage between 2.0 V and 3.6 V. The ZPAK-II interface operates only at 3.3 V.

Ceramic bypass capacitors, 0.1 µF or 0.01 µF, must be connected between each power pin and ground pin on the microcontroller.

Ground

It is very important to have a good ground return path for the debug signals ZCL and ZDA. A 4-layer board with continuous power and ground planes is best. If a 2-layer board is used, a ground trace parallel to ZCL and ZDA between the debug connector and the microcontroller ground pins is recommended.

Tips for Debugging

Follow the instructions below for debugging:

- Ensure that target V_{CC} is the correct voltage and without excessive ripple. The Flash programming operation requires slightly more power for the microcontroller, so check that voltage is valid and does not droop during this operation.
- Ensure that the system clock is clean at XIN and verify the core clock by observing the PHI clock output pin.
- Ensure the quality of the ZCL (TCK) and ZDA (TDI) signals at the target microcontroller pins, using an oscilloscope while the debugger is operating. Some amount of undershoot below ground and overshoot above V_{CC} is not unusual. It is more harmful if glitches or ringing occurs in the middle of rising or falling edges, extending into the band between 1.0 V to 2.0 V above ground. These can be interpreted as extra clock or data edges.
- On rare occasions, debugger communications can be compromised by a ground loop condition between the host PC, the debug tool, and the target system. In these cases, use a common AC outlet or power strip for all systems can fix the problem.

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As used herein

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