Technical Note

Migration from eZ80Acclaim!® eZ80F91 MCU to eZ80Acclaim*Plus!*™ eZ80F91 Connectivity ASSP

TN005206-0807

General Overview

This Technical Note highlights the improvements and feature enhancements from Zilog's eZ80Acclaim!® products in the eZ80F91 version to the eZ80Acclaim*Plus!*™ products. These changes are implemented in a backward-compatible manner for easy migration to the products listed in Table 1. Some of these improvements include the addition of four new internal registers for the General-Purpose Input/Output (GPIO) fix of the eZ80Acclaim! eZ80F91 MCU errata. The eZ80Acclaim*Plus!* eZ80F91 Connectivity ASSP device has undergone other eZ80Acclaim! eZ80F91 MCU errata fixes as well. This document provides a quick transition to the new silicon.

Table 1 lists the eZ80Acclaim*Plus!* products upgraded with the implemented improvements and feature enhancements.

Table 1. Zilog® Product Number Identification

eZ80F91AZA50SG	eZ80F91AZA50EG	eZ80F91NAA50SG	eZ80F91NAA50EG

Note: Includes both the LQFP as well as the BGA packages.

The improved key features listed below apply only to the devices listed in Table 1.

Improved Key Features

The improved key features in the eZ80Acclaim*Plus!* eZ80F91 Connectivity ASSP compared to the eZ80Acclaim! eZ80F91 MCU products include:

- GPIO edge-triggered interrupts function as specified
- Real-time Clock (RTC) functional and logical improvements
- Universal Asynchronous Receiver/Transmitter (UART) functional and logical improvements
- The Timer now handles timer events as specified
- The Flash external WP pin function works as specified
- The Flash info page is now under user control for the mass erase command
- The Watchdog Timer (WDT) time-out ranges have been reduced
- The IrDA receiver has improved pulse-width checking

- When disabled, alternate function blocks are now isolated from the shared GPIO pins:

  For example, the alternate SPI functionality shares the GPIO PB[2] as the slave select (SS). With the new silicon, the SS will not enter the SPI functional block as before, until you enable the alternate SPI functionality.
- Lower SLEEP mode current over temperature and voltage ranges
- Improved the 9-bit multidrop mode:
  - Hardware address compare for improved performance
  - Receive FIFOs work in this mode
- Added a register bit to power down the Voltage Brownout (VBO) circuit for lower SLEEP mode current
- ZDI and JTAG ID revisions were synchronized to Revision 2 for the two debug interfaces and device identification

Modifications and Migration Impact from the eZ80Acclaim! eZ80F91 MCU to the eZ80Acclaim*Plus!* eZ80F91 Connectivity ASSP

The modifications and migration impact for the following blocks are described below and references to the errata for eZ80Acclaim! eZ80F91 (UP0061):

- I/O Pad
- Power Down Controller
- Reset
- GPIO Block
- UART Block
- RTC Block
- WDT Block
- Timers
- Flash

I/O Pad

Modifications

The following changes are done to improve the functionality of I/O pins:

- Errata #5 (TDI pad does not meet the 1149.1 Boundary Scan Specification)
  - Added a pull-up resistor within the pad to meet the 1149.1 specification.
- The I/O ports help contribute to the reduction of the overall SLEEP mode current.

Impact

No software change required.

Power Down Controller

Modifications

VBO power down bit added to the CLK_PPD2 register. This will help reduce SLEEP mode current if you can power down disable VBO.

Impact

A software change is required to take advantage of the additional reduction in SLEEP mode current if the VBO feature is not required. To implement this, set or clear bit 6 of the register (CLK_PPD2 = 0x00DCh). Whenever the VBO_OFF (bit 6) of the CLK_PPD2 is set, the VBO circuit is disabled. Whenever the VBO_OFF (bit 6) of the CLK_PPD2 is cleared, the VBO circuit is enabled.

Reset

Modifications

The reset modifications are as follows:

- An analog filter is added to the $\overline{\text{RESET}}$ input pin to help improve the glitch rejection of this pin.
- A functional change was made to stop the CPU execution before the on-chip peripherals are reset.

Impact

No software change required. Applications using external $\overline{\text{RESET}}$ input show improved behavior of this pin to reject glitches on the reset pin.

GPIO Block

Modifications

Following modifications are incorporated to improve the GPIO performance:

- Errata #6 (GPIO edge-triggered interrupt mapping error), the root cause was found and design changes in the hardware fix the problem.
- The addition of four Write-only registers to clear out edge-triggered interrupts. These four registers are mapped at new internal I/O locations to minimize the software change requirements. The name and address of these four registers is provided below:
  - PA_ALT0—address 0x00A6h
  - PB_ALT0—address 0x00A7h
  - PC_ALT0—address 0x00CEh
  - PD_ALT0—address 0x00CFh

Impact

The software must use the new Px_ALT0 register to clear interrupts instead of writing to the Px_DR register to clear them.

- The alternate function modalities are qualified with the ALTERNATE FUNCTION mode setting. The input pins of the alternate modalities such as SPI, IrDA, I2C, and UART are not "listening" to the GPIO pins when they are disabled (not in the ALTERNATE FUNCTION mode). The alternate function blocks ignore any changes on the GPIO inputs.

Impact

No software changes are required unless the software takes advantage of the fact that the alternate function blocks are "listening". In this case, the software will need to setup the alternate function according to the *eZ80AcclaimPlus! Connectivity ASSP eZ80F91 ASSP Product Specification (PS0270)*.

UART Block

Modifications

The UART clear receive FIFO (CLRRxF) bit 1 and clear transmit FIFO (CLRTxF) bit 2 of the UARTx_FCTL register have changed functionality. The original functionality of these bits is described in Errata #8. Both these bits are now persistent enable bits for the receiver and transmitter paths.

Impact

The impact of the software change requires you to add the setting of these bits in the UART initialization code to enable the receiver and transmitter. When these bits are cleared, the receiver and transmitter are disabled and their respective FIFOs are cleared.

Register (UART0_FCTL = 0x00C2h, UART1_FCTL = 0x00D2h) — The CLRTxF (bit position 2) and CLRRxF (bit position 1) of each respective UART will need to be set to use that specific UART. For more information, refer to the *UART section of the eZ80AcclaimPlus! Connectivity ASSP eZ80F91 ASSP Product Specification (PS0270)*.

- The UART 9-bit multidrop mode has two enhancements to improve data transfers and simplify software handling:
  - Use the UARTx_SPR register to store the UART's multidrop address.
  - The receive FIFO can now be used in multidrop mode.

Impact

The software is required to store the multidrop address into the UARTx_SPR. After this is done the hardware will now check on the address marks comparing the incoming address is equal to the address stored in the UARTx_SPR. If the addresses match, then the address byte and all the data bytes are received until the next address mark occurs. This change allows you to remove all the extra SW code written to filter the input data stream for packets that match the F91s multidrop address.

Register (UART0_SPR = 0x00C7h, UART1_SPR = 0x00D7h) — Whenever the receive Data Ready (bit 0) of the UARTx_SPR is set, the incoming data is for the multidrop address.

In RS485 multidrop mode, the first byte of the message is the station address and the rest of the message contains the data for that station. You must set the Even Parity Select (EPS bit 4) and Parity Enable (PEN bit 3) in the UARTx_LCTL before sending the station address. We recommend that in

your UART initialization routine set up the UARTx_LCTL register for your data transfer format and set the Parity Enable (PEN bit 3) bit.

Follow the steps below each time you want to send a new message:

1. Since the UART automatically clears the Even Parity Select (EPS bit 4) bit in the UARTx_LCTL after a byte is sent, before starting a new message you have to wait for the transmitter to go idle. The Transmit Empty (TEMT bit 6) of the UARTx_LSR will be set. If you set the EPS bit of the UARTx_LCTL before the last byte of the previous message is transmitted, the EPS bit is cleared and the new station address is sent as data instead of being used as an address.
2. Setting the Even Parity Select (EPS bit 4) bit in the UARTx_LCTL register (being careful not to alter the other bits in the register) sets the address mark. Write station address to the UARTx_THR. The UART will automatically clear the EPS bit after the station address byte is transmitted.
3. Send the rest of the message. Write data to the UART Transmit Holding Register UARTx_THR whenever the Transmit Holding Register Empty (THRE bit 5) in the UARTx_LSR is set.

RTC Block

Modifications

Following hardware modifications were done to improve the RTC performance:

- Errata #1 (RTC excessive current not in SLEEP mode), the root cause was found and design changes in the hardware fix the problem.
- Errata #3 (RTC_Xin pin leakage 10 uA) was a documentation issue, the Product Specification is changed to identify the proper condition for the RTC_Xin pin when not using the RTC block.
- Errata #4 (RTC slowdown of 2 s after multiple power downs) cannot be duplicated, but the root cause for Errata #7 is identified and could be the root cause of Errata #4 as well.
- Errata #7 (RTC loses large amounts of time at spurious intervals), the root cause was found and design changes in the hardware fix the problem.

Impact

No software changes required.

WDT Block

Modifications

The following modifications were made to improve the WDT performance:

- Reduction of the time-out ranges to provide faster recovery when not using 50 MHz as the system clock.

  The WDT_CTL[1:0] was used to select fixed divider values and depending on the system clock the time-out range delays were too wide. When the system clock was 32.768 kHz, the following time-out values were selected.

- The old ranges for the WDT are listed below:
  - 8.0 secs when WDT_CTL[1:0] = 11
  - 128.0 secs when WDT_CTL[1:0] = 10
  - 1024.0 secs when WDT_CTL[1:0] = 01
  - 4096.0 secs when WDT_CTL[1:0] = 00

  The WDT_CTL register now uses the lower 4 bits to select the WDT clock source and the WDT period time. The WDT_CTL[3:2] is the WDT_CLK and used to select the clock source that drives the WDT. The WDT_CTL[1:0] is the WDT_PERIOD and used to select different divider values to reduce the ranges and provide shorter time-out range delays. The Product Specification provides examples in the WDT chapter.
- Using the same example, the new time-out range for the WDT is listed below:

  For example, when the WDT_CTL[3:2] register is set to 00 to select the WDT clock source as the system clock. Now if the system clock source is 32.768 kHz, then the following time-out delay values become available when the WDT_PERIOD is changed:
  - 3.90 msecs when WDT_CTL[1:0] = 11
  - 65.2 msecs when WDT_CTL[1:0] = 10
  - 0.5 secs when WDT_CTL[1:0] = 01
  - 4.0 secs when WDT_CTL[1:0] = 00

Impact

You will now have to adjust your WDT_CTL register settings according to the new time-out delay settings.

Timers

Modifications

Following hardware modification was done to improve the Timer performance:

- Errata #9 (Timer misses timer events), the root cause was found and design changes in the hardware fix the problem.

Impact

No software changes required.

Flash

Modifications

Following hardware modifications are incorporated to improve the flash functionality:

- Errata #2 (WP pin functionality), the root cause was found and design changes in the hardware fix the problem.

Impact

No software changes required.

A request to have the info page erase optional during a mass erase; a design change was done in the hardware to support this.

Impact

The software is required to indicate whether or not the info page is erased with the mass erase command. To implement this, you have to set or clear bit 7 of the register (FLASH_PAGE = 0x00FCh). Whenever the INFO_EN (bit 7) of the FLASH_PAGE is set and the mass erase command is issued, the main and info sections of the flash block are erased. Whenever the INFO_EN (bit 7) of the FLASH_PAGE is cleared and the mass erase command is issued, only the main section of the flash block is erased.

eZ80Acclaim*Plus!* Connectivity ASSP eZ80F91 ASSP Product Specification (PS0270) differences to the eZ80Acclaim! Flash Microcontrollers eZ80F91 MCU Product Specification (PS0192)

The following documentation changes are made to correct the errors in PS0192, improvements to clarify the chapter descriptions, and added improved eZ80F91 silicon changes:

Chapter: Architectural Overview

The description of the Pins 55, 61, 63 and 69 modified in Table 2 on Page 6.

Chapter: General Purpose Input/Output

Totally rewritten.

Chapter: Chip Select and Wait States

Page 78, Input/Output Chip Select Operation section, following change is made:

The I/O address is not within the on-chip peripheral address range 0080h-00FFh. On-chip peripheral registers assume priority for all addresses where:0080h <= ADDR[15:0] <= 00FFh.

Now reads:

The I/O address is not within the on-chip peripheral address range 0000h-00FFh. On-chip peripheral registers assume priority for all addresses where:0000h <= ADDR[15:0] <= 00FFh.

Chapter: Flash Memory

The following changes were made to the Flash Memory chapter:

1. Modified Table 43: Flash Page Select Register (FLASH_PAGE = 00FCh) on page 121

   Based on this change the following sections are modified:

   (a) Page 111, under Erasing Flash Memory section

Mass Erase:

Performing a MASS ERASE operation on Flash memory erases all bits contained in Flash.

The information page remains unaffected unless the FLASH_PAGE REGISTER (0x00FCh) bit 7 (INFO_EN) is set. This self-timed operation takes approximately 200 ms to complete.

(b) Page 112, under Information Page Characteristics section, second paragraph

There are two ways to erase the information page. You must set the FLASH_PAGE REGISTER (0x00FC) bit 7 (INFO_EN) and then the user can execute a MASS ERASE operation or execute a PAGE ERASE.

(c) Page 117, under Flash Write/Erase Protection Register section, in Note

A protect bit is not available for the information page. The information page is, however, protected from a MASS ERASE by clearing the FLASH_PAGE REGISTER (0x00FC) bit 7 (INFO_EN).

(d) Page 122, under Flash Program Control Register section, second paragraph

MASS ERASE and PAGE ERASE are self-clearing functions. MASS ERASE requires approximately 200 ms to erase the full 256 KB of main Flash and the 512 byte of the information page if the FLASH_PAGE REGISTER (0x00FC) bit 7 (INFO_EN) is set. PAGE ERASE requires approximately 10 ms to erase a 2 KB page. On completion of either a MASS ERASE or PAGE ERASE, the value of each corresponding bit is reset to 0.

Chapter: Real-Time Clock

Added the following note in the Real-Time Clock Overview section:

Note: For users NOT using the RTC the following RTC signal pins should be connected as follows to avoid a 10 uA leakage within the RTC circuit block. RTC_Xin (pin 61) should be left floating or connected to ground.

Chapter: Universal Asynchronous Receiver/ Transmitter

The following changes are done in Universal Asynchronous Receiver/ Transmitter chapter:

1. On Page 196, Table 101 (UART0_FCTL = 00C2h, UART1_FCTL = 00D2h), the description is modified.
2. On Page 204, Table 108 (UART Scratch Pad Registers (UART0_SPR = 00C7h, UART1_SPR = 00D7h), the description is modified.

Chapter: On-Chip Oscillator

The following changes are done in On-Chip Oscillator chapter:

1. On Page 351 Table 231 modified to read:

   Recommended Crystal Oscillator Specifications—32 kHz Operation; Table entry Series Resistance (RS) 50 kΩ Maximum

2. On Page 349, Figure 63 — Recommended Crystal Oscillator Configuration, the value of inductance L is changed to 3.3 uH.

Chapter: Infrared Encoder/Decoder

Modified field [7:4] in Table 110 on Page 209.

Chapter: Zilog Debug Interface

The following modifications are done in Zilog Debug Interface chapter:

1. Page 291: Replaced the 3rd paragraph under the ZDI Introduction with this:

   ZDI allows reading and writing of most internal registers without disturbing the state of the machine. Reads and Writes to memory can occur as fast as the ZDI downloads and uploads data, with a maximum frequency of 0.4 times the eZ80F91system clock frequency. Also, regardless of the ZDI clock frequency, the duration of the low-phase of the ZDI clock (that is, ZCL = 0) must at least 1.25 times the system clock period.

2. Added two paragraphs to ZDI Read memory registers on page 315.

Chapter: Electrical Characteristics

In Table 234 on page 355, Minimum, Typical and Maximum values of VBO Voltage Threshold modified and added IS_{POR_VBO} parameter. Improved values of Icc Stop/Sleep current.

References

For detailed information about these changes, refer the following documents:

- eZ80Acclaim!Flash Microcontrollers eZ80F91 MCU Product Specification (PS0192)
- Errata to eZ80Acclaim! eZ80F91 (UP0061)
- eZ80Acclaim*Plus!* Connectivity ASSP eZ80F91 ASSP Product Specification (PS0270)

Warning: DO NOT USE IN LIFE SUPPORT

LIFE SUPPORT POLICY

ZILOG'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF ZILOG CORPORATION.

As used herein

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

Document Disclaimer