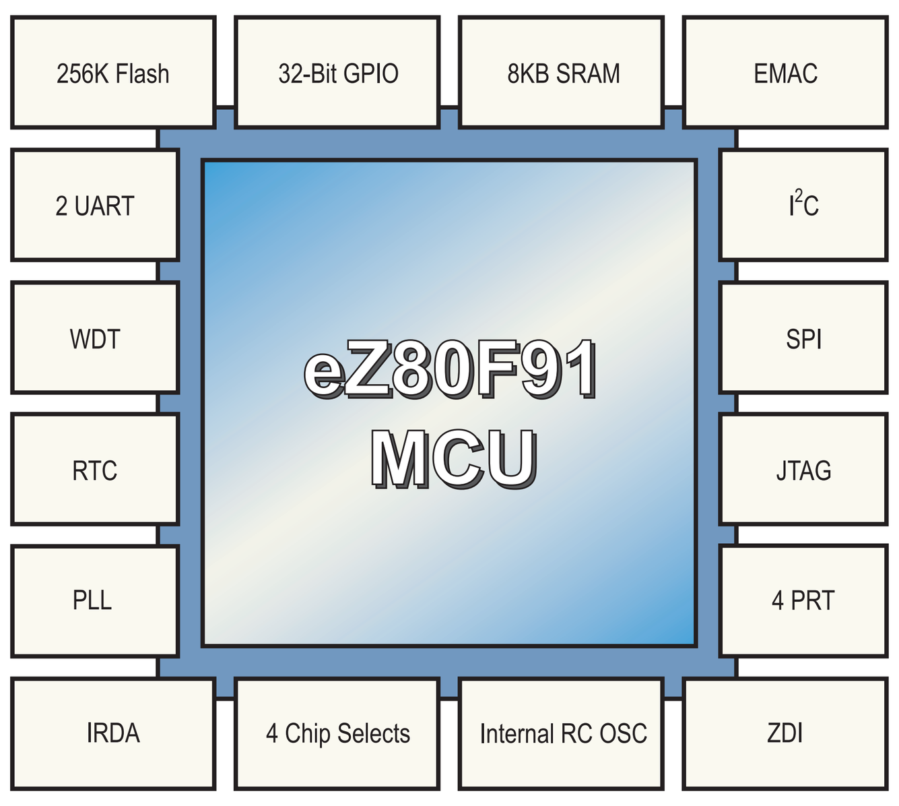
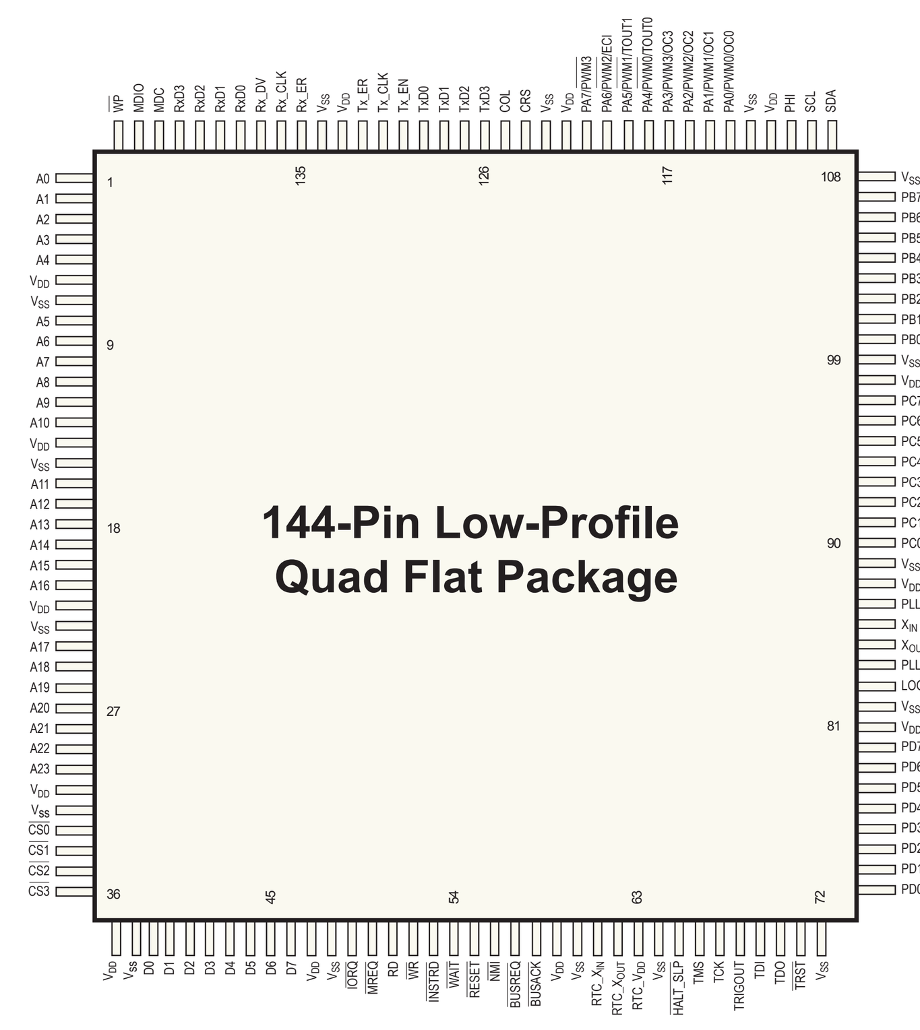
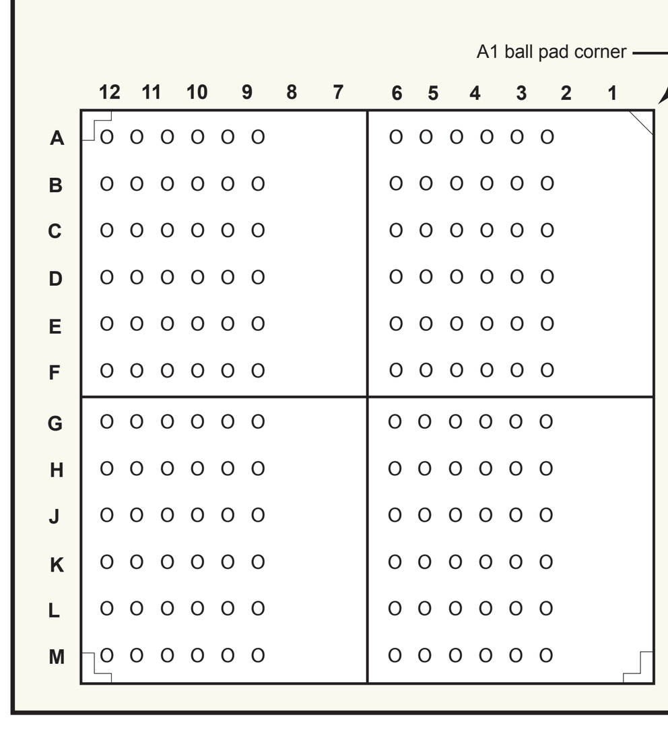
eZ80 Acclaim!® Flash Microcontrollers

eZ80F91 MCU Easy Reference Chart





144-Ball Grid Array



	12	11	10	9	8	7	6	5	4	3	2	1
A	SDA	SCL	PA0	PA4	PA7	COL	TxD0	V_{DD}	Rx_DV	MDC	WPn	A0
B	V_{SS}	PHI	PA1	PA3	V_{DD}	TxD3	Tx_EN	V_{SS}	RxD1	MDIO	A2	A1
C	PB6	PB7	V_{DD}	PA5	V_{SS}	TxD2	Tx_CLK	Rx_CLK	RxD3	A3	V_{SS}	V_{DD}
D	PB1	PB3	PB5	V_{SS}	CRS	TxD1	Rx_ER	RxD2	A4	A8	A6	A7
E	PC7	V_{DD}	PB0	PB4	PA2	Tx_ER	RxD0	A5	A11	V_{SS}	V_{DD}	A10
F	PC3	PC4	PC5	V_{SS}	PB2	PA6	A9	A17	A15	A14	A13	A12
G	V_{SS}	PC0	PC1	PC2	PC6	PLL_V_{SS}	V_{SS}	A23	A20	V_{SS}	V_{DD}	A16
H	X_{OUT}	X_{IN}	PLL_V_{DD}	V_{DD}	PD7	TMS	V_{SS}	D5	V_{SS}	A21	A19	A18
J	V_{SS}	V_{DD}	LOOP FILT_OUT	PD4	TRIGOUT	RTC_ V_{DD}	NMIn	WRn	D2	CS0n	V_{DD}	A22
K	PD5	PD6	PD3	TDI	V_{SS}	V_{DD}	RESETn	RDn	V_{DD}	D1	CS2n	CS1n
L	PD1	PD2	TRSTn	TCK	RTC XOUT	BUSACKn	WAITn	MREQn	D6	D4	D0	CS3n
M	PD0	V_{SS}	TDO	HALT_ SLPn	RTC_ XIN	BUSREQn	INSTRDn	IORQn	D7	D3	V_{SS}	V_{DD}

Chip Select Registers

Chip Select x Lower Bound Register
CS0_LBR = 00A8h, CS1_LBR = 00ABh, CS2_LBR = 00AEh, CS3_LBR = 00B1h

7:0	CSx_LBR	0 = Lower bound of the Memory Chip Select address range.* 1 = Address value of the I/O Chip Select.*

Chip Select x Upper Bound Register
CS0_UBR = 00A9h, CS1_UBR = 00AC, CS2_UBR = 00AFh, CS3_UBR = 00B2h

7:0	CSx_UBR	0 = Upper bound of the Memory Chip Select address range.* 1 = No effect.

Chip Select x Control Register
CS0_CTL = 00AAh, CS1_CTL = 00ADh, CS2_CTL = 00B0h, CS3_CTL = 00B3h

7:5	CSx_WAIT	000 = 0 wait states are asserted when this chip select is active. 001 = 1 wait state is asserted when this chip select is active. 010 = 2 wait states are asserted when this chip select is active. 011 = 3 wait states are asserted when this chip select is active. 100 = 4 wait states are asserted when this chip select is active. 101 = 5 wait states are asserted when this chip select is active. 110 = 6 wait states are asserted when this chip select is active. 111 = 7 wait states are asserted when this chip select is active.
4	CSx_IO	0 = Chip Select is configured as a Memory Select. 1 = Chip Select is configured as an I/O Chip Select.
3	CSx_EN	0 = Chip Select is disabled. 1 = Chip Select is enabled.
2:0		Reserved.

Chip Select x Bus Mode Control Register
CS0_BMC = 00F0h, CS1_BMC = 00F1h, CS2_BMC = 00F2h, CS3_BMC = 00F3h

7:6	BUS_MODE	00 = eZ80 bus mode. 01 = Z80 bus mode. 10 = Intel bus mode. 11 = Motorola bus mode.
5	AD_MUX	0 = Separate address and data. 1 = Multiplexed address and data on DATA[7:0].
4		Reserved.
3:0	BUS_CYCLE	0000 = Not valid. 0001 = Each bus mode state is 1 eZ80 clock cycle in duration.* 0010 = Each bus mode state is 2 eZ80 clock cycles in duration. 0011 = Each bus mode state is 3 eZ80 clock cycles in duration. 0100 = Each bus mode state is 4 eZ80 clock cycles in duration. 0101 = Each bus mode state is 5 eZ80 clock cycles in duration. 0110 = Each bus mode state is 6 eZ80 clock cycles in duration. 0111 = Each bus mode state is 7 eZ80 clock cycles in duration. 1000 = Each bus mode state is 8 eZ80 clock cycles in duration. 1001 = Each bus mode state is 9 eZ80 clock cycles in duration. 1010 = Each bus mode state is 10 eZ80 clock cycles in duration. 1011 = Each bus mode state is 11 eZ80 clock cycles in duration. 1100 = Each bus mode state is 12 eZ80 clock cycles in duration. 1101 = Each bus mode state is 13 eZ80 clock cycles in duration. 1110 = Each bus mode state is 14 eZ80 clock cycles in duration. 1111 = Each bus mode state is 15 eZ80 clock cycles in duration.

Real-Time Clock Registers

Real-Time Clock Seconds Register
RTC_SEC = 00E0h

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4	TEN_SEC	0Ð5 = The tens digit of the current seconds count.
3:0	SEC	0Ð9 = The ones digit of the current seconds count.
Binary Operation (BCD_EN = 0)		
7:0	SEC	00hÐ3Bh = The current seconds count.

Real-Time Clock Minutes Register
RTC_MIN = 00E1h

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4	TEN_MIN	0Ð5 = The tens digit of the current minutes count.
3:0	MIN	0Ð9 = The ones digit of the current minutes count.
Binary Operation (BCD_EN = 0)		
7:0	MIN	00hÐ3Bh = The current minutes count.

Real-Time Clock Hours Register
RTC_HRS = 00E2h

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4	TEN_HRS	0Ð2 = The tens digit of the current hours count.
3:0	HRS	0Ð9 = The ones digit of the current hours count.
Binary Operation (BCD_EN = 0)		
7:0	HRS	00hÐ17h = The current hours count.

Real-Time Clock Day-of-the-Week Register
RTC_DOW = 00E3h

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4		Reserved.
3:0	DOW	1Ð7 = The current day-of-the-week count.
Binary Operation (BCD_EN = 0)		
7:4		Reserved.
3:0	DOW	01hÐ07h = The current day-of-the-week count.

Real-Time Clock Day-of-the-Month Register
RTC_DOM = 00E4h

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4	TENS_DOM	0Ð3 = The tens digit of the current day-of-the-month count.
3:0	DOM	0Ð9 = The ones digit of the current day-of-the-month count.
Binary Operation (BCD_EN = 0)		
7:0	DOM	01hÐ1Fh = The current day-of-the-month count.

Real-Time Clock Month Register
RTC_MON = 00E5h

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4	TENS_MON	0Ð1 = The tens digit of the current month count.
3:0	MON	0Ð9 = The ones digit of the current month count.
Binary Operation (BCD_EN = 0)		
7:0	MON	01hÐ0Ch = The current month count.

Real-Time Clock Year Register
RTC_YR = 00E6h

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4	TENS_YR	0Ð9 = The tens digit of the current year count.
3:0	YR	0Ð9 = The ones digit of the current year count.
Binary Operation (BCD_EN = 0)		
7:0	YR	00hÐ63h = The current year count.

Real-Time Clock Century Register
RTC_CEN = 00E7h

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4	TENS_CEN	0Ð9 = The tens digit of the current century count.
3:0	CEN	0Ð9 = The ones digit of the current century count.
Binary Operation (BCD_EN = 0)		
7:0	CEN	00hÐ63h = The current century count.

Real-Time Clock Alarm Seconds Register
RTC_ASEC = 00E8h

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4	ATEN_SEC	0Ð5 = The tens digit of the alarm seconds value.
3:0	ASEC	0Ð9 = The ones digit of the alarm seconds value.
Binary Operation (BCD_EN = 0)		
7:0	ASEC	00hÐ3Bh = The alarm seconds value.

Real-Time Clock Alarm Minutes Register
RTC_AMIN = 00E9h

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4	ATEN_MIN	0Ð5 = The tens digit of the alarm minutes value.
3:0	AMIN	0Ð9 = The ones digit of the alarm minutes value.
Binary Operation (BCD_EN = 0)		
7:0	AMIN	00hÐ3Bh = The alarm minutes value.

Real-Time Clock Alarm Hours Register
RTC_AHRS = 00EAh

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4	ATEN_HRS	0Ð2 = The tens digit of the alarm hours value.
3:0	AHRS	0Ð9 = The ones digit of the alarm hours value.
Binary Operation (BCD_EN = 0)		
7:0	AHRS	00hÐ17h = The alarm hours value.

Real-Time Clock Alarm Day-of-the-Week Register
RTC_ADOW = 00EBh

Binary-Coded-Decimal Operation (BCD_EN = 1)		
7:4		Reserved.
3:0	ADOW	1Ð7 = The alarm day-of-the-week value.
Binary Operation (BCD_EN = 0)		
7:4		Reserved.
3:0	ADOW	01hÐ07h = The alarm day-of-the-week value.

Real-Time Clock Alarm Control Register
RTC_ACTRL = 00ECh

7:4		Reserved.
3	ADOW_EN	0 = The day-of-the-week alarm is disabled. 1 = The day-of-the-week alarm is enabled.
2	AHRS_EN	0 = The hours alarm is disabled. 1 = The hours alarm is enabled.
1	AMIN_EN	0 = The minutes alarm is disabled. 1 = The minutes alarm is enabled.
0	ASEC_EN	0 = The seconds alarm is disabled. 1 = The seconds alarm is enabled.

Real-Time Clock Control Register
RTC_CTRL = 00EDh

7	ALARM	0 = Alarm interrupt is inactive. 1 = Alarm interrupt is active.
6	INT_EN	0 = Interrupt on alarm condition is disabled. 1 = Interrupt on alarm condition is enabled.
5	BCD_EN	0 = RTC count and alarm value registers are binary. 1 = RTC count and alarm value registers are binary-coded decimal.
4	CLK_SEL	0 = RTC clock source is crystal oscillator output.* 1 = RTC clock source is power-line frequency input.*
3	FREQ_SEL	0 = Power-line frequency is 60 Hz. 1 = Power-line frequency is 50 Hz.
2	DAY_SAV	0 = Daylight Savings Time not selected. 1 = Daylight Savings Time selected.
1	SLP_WAKE	0 = RTC does not generate a sleep-mode recovery reset. 1 = RTC Alarm generates a sleep-mode recovery reset.
0	RTC_UNLOCK	0 = RTC count registers are locked to prevent write access.* 1 = RTC count registers are unlocked to allow write access.*

GPIO Registers

GPIO Mode Selection

GPIO Mode	Px_ALT2 Bits [7:0]	Px_ALT1 Bits [7:0]	Px_DDR Bits [7:0]	Px_DR Bits [7:0]	Port Mode	Output
1	0	0	0	0	Output	0
	0	0	0	1	Output	1
2	0	0	1	0	Input from pin	High impedance
	0	0	1	1	Input from pin	High impedance
3	0	1	0	0	Open-drain output	0
	0	1	0	1	Open-drain I/O	High impedance
4	0	1	1	0	Open-source I/O	High impedance
	0	1	1	1	Open-source output	1
5	1	0	0	0	Reserved	High impedance
6	1	0	0	1	InterruptÑdual edge triggered	High impedance
7	1	0	1	0	Port B, C, or DÑalternative function controls port I/O	
	1	0	1	1	Port B, C, or DÑalternative function controls port I/O	
8	1	1	0	0	InterruptÑactive Low	High impedance
	1	1	0	1	InterruptÑactive High	High impedance
9	1	1	1	0	InterruptÑfalling edge triggered	High impedance
	1	1	1	1	InterruptÑrising edge triggered	High impedance

Port x Alternate Registers 2
PA_ALT2 = 0099h, PB_ALT2 = 009Dh, PC_ALT2 = 00A1h, PD_ALT2 = 00A5h
Port x Alternate Registers 1
PA_ALT1 = 0098h, PB_ALT1 = 009Ch, PC_ALT1 = 00A0h, PD_ALT1 = 00A4h
Port x Alternate Registers 0
PA_ALT0 = 00A6h, PB_ALT0 = 00A7h, PC_ALT0 = 00CEh, PD_ALT0 = 00CFh
Port x Data Direction Registers
PA_DDR = 0097h, PB_DDR = 009Bh, PC_DDR = 009Fh, PD_DDR = 00A3h
Port x Data Registers
PA_DR = 0096h, PB_DR = 009Ah, PC_DR = 009Eh, PD_DR = 00A2h

	Px_ALT2	Px_ALT1	Px_ALT0	Px_DDR	Px_DR
7	Mode for Px7, where x = Port A, B, C, or D.				
6	Mode for Px6, where x = Port A, B, C, or D.				
5	Mode for Px5, where x = Port A, B, C, or D.				
4	Mode for Px4, where x = Port A, B, C, or D.				
3	Mode for Px3, where x = Port A, B, C, or D.				
2	Mode for Px2, where x = Port A, B, C, or D.				
1	Mode for Px1, where x = Port A, B, C, or D				
0	Mode for Px0, where x = Port A, B, C, or D.				

EMAC Registers

EMAC Test Register
EMAC_TEST = 0020h

7		Reserved.
6	TEST_FIFO	0 = FIFO test mode disabledÑnormal operation. 1 = FIFO test mode enabled.
5	TxRx_SEL	0 = Select the Receive FIFO when FIFO test mode is enabled. 1 = Select the Transmit FIFO when FIFO test mode is enabled.
4	SSTC	0 = Normal operation. 1 = Shortcut slot timer counter.*
3	SIMR	0 = Normal operation. 1 = Simulation Reset.
2	FRC_OVR_ERR	0 = Normal operation. 1 = Force overrun error in Receive FIFO.
1	FRC_UND_ERR	0 = Normal operation. 1 = Force underrun error in Transmit FIFO.
0	LPBK	0 = Normal operation. 1 = EMAC Transmit interface is looped back into EMAC Receive Interface.

EMAC Configuration Register 1
EMAC_CFG1 = 0021h

7	PADEN	0 = No padding.* 1 = EMAC pads all short frames at the end of the data field.
6	ADPADN	0 = Disable auto detection. 1 = Enable frame detection.*
5	VLPAD	0 = Do not pad all short frames. 1 = EMAC pads all short frames to 64 bytes and append a valid CRC.
4	CRCEN	0 = Do not append CRC. 1 = Append CRC to every frame regardless of padding options.
3	FULLD	0 = Half-duplex mode, CSMA/CD enabled.* 1 = Enable full duplex mode, CSMA/CD disabled.*
2	FLCHK	0 = Ignore the length field within Transmit/Receive frames. 1 = Transmit Receive frame lengths compared to the length/type field.*
1	HUGEN	0 = Limit the Receive frame size to the number of bytes specified.* 1 = Allow unlimited-sized frames to be received.
0	DCRCC	0 = No proprietary header.* 1 = Proprietary header exists on the front of IEEE 802.3 frames.

EMAC Configuration Register 2
EMAC_CFG2 = 0022h

7	BPNB	0 = Use normal back-off algorithm prior to transmitting packet.* 1 = EMAC immediately retransmits the packet without back-off.*
6	NOBO	0 = Enable exponential back-off. 1 = EMAC immediately retransmits following a collision.*
5:0	LCOL	00hÐ3Fh: Sets the number of bytes after Start Frame Delimiter.*

EMAC Configuration Register 3
EMAC_CFG3 = 0023h

7	LONGP	0 = Any preamble length allowed.* 1 = Only Receive packets with preamble fields of 12 bytes or less allowed.
6	PUREP	0 = No preamble error checking performed. 1 = EMAC verifies the content of the preamble.*
5	XSDFR	0 = EMAC aborts when excessive deferral limit is reached. 1 = EMAC defers to the carrier indefinitely.*
4	BITMD	0 = Disable 10 Mbps ENDEC mode. 1 = Enable 10 Mbps ENDEC mode.
3:0	RETRY	0hÐFh: Number of retransmission attempts following a collision.*

EMAC Configuration Register 4
EMAC_CFG4= 0024h

7		Reserved.
6	TPCF	0 = Do not transmit a pause control frame. 1 = Transmit pause control frame.*
5	THDF	0 = Disable back pressure. 1 = EMAC asserts back pressure on the link.*
4	PARF	0 = Only accept frames that meet preset criteria.* 1 = All frames are received.*
3	RxFC	0 = EMAC ignores received pause control frames. 1 = EMAC acts upon pause control frames received.
2	TxFC	0 = Pause control frames are not allowed to be transmitted. 1 = Pause control frames are allowed to be transmitted.
1	TPAUSE	0 = Do not force a pause condition. 1 = Force a pause condition while this bit is asserted.
0	RxEN	0 = Do not receive frames. 1 = Allow Receive frames to be received.

EMAC Station Address Registers
EMAC_STAD_0 = 0025h, EMAC_STAD_1 = 0026h, EMAC_STAD_2 = 0027h, EMAC_STAD_3 = 0028h, EMAC_STAD_4 = 0029h, EMAC_STAD_5 = 002Ah

7:0	EMAC_STAD_x	00hÐFFh: This 48-bit station address comprises { EMAC_STAD_5 [7:0] = STAD [47:40], ÊÊ EMAC_STAD_4 [7:0] = STAD [39:32], ÊÊ EMAC_STAD_3 [7:0] = STAD [31:24], ÊÊ EMAC_STAD_2 [7:0] = STAD [23:16], ÊÊ EMAC_STAD_1 [7:0] = STAD [15:8], ÊÊ EMAC_STAD_0 [7:0] = STAD [7:0]}

EMAC Transmit Pause Timer Value RegistersÑLow and High Bytes
EMAC_TPTV_L = 002Bh, EMAC_TPTV_H = 002Ch

7:0	EMAC_TPTV_x	00hÐFFh: The 16-bit value, {EMAC_TPTV_H, EMAC_TPTV_L}, is inserted into outgoing pause control frames.*

EMAC Interpacket Gap Register
EMAC_IPGT = 002Dh

7		Reserved.
6:0	IPGT	00hÐ7Fh: The number of octets of IPG.

EMAC Non-Back-To-Back IPG RegisterÑPart 1
EMAC_IPGR1 = 002Eh

7		Reserved.
6:0	IPGR1	00hÐ7Fh: The optional carrier sense window value.*

EMAC Non-Back-To-Back IPG RegisterÑPart 2
EMAC_IPGR2 = 002Fh

7		Reserved.
6:0	IPGR2	00hÐ7Fh: The non-back-to-back interpacket gap.

EMAC Maximum Frame Length RegistersÑLow and High Bytes
EMAC_MAXF_L = 0030h, EMAC_MAXF_H = 0031h

7:0	EMAC_MAXF_x	0000hÐFFFFh: The Low/High byte of the 2-byte MAXF value {EMAC_MAXF_L [7:0] = MAXF [7:0], EMAC_MAXF_H [7:0] = MAXF [15:8]}

EMAC Address Filter Register
EMAC_AFR = 0032h

7:4		Reserved.
3	PROM	1 = Enable Promiscuous mode and disable station address filtering.* 0 = Disable Promiscuous mode.
2	MC	1 = Accept any multicast message.* 0 = Do not accept multicast messages of any type.
1	QMC	1 = Accept only qualified multicast messages.* 0 = Do not accept qualified multicast messages.
0	BC	1 = Accept broadcast messages.* 0 = Do not accept broadcast messages.

EMAC Hash Table Registers
EMAC_HTBL_0 = 0033h, EMAC_HTBL_1 = 0034h, EMAC_HTBL_2 = 0035h, EMAC_HTBL_3 = 0036h, EMAC_HTBL_4 = 0037h, EMAC_HTBL_5 = 0038h, EMAC_HTBL_6 = 0039h, EMAC_HTBL_7 = 003Ah

7:0	EMAC_HTBL_x	00hÐFFh: 64 bit hash table = {EMAC_HTBL_7, EMAC_HTBL_6, EMAC_HTBL_5, EMAC_HTBL_4, EMAC_HTBL_3, EMAC_HTBL_2, EMAC_HTBL_1, EMAC_HTBL_0}*

EMAC MII Management Register
EMAC_MIIMGT = 003Bh

7	LCTLD	1 = Rising edge causes the CTLD control data to be transmitted* 0 = No operation.
6	RSTAT	1 = Rising edge causes status to be read from external PHY.* 0 = No operation.
5	SCINC	1 = Scan PHY address increments upon SCAN cycle.* 0 = Normal operation.
4	SCAN	1 = Perform continuous Read cycles via MII management.* 0 = Normal operation.
3	SPRE	1 = Suppress MDO preamble. 0 = Normal preamble.
2:0	CLKS	000 MDC = SCLKÊÕÊ4 100 MDC = SCLKÊÕÊ10 001 MDC = SCLKÊÕÊ4 101 MDC = SCLKÊÕÊ14 010 MDC = SCLKÊÕÊ6 110 MDC = SCLKÊÕÊ20 011 MDC = SCLKÊÕÊ8 111 MDC = SCLKÊÕÊ28

EMAC PHY Configuration Data RegisterÑLow and High Bytes
EMAC_CTLD_L = 003Ch, EMAC_CTLD_H = 003Dh

7:0	EMAC_CTLD_x	00hÐFFh: Low/High byte of the 2-byte PHY configuration data value {EMAC_CTLD_H, EMAC_CTLD_L}.*

EMAC PHY Address Register
EMAC_RGAD= 003Eh

7:5		Reserved.
4:0	RGAD	00hÐ1Fh: 5-bit address of external PHY unit registers.

EMAC PHY Unit Select Address Register
EMAC_FIAD = 003Fh

7:5		Reserved.
4:0	FIAD	00hÐ1Fh: 5-bit address of external PHY unit.

EMAC Transmit Polling Timer Register
EMAC_PTMR = 0040h

7:0	EMAC_PTMR	00hÐFFh: The Transmit polling period in units of SYSCLKÊÕÊ256. 00 = Disables Transmit polling timer.

EMAC Reset Control Register
EMAC_RST = 0041h

7:6		Reserved.
5	SRST	1 = Software reset active.* 0 = Normal operation.
4	HRTFN	1 = Reset transmit function. 0 = Normal operation.
3	HRRFN	1 = Reset receive function. 0 = Normal operation.
2	HRTMC	1 = Reset EMAC transmit control function. 0 = Normal operation.
1	HRRMC	1 = Reset EMAC receive control function. 0 = Normal operation.
0	HRMGT	1 = Reset EMAC management function. 0 = Normal operation.

EMAC Transmit Lower Boundary Pointer RegistersÑLow and High Bytes
EMAC_TLBP_L = 0042h, EMAC_TLBP_H = 0043h*

7:0	EMAC_TLBP_x	0000hÐFFFFh: EMAC_TLBP_H = TLBP [15:8] EMAC_TLBP_L = TLBP [7:0]

EMAC Boundary Pointer RegistersÑLow, High, and Upper Bytes
EMAC_BP_L = 0044h, EMAC_BP_H = 0045h, EMAC_BP_U = 0046h

7:0	EMAC_BP_x	0000hÐFFFFh: EMAC_BP_U = BP [23:16] EMAC_BP_H = BP [15:8] EMAC_BP_L = BP [7:0]

EMAC Receive High Boundary Pointer RegistersÑLow and High Bytes
EMAC_RHBP_L = 0047h, EMAC_RHBP_H = 0048h

7:0	EMAC_RHBP_x	00hÐFFh: These bits represent the Low/High byte of the 2-byte EMAC Receive High Boundary Pointer value {EMAC_RHBP_H, EMAC_BRHP_L}.*

EMAC Receive Read Pointer RegistersÑLow and High Bytes
EMAC_RRP_L = 0049h, EMAC_RRP_H = 004Ah

7:0	EMAC_RRP_x	0000hÐFFFFh: EMAC_RRP_H = RRP [15:8] EMAC_?RRP_L = RRP [7:0]

EMAC Buffer Size Register
EMAC_BUFSZ = 004Bh

7:6	BUFSZ	00 = Set EMAC Rx/Tx buffer size to 256 bytes. 01 = Set EMAC Rx/Tx buffer size to 128 bytes. 10 = Set EMAC Rx/Tx buffer size to 64 bytes. 11 = Set EMAC Rx/Tx buffer size to 32 bytes.
5:0	TPCF_LEV	00 = Disable Transmit Pause Control Frame generation.* 01 = Transmit Pause Control Frame level.*

EMAC Interrupt Enable Register
EMAC_IEN = 004Ch

7	TxFSMERR	1 = Enable Transmit State Machine error interrupt.* 0 = Disable Transmit State Machine error interrupt.*
6	MGTDONE	1 = Enable MII Management Done interrupt.* 0 = Disable MII M anagement Done interrupt.*
5	Rx_CF	1 = Enable Receive Control Frame interrupt.* 0 = Disable Receive Control Frame interrupt.*
4	Rx_PCF	1 = Enable Receive Pause Control Frame interrupt.* 0 = Disable Receive Pause Control Frame interrupt.*
3	Rx_DONE	1 = Enable Receive Done interrupt.* 0 = Disable Receive Done interrupt.*
2	Rx_OVR	1 = Enable Receive Overrun interrupt.* 0 = Disable Receive Overrun interrupt.*
1	Tx_CF	1 = Enable Transmit Control Frame interrupt.* 0 = Disable Transmit Control Frame interrupt.*
0	Tx_DONE	1 = Enable Transmit Done interrupt.* 0 = Disable Transmit Done interrupt.*

EMAC Interrupt Status Register
EMAC_ISTAT = 004Dh

7	TxFSMERR_STAT	1 = Internal error occurred in the EMAC Transmit path.* 0 = Normal operation.*
6	MGTDONE_STAT	1 = MII Mgmt. interrupt has completed a Read or Write access to PHY.* 0 = MII Mgmt. did not occur.
5	Rx_CF_STAT	1 = Receive Control Frame interrupt occurred.* 0 = Receive Control Frame interrupt did not occur.
4	Rx_PCF_STAT	1 = Receive Pause Control Frame interrupt occurred.* 0 = Receive Pause Control Frame interrupt did not occur.*
3	Rx_DONE_STAT	1 = Receive Done interrupt occurred.* 0 = Receive Done interrupt did not occur.*
2	Rx_OVR_STAT	1 = Receive Overrun interrupt occurred.* 0 = Receive Overrun interrupt did not occur.*
1	Tx_CF_STAT	1 = Transmit Control Frame interrupt occurred.* 0 = Transmit Control Frame interrupt did not occur.*
0	Tx_DONE_STAT	1 = Transmit Done interrupt occurred.* 0 = Transmit Done interrupt did not occur.*

Ê Note: Write a 1 to clear bit.

EMAC PHY Read Status Data RegistersÑLow and High Bytes
EMAC_PRSD_L = 004Eh, EMAC_PRSD_H = 004Fh

7:0	EMAC_PRSD_x	0000hÐFFFFh: EMAC_PRSD_H = PRSD [15:8] EMAC_PRSD_L = PRSD [7:0]

EMAC MII Status Register
EMAC_MIISTAT = 0050h

7	BUSY	1 = MII management operation in progressÑBusy.* 0 = Not busy.
6	MIILF	1 = Local copy of PHY Link fail bit. 0 = PHY Link OK.
5	NVALID	1 = MII Scan result is not valid Emac_PRSD is invalid. 0 = Emac_PRSD is valid.
4:0	RDADR	00hÐ1Fh: Denotes PHY addressed in current scan cycle.

EMAC Receive Write Pointer RegistersÑLow and High Bytes
EMAC_RWP_L = 0051h, EMAC_RWP_H = 0052h

7:0	EMAC_RWP_x	0000hÐ1FE0h: EMAC_RWP_H = RWP [15:8] EMAC_RWP_L = RWP [7:0]

EMAC Transmit Read Pointer RegistersÑLow and High Bytes
EMAC_TRP_L = 0053h, EMAC_TRP_H = 0054h

7:0	EMAC_TRP_x	0000hÐ1FE0h: EMAC_TRP_H = TRP [15:8] EMAC_TRP_L = TRP [7:0]

EMAC Receive Blocks Left RegistersÑLow and High Bytes
EMAC_BLKSLFT_L = 0055h, EMAC_BLKSLFT_H = 0056h

7:0	EMAC_BLKSLFT_x	0000hÐFFFFh: EMAC_BLKSLFT_H = RBL [15:8] EMAC_BLKSLFT_L = RBL [7:0]

EMAC FIFO Data RegisterÑLow and High Bytes
EMAC_FDATA_L = 0057h, EMAC_FDATA_H = 0058h

7:0	EMAC_FDATA_x	0000hÐ03FFh: EMAC_FDATA_H[1:0] = FD [9:8] EMAC_FDATA_L = FD [7:0]

EMAC FIFO Flags Register
EMAC_FFLAGS = 0059h

7	TFF	1 = Transmit FIFO full. 0 = Transmit FIFO not full.
6		Reserved.
5	TFAE	1 = Transmit FIFO almost empty. 0 = Transmit FIFO not almost empty.
4	TFE	1 = Transmit FIFO empty. 0 = Transmit FIFO not empty.
3	RFF	1 = Receive FIFO full. 0 = Receive FIFO not full.
2	RFAF	1 = Receive FIFO almost full. 0 = Receive FIFO not almost full.
1	RFAE	1 = Receive FIFO almost empty. 0 = Receive FIFO not almost empty.
0	RFE	1 = Receive FIFO empty. 0 = Receive FIFO not empty.

RAM Control Registers

RAM Control Register
RAM_CTL = 00B4h

7	GPRAM_EN	0 = On-chip general-purpose RAM is disabled. 1 = On-chip general-purpose RAM is enabled.
6	ERAM_EN	0 = On-chip EMAC RAM is disabled. 1 = On-chip EMAC RAM is enabled.
5:0		Reserved.

RAM Address Upper Byte Register
RAM_ADDR_U = 00B5h

7:0	RAM_ADDR_U	00hÐFFh: This byte define the upper byte of the RAM address.*

MBIST Control Register
MBIST_GPR = 00B6h, MBIST_EMR = 00B7h

7	MBIST_ON	0 = MBIST Testing of the RAM is disabled. 1 = MBIST Testing of the RAM is enabled.
6	MBIST_DONE	0 = MBIST Testing has not completed. 1 = MBIST Testing has completed.
5	MBIST_PASS	0 = MBIST Testing has failed. 1 = MBIST Testing has passed.
4:0		Reserved.

Power-Down Registers

Clock Peripheral Power-Down Register 1
CLK_PPD1 = 00DBh

7	GPIO_D_OFF	0 = System clock to GPIO Port D is powered down.* 1 = System clock to GPIO Port D is powered up.
6	GPIO_C_OFF	0 = System clock to GPIO Port C is powered down.* 1 = System clock to GPIO Port C is powered up.
5	GPIO_B_OFF	0 = System clock to GPIO Port B is powered down.* 1 = System clock to GPIO Port B is powered up.
4	GPIO_A_OFF	0 = System clock to GPIO Port A is powered down.* 1 = System clock to GPIO Port A is powered up.
3	SPI_OFF	0 = System clock to SPI is powered down. 1 = System clock to SPI is powered up.
2	I2C_OFF	0 = System clock to I^{2}C is powered down. 1 = System clock to I^{2}C is powered up.
1	UART1_OFF	0 = System clock to UART1 is powered down. 1 = System clock to UART1 is powered up.
0	UART0_OFF	0 = System clock to UART0 is powered down. 1 = System clock to UART0 is powered up.

Clock Peripheral Power-Down Register 2
CLK_PPD2 = 00DCh

7	PHI_OFF	0 = PHI clock output is enabled. 1 = PHI clock output is disabled.*
6	VBO_OFF	0=VBO detection circuit is enabled 1=VBO detection circuit is disabled
5:4		Reserved.
3	TIMER2_OFF	0 = System clock to TIMER2 is powered down. 1 = System clock to TIMER2 is powered up.
2	TIMER1_OFF	0 = System clock to TIMER1 is powered down. 1 = System clock to TIMER1 is powered up.
1	TIMER0_OFF	0 = System clock to TIMER0 is powered down. 1 = System clock to TIMER0 is powered up.
0	TIMER0_OFF	0 = System clock to TIMER0 is powered down. 1 = System clock to TIMER0 is powered up.

UART Control Registers

UART Baud Rate Generator RegistersÑLow Byte
UART0_BRG_L = 00C0h, UART1_BRG_L = 00D0h

7:0	UARTx_BRG_L	00hÐFFh: These bits represent the Low byte of the 16-bit Baud Rate Generator divider value.*

UART Baud Rate Generator RegistersÑHigh Byte
UART0_BRG_H = 00C1h, UART1_BRG_H = 00D1h

7:0	UARTx_BRG_H	00hÐFFh: These bits represent the High byte of the16-bit Baud Rate Generator divider value.*

UART Transmit Holding Registers
UART0_THR = 00C0h, UART1_THR = 00D0h

7:0	TxD	Transmit data byte.

UART Receive Buffer Registers
UART0_RBR = 00C0h, UART1_RBR = 00D0h

7:0	RxD	Receive data byte.

UART Interrupt Enable Registers
UART0_IER = 00C1h, UART1_IER = 00D1h

7:5		Reserved.
4	TCIE	0 = Transmission complete interrupt is disabled. 1 = Transmission complete interrupt is generated.*
3	MIIE	0 = Modem interrupt on edge detect of status inputs disabled. 1 = Modem interrupt on edge detect of status inputs enabled.
2	LSIE	0 = Line status interrupt is disabled. 1 = Line status interrupt is enabled.*
1	TIE	0 = Transmit interrupt is disabled. 1 = Transmit interrupt is enabled.*
0	RIE	0 = Receive interrupt is disabled. 1 = Receive interrupt is enabled.*

UART Interrupt Identification Registers
UART0_IIR = 00C2h, UART1_IIR = 00D2h

7:6	FSTS	00 = FIFO is disabled. 10 = Receive FIFO is disabled. 1 = FIFO is enabled.
5:4		Reserved.
3:1	INSTS	000Ð110: The Interrupt Status Code indicated in these three bits is valid only if INTBIT is 1.*
0	INTBIT	0 = An active interrupt source exists within the UART. 1 = No active interrupt source exists within the UART.

UART FIFO Control Registers
UART0_FCTL = 00C2h, UART1_FCTL = 00D2h

7:6	TRIG	00 = Receive FIFO trigger level is set to 1.* 01 = Receive FIFO trigger level is set to 4.* 10 = Receive FIFO trigger level is set to 8.* 11 = Receive FIFO trigger level is set to 14.*
5:3		ReservedÑmust be 000b.
2	CLRTxF	0 = Transmit disable. 1 = Transmit enable.
1	CLRRxF	0 = Receive disable. 1 = Receive enable.
0	FIFOEN	0 = Transmit and receive FIFOs are disabled.* 1 = Transmit and receive FIFOs are enabled.

UART Line Control Registers
UART0_LCTL = 00C3h, UART1_LCTL = 00D3h

7	DLAB	0 = Access to UARTs is enabled.* 1 = Access to Baud Rate Generators is enabled.*
6	SB	0 = Do not send a BREAK signal. 1 = Send a BREAK signal.*
5	FPE	0 = Do not force a parity error. 1 = Force a parity error.*
4	EPS	0 = Use odd parity for transmission.* 1 = Use even parity for transmission.*
3	PEN	0 = Parity bit transmit and receive is disabled. 1 = Parity bit transmit and receive is enabled.*
2:0	CHAR	000Ð111: UART character parameter selection.*

UART Modem Control Registers
UART0_MCTL = 00C4h, UART1_MCTL = 00D4h

7		Reserved.
6	POLARITY	0 = TxD and RxD signalsÑnormal polarity. 1 = Invert polarity of TxD and RxD signals.
5	MDM	0 = Multidrop mode disabled. 1 = Multidrop mode enabled.*
4	LOOP	0 = LOOP BACK mode is disabled. 1 = LOOP BACK mode is enabled.*
3	OUT2	0Ð1: No function in normal operation.*
2	OUT1	0Ð1: No function in normal operation.*
1	RTS	0Ð1: Request to send.*
0	DTR	0Ð1: Data terminal ready.*

UART Line Status Registers
UART0_LSR = 00C5h, UART1_LSR = 00D5h

7	ERR	0 = Always 0 when operating with FIFO disabled.* 1 = Error detected in the FIFO.*
6	TEMT	0 = THR/FIFO or SPI_TSR not empty, or transmitter not idle. 1 = Parity bit transmit and receive is enabled.*
5	THRE	0 = THR/FIFO is not empty. 1 = THR/FIFO is empty.*
4	BI	0 = Receiver does not detect a BREAK condition.* 1 = Receiver detects a BREAK condition.*
3	FE	0 = No framing error detected.* 1 = Framing error detected.*
2	PE	0 = Received character does not contain a parity error.* 1 = Received character contains a parity error.*
1	OE	0 = Received character does not contain an overrun error.* 1 = Overrun error is detected.*
0	DR	0 = Reset to 0 when UARTx_RBR register is read.* 1 = Data ready.*

UART Modem Status Registers
UART0_MSR = 00C6h, UART1_MSR = 00D6h

7	DCD	0Ð1: Data Carrier Detect.*
6	RI	0Ð1: Ring Indicator.*
5	DSR	0Ð1: Data Set Ready.*
4	CTS	0Ð1: Clear To Send.*
3	DDCD	0Ð1: Delta status change of Data Carrier Detect.*
2	TERI	0Ð1: Trailing Edge change on Ring Indicator.*
1	DDSR	0Ð1: Delta status change of Data Set Ready.*
0	DCTS	0Ð1: Delta status change of Clear To Send.*

UART Scratch Pad Registers
UART0_SPR = 00C7h, UART1_SPR = 00D7h

7:0	SPR	00hÐFFh: UART scratch pad register is available for use as a general-purpose Read/Write register. In multi-drop 9 bit mode, this register is used to store the address value.

Watch-Dog Timer Registers

Watch-Dog Timer Control Register
WDT_CTL = 0093h

7	WDT_EN	0 = WDT is disabled. 1 = WDT is enabled.*
6	NMI_OUT	0 = WDT time-out resets the eZ80 CPU. 1 = WDT time-out generates a NMI to the CPU.
5	RST_FLAG	0 = RESET caused by external full-chip reset or ZDI reset. 1 = RESET caused by WDT time-out.*
4	NMI_FLAG	0 = NMI caused by external source. 1 = NMI caused by WDT time-out.*
3:2	WDT_CLK	00 = WDT clock source is system clock. 01 = WDT clock source is Real-Time Clock source*. 10 = WDT clock source is internal RC oscillator. 11 = Reserved.
1:0	WDT_PERIOD	00 = WDT time-out period is 2^{27} clock cycles. 01 = WDT time-out period is 2^{25} clock cycles. 10 = WDT time-out period is 2^{22} clock cycles. 11 = WDT time-out period is 2^{18} clock cycles.

Watch-Dog Timer Reset Register
WDT_RR = 0094h

7:0	WDT_RR	A5h = The first Write value required to reset the WDT prior to a time-out. 5Ah = The second Write value required to reset the WDT prior to a time-out.*

PLL Registers

PLL Divider RegisterÑLow Bytes
PLL_DIV_L = 005Ch

7:0	PLL_DIV_L	00hÐFFh: These bits represent the Low byte of the 11-bit PLL divider value.*

PLL Divider RegisterÑHigh Byte
PLL_DIV_H = 005Dh

7:3		Reserved.
2:0	PLL_DIV_H	0hÐ7h: These bits represent the High byte of the 11-bit PLL divider value.*

PLL Control Register 0
PLL_CTL0 = 005Eh

7:6	CHRP_CTL1	00 = Charge pump current = 100 µA. 01 = Charge pump current = 500 µA. 10 = Charge pump current = 1.0 mA. 11 = Charge pump current = 1.5 mA.
5:4		Reserved.
3:2	LDS_CTL1	00 = Lock criteriaÑ8 consecutive cycles of 20ns. 01 = Lock criteriaÑ16 consecutive cycles of 20ns. 10 = Lock criteriaÑ8 consecutive cycles of 400ns. 11 = Lock criteriaÑ16 consecutive cycles of 400ns.
1:0	CLK_MUX	00 = System clock source is the external crystal oscillator. 01 = System clock source is the PLL.* 10 = System clock source if the Real-Time Clock crystal oscillator. 11 = Reserved.*

PLL Control Register 1
PLL_CTL = 005Fh

7:6		Reserved.
5	LCK_STATUS	0 = PLL is currently out of lock. 1 = PLL is currently locked.
4	INT_LOCK	0 = Lock signal from PLL has not risen since last read.* 1 = Interrupt generated when PLL enters lock mode.*
3	INT_UNLOCK	0 = Lock signal from PLL has not fallen since last read.* 1 = Interrupt generated when PLL goes out of lock mode.*
2	INT_LOCK_EN	0 = Interrupt generation for PLL locked condition is disabled.* 1 = Interrupt generation for PLL locked condition is enabled.*
1	INT_UNLOCK_EN	0 = Interrupt generation for PLL unlocked condition is disabled.* 1 = Interrupt generation for PLL unlocked condition is enabled.*
0	PLL_ENABLE	0 = PLL is disabled.* 1 = PLL is enabled.

Flash Control Registers

Flash Key Register
FLASH_KEY = 00F5h

7:0	FLASH_KEY	B6h,49h: Sequential Write with the values B6h, 49h to this register will unlock the Flash.

Flash Data Register
FLASH_DATA = 00F6h

7:0	FLASH_DATA	00hÐFFh: Data value to write to Flash memory, or the data value that is read from Flash memory.

Flash Address Upper Byte Register
FLASH_ADDR_U = 00F7h

7:2	FLASH_ADDR_U	00hÐFCh: These bits define the upper byte of the Flash address.*
1:0		Reserved.*

Flash Control Register
FLASH_CTRL = 00F8h

7:5	FLASH_WAIT	000 = 0 wait states are inserted when Flash is active. 001 = 1 wait states are inserted when Flash is active. 010 = 2 wait states are inserted when Flash is active. 011 = 3 wait states are inserted when Flash is active. 100 = 4 wait states are inserted when Flash is active. 101 = 5 wait states are inserted when Flash is active. 110 = 6 wait states are inserted when Flash is active. 111 = 7 wait states are inserted when Flash is active.
4		Reserved.
3	FLASH_EN	0 = Flash memory access is disabled. 1 = Flash memory access is enabled.
2:0		Reserved.

Flash Frequency Divider Register
FLASH_FDIV = 00F9h

7:0	FLASH_FDIV	01hÐFFh: Divider value for generating the required 5.1Ð6.5µs Flash controller clock period.

Flash Write/Erase Protection Register
FLASH_PROT = 00FAh

7	BLK7_PROT	0 = Disable Write/Erase Protect on block 38000h to 3FFFFh. 1 = Enable Write/Erase Protect on block 38000h to 3FFFFh.
6	BLK6_PROT	0 = Disable Write/Erase Protect on block 30000h to 37FFFh. 1 = Enable Write/Erase Protect on block 30000h to 37FFFh.
5	BLK5_PROT	0 = Disable Write/Erase Protect on block 28000h to 2FFFFh. 1 = Enable Write/Erase Protect on block 28000h to 2FFFFh.
4	BLK4_PROT	0 = Disable Write/Erase Protect on block 20000h to 27FFFh. 1 = Enable Write/Erase Protect on block 20000h to 27FFFh.
3	BLK3_PROT	0 = Disable Write/Erase Protect on block 18000h to 1FFFFh. 1 = Enable Write/Erase Protect on block 18000h to 1FFFFh.
2	BLK2_PROT	0 = Disable Write/Erase Protect on block 10000h to 17FFFh. 1 = Enable Write/Erase Protect on block 10000h to 17FFFh.
1	BLK1_PROT	0 = Disable Write/Erase Protect on block 08000h to 0FFFFh. 1 = Enable Write/Erase Protect on block 08000h to 0FFFFh.
0	BLK0_PROT	0 = Disable Write/Erase Protect on block 00000h to 07FFFh. 1 = Enable Write/Erase Protect on block 00000h to 07FFFh.

Flash Interrupt Control Register
FLASH_IRQ = 00FBh

7	DONE_IEN	0 = Flash Erase/Row Program Done Interrupt is disabled. 1 = Flash Erase/Row Program Done Interrupt is enabled.
6	ERR_IEN	0 = Error Condition Interrupt is disabled. 1 = Error Condition Interrupt is enabled.
5	DONE	0 = Erase/Row Program Done Flag is not set. 1 = Erase/Row Program Done Flag is set.
4		Reserved.
3	WR_VIO	0 = Write Violation Error Flag is not set. 1 = Write Violation Error Flag is set.
2	RP_TMO	0 = Row Program Time-Out Error Flag is not set. 1 = Row Program Time-Out Error Flag is set.
1	PG_VIO	0 = Page Erase Violation Error Flag is not set. 1 = Page Erase Violation Error Flag is set.
0	MASS_VIO	0 = Mass Erase Violation Error Flag is not set. 1 = Mass Erase Violation Error Flag is set.

Flash Page Select Register
FLASH_PAGE = 00FCh

7	INFO_EN	0 = Flash I/O access to main Flash memory. 1 = Flash I/O access to the information page.*
6:0	FLASH_PAGE	00h-7Fh: Page address of Flash memory to be used during the PAGE ERASE or I/O access of main Flash memory.*

Flash Row Select Register
FLASH_ROW = 00FDh

7:3		Reserved.
2:0	FLASH_ROW	0hÐ7h: Row address of Flash memory to be used during an I/O access of Flash memory.*

Flash Column Select Register
FLASH_COL = 00FEh

7:0	FLASH_COL	00hÐFFh: Column address of Flash memory to be used during an I/O access of Flash memory.

Flash Program Control Register
FLASH_PGCTL = 00FFh

7:3		Reserved.
2	ROW_PGM	0 = Row Program Disable or Row Program completed. 1 = Row Program Enable.*
1	PG_ERASE	0 = Page Erase Disable.* 1 = Page Erase Enable.*
0	MASS_ERASE	0 = Mass Erase Disable.* 1 = Mass Erase Enable.*

I^{2}C Registers

I^{2}C Slave Address Register
I2C_SAR = 00C8h

7:1	SLA	00hÐ7Fh: 7-bit slave address or upper 2 bits of address when operating in 10-bit mode.
0	GCE	0 = I^{2}C not enabled to recognize the General Call Address. 1 = I^{2}C enabled to recognize the General Call Address.

I^{2}C Extended Slave Address Register
I2C_XSAR = 00C9h

7:0	SLAX	00hÐFFh: Least significant 8 bits of the 10-bit extended slave address.

I^{2}C Data Register
I2C_DR = 00CAh

7:0	DATA	00hÐFFh: I^{2}C data byte.

I^{2}C Control Register
I2C_CTL = 00CBh

7	IEN	0 = I^{2}C interrupt is disabled. 1 = I^{2}C interrupt is enabled.
6	ENAB	0 = The I^{2}C bus is disabled and all inputs are ignored. 1 = The I^{2}C bus is enabled.*
5	STA	0 = A master mode START condition is sent. 1 = A master mode start-transmit condition on the bus.
4	STP	0 = A master mode STOP condition is sent. 1 = A master mode stop-transmit condition on the bus.
3	IFLG	0 = The I^{2}C interrupt flag is not set. 1 = The I^{2}C interrupt flag is set.
2	AAK	0 = Not Acknowledge. 1 = Acknowledge.
1:0		Reserved.

I^{2}C Status Register
I2C_SR = 00CCh

7:3	STAT	00000Ð11111: 5-bit I^{2}C status code.
2:0		Reserved.

I^{2}C Clock Control Register
I2C_CCR = 00CCh

7		Reserved.
6:3	M	0000Ð1111: I^{2}C clock divider scalar value.
2:0	N	000Ð111: I^{2}C clock divider exponent.

I^{2}C Software Reset Register
I2C_SRR = 00CDh

7:0	SRR	00hÐFFh: Writing any value to this register performs a software reset of the I^{2}C module.

Timer Registers

Timer Control Register
TMR0_CTL = 0060h, TMR1_CTL = 0065h, TMR2_CTL = 006Fh, TMR3_CTL = 0074h

7	BRK_STOP	0 = Timer continues operating during debug break points. 1 = Timer stops operating and holds count value at breakpoint.
6:5	CLK_SEL	00 = Timer source is the system clock divided by the prescaler. 01 = Timer source is the Real Time Clock Input. 10 = Timer source is the Event Count (ECx) inputÑfalling edge.* 11 = Timer source is the Event Count (ECx) inputÑrising edge.*
4:3	CLK_DIV	00 = System clock divider = 4. 01 = System clock divider = 16. 10 = System clock divider = 64. 11 = System clock divider = 256.
2	TIM_CONT	0 = Timer operates in SINGLE PASS mode.* 1 = Timer operates in CONTINUOUS mode.*
1	RLD	0 = Reload function is not forced. 1 = Force reload.*
0	TIM_EN	0 = Programmable reload timer is disabled. 1 = Programmable reload timer is enabled.

Timer Interrupt Enable Register
TMR0_IER = 0061h, TMR1_IER = 0066h, TMR2_IER = 0070h, TMR3_IER = 0075h

7		Unused.
6	IRQ_OC3_EN	0 = Interrupt requests for OC3 are disabled.* 1 = Interrupt requests for OC3 are enabled.*
5	IRQ_OC2_EN	0 = Interrupt requests for OC2 are disabled.* 1 = Interrupt requests for OC2 are enabled.*
4	IRQ_OC1_EN	0 = Interrupt requests for OC1 are disabled.* 1 = Interrupt requests for OC1 are enabled.*
3	IRQ_OC0_EN	0 = Interrupt requests for OC0 are disabled.* 1 = Interrupt requests for OC0 are enabled.*
2	IRQ_ICB_EN	0 = Interrupt requests for IC1 or IC3 are disabled.* 1 = Interrupt requests for IC1 or IC3 are enabled.*
1	IRQ_ICA_EN	0 = Interrupt requests for IC0 or IC2 or PWM power trip are disabled.* 1 = Interrupt requests for IC0 or IC2 or PWM power trip are enabled.*
0	IRQ_EOC_EN	0 = Interrupt on end-of-count is disabled. 1 = Interrupt on end-of-count enabled.

Timer Interrupt Identification Register
TMR0_IIR = 0062h, TMR1_IIR = 0067h, TMR2_IIR = 0071h, TMR3_IIR = 0076h

7		Unused.
6	OC3	0 = Output compare, OC3, does not occur. 1 = Output compare, OC3, occurs.
5	OC2	0 = Output compare, OC2, does not occur. 1 = Output compare, OC2, occurs.
4	OC1	0 = Output compare, OC1, does not occur. 1 = Output compare, OC1, occurs.
3	OC0	0 = Output compare, OC0, does not occur. 1 = Output compare, OC0, occurs.
2	ICB	0 = Input capture, ICB for IC1 or IC3, does not occur.* 1 = Input capture, ICB for IC1 or IC3, occurs.*
1	ICA	0 = Input capture, IC0 for IC3, or PWM power trip, does not occur.* 1 = Input capture, IC0 for IC3, or PWM power trip, occurs.*
0	EOC	0 = End-of-count does not occur. 1 = End-of-count occurs.

Timer Data RegistersÑLow and High Bytes
TMR0_DR_L = 0063h, TMR1_DR_L = 0068h, TMR2_DR_L = 0072h, TMR3_DR_L = 0077h,TMR0_DR_H = 0064h, TMR1_DR_H= 0069h, TMR2_DR_H = 0073h, TMR3_DR_H = 0078h

7:0	TMR_DR_x	00hÐFFh: TMRx_DR_H = TDATA [15:8] TMRx_DR_L = TDATA [7:0]

Timer Reload RegistersÑLow and High Byte
TMR0_RR_L = 0063h, TMR1_RR_L= 0068h, TMR2_RR_L = 0072h, TMR3_RR_L = 0077h,TMR0_RR_H = 0064h, TMR1_RR_H= 0069h, TMR2_RR_H = 0073h, TMR3_RR_H = 0078h

7:0	TMR_RR_x	00hÐFFh: TMRx_RR_H = RELOAD [15:8] TMRx_RR_L = RELOAD [7:0]

Timer Input Capture Control Register
TMR1_CAP_CTL = 006Ah, TMR3_CAP_CTL= 007Bh

7:4		Reserved.
3:2	CAP_EDGE_B	00 = Disable capture on ICB. 01 = Enable capture only on the falling edge of ICB. 10 = Enable capture only on the rising edge of ICB. 11 = Enable capture on both edges of ICB.
1:0	CAP_EDGE_A	00 = Disable capture on ICA. 01 = Enable capture only on the falling edge of ICA. 10 = Enable capture only on the rising edge of ICA. 11 = Enable capture on both edges of ICA.

Timer Input Capture Value A RegistersÑLow and High Bytes
TMR1_CAPA_L = 006Bh, TMR3_CAPA_L = 007Ch, TMR1_CAPA_H = 006Ch, TMR3_CAPA_H = 007Dh

7:0	TMRx_CAPA_x	00hÐFFh: TMRx_CAPA_H = CAPTUREA [15:8] TMRX_CAPA_L = CAPTUREA [7:0]

Timer Input Capture Value B RegistersÑLow and High Bytes
TMR1_CAPB_L = 006Dh, TMR3_CAPB_L = 007Eh, TMR1_CAPB_H =006Eh, TMR3_CAPB_H = 007Fh

7:0	TMRx_CAPB_x	00hÐFFh: TMRx_CAPB_H = CAPTUREB [15:8] TMRx_CAPB_L = CAPTUREB [7:0]

Timer Output Compare Control Register 1
TMR3_OC_CTL1 = 0080h

7:6		Unused.
5:2	OCx_INIT X[3:0]	0 = OC pin cleared when initialized. 1 = OC pin set when initialized.
1	MAST_MODE	0 = OC pins are independent. 1 = OC pins all mimic OC0.
0	OC_EN	0 = OUTPUT COMPARE mode is disabled. 1 = OUTPUT COMPARE mode is enabled.

Timer Output Compare Control Register 2
TMR3_OC_CTL2 = 0081h

7:0	OCx_MODE X[3:0]	00 = Initialize OC pin to value specified in TMR3_OC_CTL1.* 01 = OC pin is cleared upon timer compare. 10 = OC pin is set upon timer compare. 11 = OC pin toggles upon timer compare.

Timer Output Compare Value RegistersÑLow and High Bytes
TMR3_OC0_L = 0082h, TMR3_OC1_L = 0084h,TMR3_OC2_L = 0086h, TMR_OC3_L = 0088h,TMR3_OC0_H = 0082h, TMR3_OC1_H = 0084h, TMR3_OC2_H = 0086h, TMR_OC3_H = 0088h

7:0	TMR3_OCx_x	00hÐFFh: TMR3_OCx_H = COMPARE [15:8] TMR3_OCx_L = COMPARE [7:0]

SPI Registers

SPI Baud Rate Generator RegisterÑLow Byte
SPI_BRG_L = 00B8h

7:0	SPI_BRG_L	00hÐFFh: These bits represent the Low byte of the 16-bit Baud Rate Generator divider value.*

SPI Baud Rate Generator RegisterÑHigh Byte
SPI_BRG_H = 00B9h

7:0	SPI_BRG_H	00hÐFFh: These bits represent the High byte of the 16-bit Baud Rate Generator divider value.*

SPI Control Register
SPI_CTL = 00BAh

7	IRQ_EN	0 = SPI system interrupt is disabled. 1 = SPI system interrupt is enabled.
6		Reserved.
5	SPI_EN	0 = SPI is disabled. 1 = SPI is enabled.
4	MASTER_EN	0 = When enabled, the SPI operates as a slave. 1 = When enabled, the SPI operates as a master.
3	CPOL	0 = Master SCK pin idles in a Low (0) state. 1 = Master SCK pin idles in a High (1) state.
2	CPHA	0 = SS must go High after every data byte transfer. 1 = SS can remain Low to transfer any number of data bytes.
1:0		Reserved.

SPI Status Register
SPI_SR = 00BBh

7	SPIF	0 = SPI data transfer is not finished. 1 = SPI data transfer is finished.*
6	WCOL	0 = An SPI write collision is not detected. 1 = An SPI write collision is detected.*
5		Reserved.
4	MODF	0 = A mode fault (multimaster conflict) is not detected. 1 = A mode fault (multimaster conflict) is detected.*
3:0		Reserved.

SPI Transmit Shift Register
SPI_TSR = 00BCh

7:0	TX_DATA	00hÐFFh: SPI transmit data.

SPI Receive Buffer Register
SPI_RBR = 00BCh

7:0	RX_DATA	00hÐFFh: SPI received data.

IrDA Registers

Infrared Encoder/Decoder Control Register
IR_CTL = 00BFh

7:3		Reserved.
2	LOOP_BACK	0 = Internal LOOPBACK mode is disabled. 1 = Internal LOOPBACK mode is enabled.*
1	IR_RxEN	0 = IR_RXD data is ignored. 1 = IR_RXD data is passed to the UART0 RxD.
0	IR_EN	0 = Infrared Encoder/Decoder is disabled. 1 = Infrared Encoder/Decoder is enabled.

Multi-PWM Control Registers

PWM Control Register 1
PWM_CTL1 = 0079h

7	PAIR_EN	0 = Global disable of the PWM outputs.* 1 = Global enable of the PWM and PWM output pairs.
6	PT_EN	0 = Disable power-trip feature. 1 = Enable power-trip feature.
5	MM_EN	0 = Disable Master mode. 1 = Enable Master mode.
4	PWM3_EN	0 = Disable PWM generator 3. 1 = Enable PWM generator 3.
3	PWM2_EN	0 = Disable PWM generator 2. 1 = Enable PWM generator 2.
2	PWN1_EN	0 = Disable PWM generator 1. 1 = Enable PWM generator 1.
1	PWM0_EN	0 = Disable PWM generator 0. 1 = Enable PWM generator 0.
0	MPWM_EN	0 = Disable Multi-PWM mode. 1 = Enable Multi-PWM mode.

PWM Control Register 2
PWM_CTL2 = 007Ah

7:6	AON_EN	00 = Disable AND/OR features on PWM. 01 = Enable AND logic on PWM. 10 = Enable OR logic on PWM. 11 = Disable AND/OR features on PWM.
5:4	AO_EN	00 = Disable AND/OR features on PWM. 01 = Enable AND logic on PWM. 10 = Enable OR logic on PWM. 11 = Disable AND/OR features on PWM.
3:0	PWM_DLY	Amount of delay between falling edge of PWM (PWM) and rising edge of PWM (PWM). 0000 = None 1000 = 8 SCLK periods 0001 = 1 SCLK period 1001 = 9 SCLK periods 0010 = 2 SCLK periods 1010 = 10 SCLK periods 0011 = 3 SCLK periods 1011 = 11 SCLK periods 0100 = 4 SCLK periods 1100 = 12 SCLK periods 0101 = 5 SCLK periods 1101 = 13 SCLK periods 0110 = 6 SCLK periods 1110 = 14 SCLK periods 0111 = 7 SCLK periods 1111 = 15 SCLK periods

PWM Control Register 3
PWM_CTL3 = 007Bh

7:4	PT_ICx_EN X[3:0]	0 = Power trip disabled on ICx. 1 = Power trip enabled on ICx.
3	PT_TRI	0 = All PWM trip levels are tristate. 1 = All PWM trip levels are defined by PT_LVL and PT_LVL_N.
2	PT_LVL	0 = After power trip, PWMx outputs are set to one. 1 = After power trip, PWMx outputs are set to zero.
1	PT_LVL_N	0 = After power trip, PWMx outputs are set to one. 1 = After power trip, PWMx outputs are set to zero.
0	PTD	0 = Power trip has been cleared. 1 = This bit is set after power trip event.

ZDI Registers

ZDI Address Match Registers
ZDI_ADDR0_L = 00h, ZDI_ADDR0_H = 01h, ZDI_ADDR0_U = 02H, ZDI_ADDR1_L = 04h, ZDI_ADDR1_H = 05h, ZDI_ADDR1_U = 06H, ZDI_ADDR2_L = 08h, ZDI_ADDR2_H = 09h, ZDI_ADDR2_U = 0AH, ZDI_ADDR3_L = 0Ch, ZDI_ADDR3_H = 0Dh, ZDI_ADDR3_U = 0EH*

7:0	ZDI_ADDRX_L, ZDI_ADDRX_H, or ZDI_ADDRX_U	000000hÐFFFFFFh: ZDI_ADDRX_U = ADDRX [23:16] ZDI_ADDRX_H = ADDRX [15:8] ZDI_ADDRX_L = ADDRX [7:0]

ZDI Break Control Register
ZDI_BRK_CTL = 10h*

7	BRK_NEXT	0 = ZDI break on the next CPU instruction is disabled.* 1 = ZDI break on the next CPU instruction is enabled.*
6	BRK_ADDR3	0 = ZDI break, upon matching break address 3, is disabled. 1 = ZDI break, upon matching break address 3, is enabled.
5	BRK_ADDR2	0 = ZDI break, upon matching break address 2, is disabled. 1 = ZDI break, upon matching break address 2, is enabled.
4	BRK_ADDR1	0 = ZDI break, upon matching break address 1, is disabled. 1 = ZDI break, upon matching break address 1, is enabled.
3	BRK_ADDR0	0 = ZDI break, upon matching break address 0, is disabled. 1 = ZDI break, upon matching break address 0, is enabled.
2	IGN_LOW_1	0 = Break on entire ADDR1. 1 = Break on upper 16 bits or ADDR1.
1	IGN_LOW_0	0 = Break on entire ADDR0. 1 = Break on upper 16 bits or ADDR0.
0	SINGLE_STEP	0 = ZDI SINGLE STEP mode is disabled. 1 = ZDI SINGLE STEP mode is enabled.*

ZDI Master Control Register
ZDI_MASTER_CTL = 11h

7	ZDI_RESET	0 = No action. 1 = Initiate a RESET of the eZ80F91.*
6:0		Reserved.

ZDI Write Data Registers
ZDI_WR_U = 13h, ZDI_WR_H = 14h, ZDI_WR_L= 15h*

7:0	ZDI_WR_L, ZDI_WR_H, or ZDI_WR_U	000000hÐFFFFFFh: Write operation defined by the ZDI_RW_CTRL register. {ZDI_WR_U = WDATA [23:16], ZDI_WR_H = WDATA[15:8], ZDI_WR_L = WDATA[7:0]}*

ZDI Read/Write Control Register
ZDI_RW_CTL = 16h*

7:0		00 Read {MBASE, A, F} 80 Write AF 01 Read BC 81 Write BC 02 Read DE 82 Write DE 03 Read HL 83 Write HL 04 Read IX 84 Write IX 05 Read IY 85 Write IY 06 Read SP 86 Write SP 07 Read PC 87 Write PC 08 Set ADL 88 Reserved 09 Reset ADL 89 Reserved 0A Exchange CPU register sets 8A Reserved 0B Read memory from current PC value, increment PC 8B Write memory from current PC value, increment PC

ZDI Bus Control Register
ZDI_BUS_CTL = 17h*

7	ZDI_BUSAK_EN	0 = Ignore external bus requests (BUSREQ).* 1 = Accept external bus requests (BUSREQ).*
6	ZDI_BUSAK	0 = Deassert the bus acknowledge pin (BUSACK).* 1 = Assert the bus acknowledge pin (BUSACK).*
5:0		Reserved.

ZDI Instruction Store 4:0 Registers
ZDI_IS4 = 21h, ZDI_IS3 = 22h, ZDI_IS2= 23h, ZDI_IS1= 24h, ZDI_IS0 = 25h*

7:0	ZDI_IS4, ZDI_IS3, ZDI_IS2, ZDI_IS1, or ZDI_IS0	00hÐFFh: ZDI_IS0 = INST [1st BYTE], ZDI_IS1 = INST [2nd BYTE], ZDI_IS2 = INST [3rd BYTE], ZDI_IS3 = INST [4th BYTE], ZDI_IS4 = INST [5th BYTE]*

ZDI Write Memory Register
ZDI_WR_MEM = 30h*

7:0	ZDI_WR_MEM	00hÐFFh: Byte written to ZDI_WR_MEM is also written to memory at address indicated by PC.

eZ80 Product ID RegistersÑLow and High Bytes
ZDI_ID_L = 00h, ZDI_ID_H = 01h

7:0	ZDI_ID_x	08h/00h: {ZDI_ID_H, ZDI_ID_L} = {00h, 08h} indicates the eZ80F91 product.*

eZ80 Product ID Revision Register
ZDI_ID_REV = 02*

7:0	ZDI_ID_REV	00hÐFFh: Identifies the current revision of the eZ80F91 product.

ZDI Status Register
ZDI_STAT = 03h*

7	ZDI_ACTIVE	0 = CPU is not functioning in ZDI mode. 1 = CPU is currently functioning in ZDI mode.
6		Reserved.
5	HALT_SLP	0 = CPU is not currently in HALT or SLEEP mode. 1 = CPU is currently in HALT or SLEEP mode.
4	ADL	0 = CPU is operating in Z80 MEMORY mode.* 1 = CPU is operating in ADL MEMORY mode.*
3	MADL	0 = CPUÕs Mixed-Memory mode (MADL) bit is reset to 0. 1 = CPUÕs Mixed-Memory mode (MADL) bit is set to 1.
2	IEF1	0 = CPUÕs Interrupt Enable Flag 1 is reset to 0.* 1 = CPUÕs Interrupt Enable Flag 1 is set to 1.*
1:0	RESERVED	Reserved.

ZDI Read RegistersÐLow, High and Upper
ZDI_RD_L = 10h, ZDI_RD_H = 11h, ZDI_RD_U= 12h*

7:0	ZDI_RD_L, ZDI_RD_H, or ZDI_RD_U	000000hÐFFFFFFh: Read Control register during a ZDI Read operation. {ZDI_RD_U = RDATA [23:16], ZDI_RD_H = RDATA [15:8], ZDI_RD_L = RDATA [7:0]}

ZDI Read Memory Register
ZDI_RD_MEM = 20h*

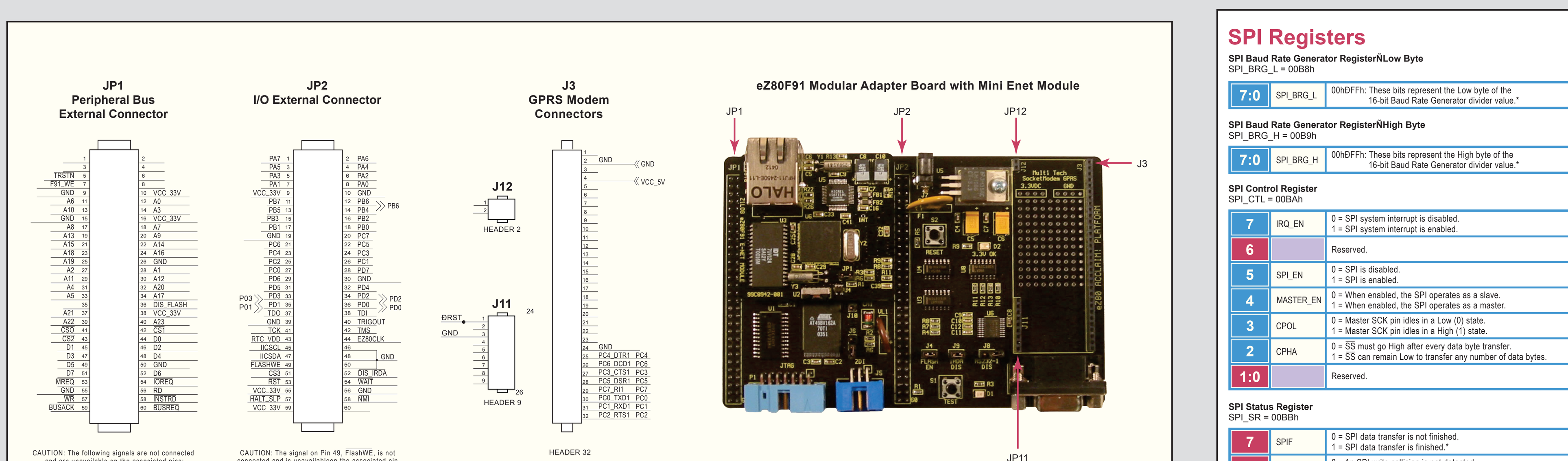
7:0	ZDI_RD_MEM	00hÐFFh: 8-bit data Read from the memory address indicated by the CPUÕs Program Counter.*

Interrupt Controller

Interrupt Vector Sources by Priority
INT_P0 = 0010h, INT_P1 = 0011h, INT_P2 = 0012h
INT_P3 = 0013h, INT_P4 = 0014h, INT_P5 = 0015h

Priority	Priority Control Bit	Vector	Source	Priority	Priority Control Bit	Vector	Source
0	INT_P0[0]	040h	EMAC Rx	24	INT_P3[0]	0A0h	Port B 0
1	INT_P0[1]	044h	EMAC Tx	25	INT_P31]	0A4h	Port B 1
2	INT_P0[2]	048h	EMAC SYS	26	INT_P3[2]	0A8h	Port B2
3	INT_P0[3]	04Ch	PLL	27	INT_P3[3]	0ACh	Port B3
4	INT_P0[4]	050h	Flash	28	INT_P3[4]	0B0h	Port B4
5	INT_P0[5]	054h	Timer 0	29	INT_P3[5]	0B4h	Port B5
6	INT_P0[6]	058h	Timer 1	30	INT_P3[6]	0B8h	Port B6
7	INT_P0[7]	05Ch	Timer 2	31	INT_P3[7]	0BCh	Port B7
8	INT_P1[0]	060h	Timer 3	32	INT_P4[0]	0C0h	Port C0
9	INT_P1[1]	064h	unused*	33	INT_P4[1]	0C4h	Port C1
10	INT_P1[2]	068h	unused*	34	INT_P4[2]	0C8h	Port C2
11	INT_P1[3]	06Ch	RTC	35	INT_P4[3]	0CCh	Port C3
12	INT_P1[4]	070h	UART 0	36	INT_P4[4]	0D0h	Port C4
13	INT_P1[5]	074h	UART 1	37	INT_P4[5]	0D4h	Port C5
14	INT_P1[6]	078h	I2C	38	INT_P4[6]	0D8h	Port C6
15	INT_P1[7]	07Ch	SPI	39	INT_P4[7]	0DCh	Port C7
16	INT_P2[0]	080h	Port A 0	40	INT_P5[0]	0E0h	Port D0
17	INT_P2[1]	084h	Port A 1	41	INT_P5[1]	0E4h	Port D1
18	INT_P2[2]	088h	Port A 2	42	INT_P5[2]	0E8h	Port D2
19	INT_P2[3]	08Ch	Port A 3	43	INT_P5[3]	0ECh	Port D3
20	INT_P2[4]	090h	Port A 4	44	INT_P5[4]	0F0h	Port D4
21	INT_P2[5]	094h	Port A 5	45	INT_P5[5]	0F4h	Port D5
22	INT_P2[6]	098h	Port A 6	46	INT_P5[6]	0F8h	Port D6
23	INT_P2[7]	09Ch	Port A 7	47	INT_P5[7]	0FCh	Port D7

Note: Each bit sets the Interrupt Priority Level for the given device. 0 = Default Level 0, 1 = Higher Level 1



eZ80F91 Modular Adapter Board Interfaces

LEGEND

Blue	Read/Write
Red	Read Only
Green	Write Only
Orange	Unique parameter-dependent Read/Write behavior
Lavender	Reserved

*Zilog has exercised all efforts to ensure accuracy. Should you find discrepancies, please consult the eZ80F91 Product Specification (PS0192).

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