Application Note

Using BSDL Files with eZ80® and eZ80Acclaim!™ Devices

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ZiLOG Worldwide Headquarters • 532 Race Street • San Jose, CA 95126
Telephone: 408.558.8500 • Fax: 408.558.8300 • www.zilog.com

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ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126
Telephone: 408.558.8500
Fax: 408.558.8300
www.zilog.com

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Document Disclaimer

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Acknowledgments

BSDL Syntax and Semantic Error Checking

Agilent Technologies
BSDL/IEEE 1149.1 Verification Service
http://we.home.agilent.com/upload/cmc_upload/bsdl_s2r_2.htm

BSDL File Verification

JTAG Technologies Verification Service
www.jtag.com

Abstract

This Application Note is targeted toward Board Test Development Engineers and Technicians to provide a smooth implementation of eZ80® and eZ80Acclaim!™ testability features. Knowledge of the JTAG 1149.1 specification, boundary-scan architecture, and Boundary-Scan Description Language (BSDL) is required. For additional information, refer to IEEE Standard 1149.1, titled *IEEE Standard Test Access Port and Boundary-Scan Architecture*.

General Overview

ZiLOG has phased JTAG 1149.1 support into the On-Chip Instrumentation (OCI)[1] debugger interface implemented on eZ80® and eZ80Acclaim!™ microprocessors. OCI contains a JTAG-style Test Access Port (TAP). JTAG 1149.1 support is implemented in the current eZ80® and eZ80Acclaim!™ product lines, as indicated in Table 1.

Table 1. JTAG 1149.1 Implementation in the eZ80® Family of Devices

Device	Speed of Device	JTAG Functionality
eZ80® Product Line		
eZ80190	20MHz/50MHz	No JTAG Functions.
eZ80L92	20MHz/50MHz	JTAG-compatible TAP; no boundary scan register; no $\overline{\text{TRST}}$ support.
eZ80Acclaim!™ Product Line		
eZ80F92	20MHz	JTAG-compatible TAP; no boundary scan register; no $\overline{\text{TRST}}$ support.
eZ80F93	20MHz	JTAG-compatible TAP; no boundary scan register; no $\overline{\text{TRST}}$ support.
eZ80F91	50MHz	JTAG-compatible TAP with boundary scan register and $\overline{\text{TRST}}$ support.

As noted in Table 1, eZ80® and eZ80Acclaim!™ devices are *compatible* to the Joint Test Action Group (JTAG) 1149.1 standard.

TAP Implementation

The OCI feature of the eZ80® and eZ80Acclaim!™ devices uses JTAG-standard control pins with an 1149.1-compliant 16-state TAP. These TAP signals are listed in Table 2.

[1]On-Chip Instrumentation and OCI are registered trademarks of First Silicon Solutions, Inc.

Table 2. TAP Implementation

Test Access Port Signal	Direction
JTAG Test Mode Select (TMS)	Input
JTAG Test Clock In (TCK)	Input
JTAG Test Data In (TDI)	Input[1]
JTAG Test Data Out (TDO)	Output
JTAG Test Reset ($\overline{\text{TRST}}$)	Input[2]

Notes:
1. TDI does not feature an on-chip pull-up resistor. For 1149.1 compliance, a pull-up resistor must be placed on the PCB.
2. The TRST feature is only provided on the eZ80F91 device.

TAP Activation

To activate the TAP on eZ80® and eZ80Acclaim!™ devices, the TCK pin must be driven Low at least two CPU system clock cycles prior to the deassertion of the RESET pin. Otherwise, the JTAG features are disabled.

The eZ80L92, eZ80F92, and eZ80F93 devices do not feature an automatic power-on reset circuit. Device reset, via the external RESET pin, must always be executed following the application of power. Without a RESET following power-up, proper operation of the device cannot be guaranteed.

The eZ80F91 device includes a power-on-reset circuit. However, for Boundary Scan testing, ZiLOG recommends using the external RESET function. See the Reset Sections of the eZ80® and eZ80Acclaim!™ product specifications and their pin characteristics tables to obtain I/O pin direction states following reset.

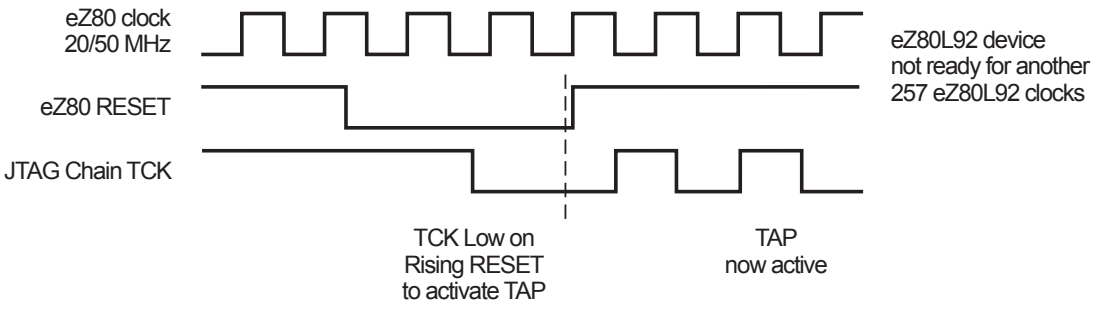

Figure 1. Reset Timing with the eZ80L92, eZ80F92, and eZ80F93 Devices

Reset Timing

Performing a device reset with TCK held Low is required for TAP operation on all eZ80® and eZ80Acclaim!™ devices (see Figure 1). Device reset, via the external RESET pin, is required on the eZ80L92, eZ80F92, and eZ80F93 devices; it is recommended on the eZ80F91.

As a result of TAP activation, the TAP exists in an unknown state. To enter the TAP Test-Logic-Reset state, TMS must be held High for at least five rising edges of TCK. On the eZ80F91 device TRST can be used to initialize the TAP controller and is recommended over the TMS – TCK method.

The maximum frequency of TCK is half the frequency of the CPU system clock. When in the Test-Logic-Reset state, the IDCODE is forced into the instruction register's parallel output latches, as defined in 1149.1.

eZ80L92-, eZ80F92-, and eZ80F93-Specific Implementation

This section is specific to the eZ80L92, eZ80F92, and eZ80F93 devices.

Boundary Register Commands

When the boundary register commands SAMPLE, PRELOAD, or EXTEST are captured in the TAP instruction register, the eZ80® device places an 8-bit data register between TDI and TDO, as indicated in Tables 3 and 4. The selected register contains the OCI revision, which is shifted out prior to TDO echoing TDI in an 8-bit delay bypass mode. See Figure 2.

Table 3. eZ80L92, eZ80F92, and eZ80F93 Required Public Instructions

Standard 1149.1 Command	eZ80L92, eZ80F92, and eZ80F93 Action
BYPASS	1149.1-compliant.
SAMPLE	Defaults to an 8-bit data register rev_code.
PRELOAD	Defaults to an 8-bit data register rev_code.
EXTEST	Defaults to an 8-bit data register rev_code.

Table 4. eZ80L92, eZ80F92, and eZ80F93 Optional Public Instructions

Standard 1149.1 Command	eZ80L92, eZ80F92, and eZ80F93 Action
IDCODE	1149.1-compliant.

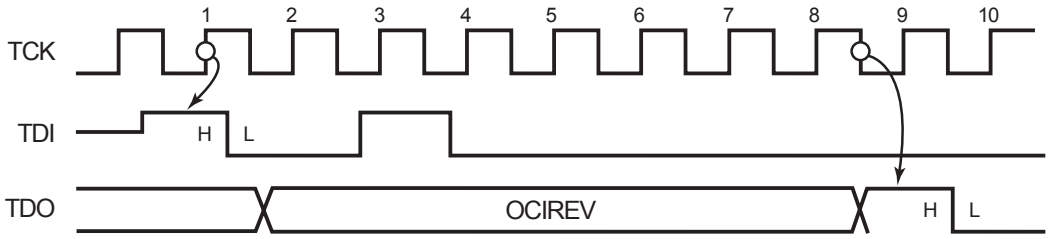

Figure 2. Sample Command Operation

The OCI contains an extensive set of private commands for use with an application's development tools. Private command access requires a software license agreement. The private commands are not applicable to printed circuit board boundary scan testing.

ATPG Editing

Automatic Test Program Generation (ATPG) tools require the BSDL file to be 1149.1-compliant. Printed circuit board boundary scan test programs created with ATPG tools include the eZ80® 8-bit dummy register as part of a boundary scan chain TDI-to-TDO register length.

ZiLOG recommends that eZ80® 8-bit OCI revision data be set to *expect don't care* on ATPG-created code for SAMPLE, PRELOAD, and EXTEST test calls. The OCI revision level is not included in the BSDL file or device documentation. OCI revision value is subject to change on future eZ80® devices. Therefore, the expected values and bits are set to *internal* and *don't care*.

The eZ80® device does not feature a boundary scan register that can be used to verify interconnections to other boundary scan components. The device pins in output mode will drive a High or Low voltage during all modes of boundary scan operation. See the **Pin Characteristics** table in the eZ80L92 Product Specification (PS0130) or in the eZ80F92/eZ80F93 Product Specification (PS0153) to obtain I/O pin direction states following reset.

Caution: Because ATPG tools can either generate patterns to drive the printed circuit board traces (nets) between devices or ignore these traces completely, care must be taken to review their impact on all scan chain devices.

eZ80F91-Specific Implementation

The eZ80F91 device meets all 1149.1 operation requirements for the supported commands. However, the TDI pin is not 1149.1-compliant because it is not a dedicated input pin and does not feature an on-device pull-up resistor. After device RESET, the TDI pin defaults to Input mode.

TDI functions as a JTAG TAP input or ZiLOG Debug Interface (ZDI) input pin depending on the state of TCK during RESET. ZiLOG recommends using an external pull-up resistor. An external resistor does not interfere with TDI pin operation during ZDI bus device operation.

Table 5. eZ80F91 Required Public Instructions

Standard 1149.1 Command	eZ80F91 Action
BYPASS	1149.1-compliant.
SAMPLE	1149.1-compliant.
PRELOAD	1149.1-compliant.
EXTEST	1149.1-compliant.

Table 6. eZ80F91 Optional Public Instructions

Standard 1149.1 Command	eZ80F91 Action
IDCODE	1149.1-compliant.

The OCI contains an extensive set of private commands for use with an application's development tools. Private command access requires a software license agreement. These private commands are not applicable to printed circuit board boundary scan testing.

BSDL Files

Associated with this Application Note are BSDL files available for download on zilog.com. These BSDL files and their associated pin packages are listed in Table 7.

Table 7. Downloadable BSDL Files

BSDL File	Pin Package
eZ80L92.bsd	100-pin LQFP
eZ80F92.bsd	100-pin LQFP
eZ80F93.bsd	100-pin LQFP
eZ80F91.bsd	144-pin LQFP
	144-pin caBGA

Notes