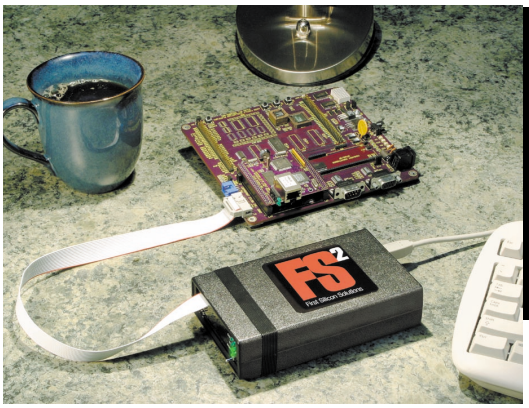


eZ80™

In-Target System Analyzer for ZiLOG's eZ80®

Features

- JTAG interface for eZ80L92, eZ80F91, eZ80F92, eZ80F93 and other parts in the family with available JTAG interface
- Trigger-in and Trigger-out signals to cross trigger with external instrumentation
- Read-write all CPU registers, memory, and I/O
- Go and halt processor run control
- Trace window with executed assembly and source code
- Single step by assembly or C source instruction
- Unlimited software breakpoints
- Four hardware execution breakpoints for code in ROM and Flash memory
- Flash programming support
- Four standard eZ80® triggers for address match and optionally qualifying any cycle type
- Additional four advanced triggers for address, data, and cycle types with support for address ranges, data values, and masked data values
- Load binary, Intel Hex, S-records, or COFF (from ZDS) and IAR file formats
- Single line assembler and disassembler
- Load code and debug symbols including code, variables, and variable types
- Source level debug from IAR Embedded Workbench interface
- Standalone windowed source debug interface supports ZDS tools

Debugging made easy

FS2 First Silicon Solutions

The FS2 In-Target System Analyzer for the eZ80® (ISA-eZ80) supports the special features and integrated peripherals of the eZ80® microprocessor and microcontroller family. It supports the ZiLOG Developer Studio (ZDS) and is integrated with the IAR Embedded Workbench software tools to maximize your productivity. The system analyzer provides source-level debug with an intuitive, easy-to-use interface. It features complete run control over the eZ80® and enables you to access and modify CPU registers, memory, and I/O. On-Chip Instrumentation (OCI™) debug features built into the eZ80® allow FS2 to provide a powerful debug tool with advanced features at a competitive price. The ISA-eZ80 debugger is housed in a compact chassis that connects to the target system using a standard 14-pin JTAG debug connector.

Setting software and hardware breakpoints

You can set an unlimited number of software breakpoints in RAM address space. In addition, there are four hardware breakpoints available. Hardware breakpoints are a great benefit for setting breakpoints and stepping through code in ROM and Flash memories.

Advanced triggers for breakpoint conditions

There are a total of eight hardware triggers. There are four standard eZ80® triggers that can monitor addresses and optionally detect any cycle type. A single address can be specified or a range of 256 addresses can be used with two of the standard triggers.

There are four additional enhanced triggers that allow you to specify data values in addition to addresses. These triggers can be paired to support address ranges and data masking. Enhanced triggers can also specify the type of memory or I/O cycle and desired action, whether to break, pulse the external trigger out, or start/stop trace collection.

ZiLOG

In-Target System Analyzer for ZiLOG's eZ80®

Trace features speed debugging

FS2's trace system uses branch trace message (BTM) collection, where the hardware only captures branch points in the code flow. Trace depth is typically 64 frames (32 to/from address pairs). Software reconstructs the instruction history between branch locations. So effective instruction depth displayed in the trace can be much deeper depending on the number of branches taken or not taken in the user's program. Tracing can be turned on/off by any of the four advanced triggers. The trace display shows disassembled instructions alone, source code, or mixed source/assembly.

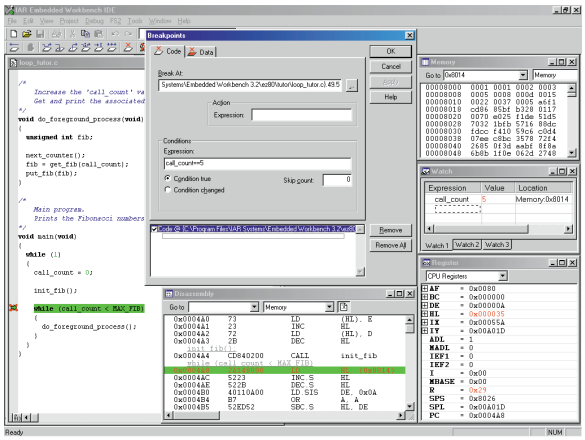
Flexible source-level debug interface options

The FS2 system is integrated with the IAR Embedded Workbench interface. In this mode all run-control, triggering, and trace features are accessible from the IAR debug interface. This combines all the capabilities of the FS2 system with the IAR Embedded Workbench, a powerful editing, compiling, project management, and source-level debug environment.

ZiLOG ZDS software tools are supported by the FS2 standalone source-level debug interface. The interface provides separate windows for source viewing and setting breakpoints, memory/register display, triggers, console commands, symbol explorer, and trace display.

Command-line interface

The ISA-eZ80 includes a command line interface (CLI). The CLI can be used as both a user interface and also for writing sophisticated automated sequences of tasks for items like regression tests. The CLI is based on the widely used Tcl/Tk scripting language.



FS2 In-Target System Analyzer GUI (with IAR interface)

Setting up is simple

The emulator connects to the target system using a 14-pin JTAG header. The software runs on Windows 98/NT/2000/XP PC over an IEEE-1284 EPP/ECP high-speed parallel or USB port. USB is supported on Windows 98SE/2000 and XP. A Pentium class computer with a minimum of 32MB of memory is required. All software is supplied, except user supplied IAR Workbench or ZDS tools.

Testing

A comprehensive self-test capability is included with the ISA-eZ80 system. For system verification, a loop-back board is provided which is plugged onto the end of the target interface cable. The self-test process exercises internal nodes and tests to ensure the cable signal integrity.

Product code: ISA-EZ80-JTAG

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