

S3 Family of Microcontrollers

S3F8S8B Development Kit

User Manual

UM027302-0816



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Revision History

Each instance in this document's revision history reflects a change from its previous edition. To learn more, refer to the corresponding page(s) or appropriate links furnished in the table below.

	Revision		
Date	Level	Description	Page
Aug 2016	02	Updated for ZDS-S3 version 5.3.0. Removed ISP I support	All
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Overview

Zilog's S3F8S8B Development Kit, part number S3F8S8B0100ZCOG, allows you to evaluate your S3F8S8B-based designs and applications. The Kit features a Development Board consisting of the following components:

- Four LEDs
- Seventeen pushbuttons
- Speaker
- LCD module
- UART
- 256 byte Serial EEPROM
- Header Pins

This user manual provides instructions for setting up and configuring the S3F8S8B Development Board. It includes schematic diagrams and a discussion of the Board features and ZDS II.

The S3F8S8B Development Board features an S3F8S8B MCU in a 100-pin TQFP package, plus an S3 PGM connector to connect the Board to a host development PC using the S3 Flash In-System Programmer II (ISP II). To learn more about the S3F8S8B MCU, refer to the S3F8S8B Product Specification (<u>PS0326</u>) and/or the S3 Flash In-System Programmer User Manual (<u>UM0266</u>).

This document guides you through the following tasks:

- Downloading and installing ZDSII software and documentation
- Connecting the S3 Flash ISP II and S3F8S8B Development Board to your PC
- Starting the S3F8S8B Ledblink sample program

Kit Contents

The S3F8S8B Development Kit contains the following items:

- S3F8S8B Development Board
- S3 Flash ISP II
- 10-circuit ribbon cable
- USB A (male) to Mini-B USB cable (2)



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• S3F8S8B Development Kit hardcopy insert

Figure 1 shows the contents of the S3F8S8B Development Kit.



Figure 1. S3F8S8B Development Kit

Features

The S3F8S8B Development Kit includes the following key items.

- S3F8S8B Development Board, which contains the following features:
 - S3F8S8B 100-pin TQFP MCU operating at 12 MHz, with 64 KB of internal Flash memory and 2 KB of internal RAM memory
 - USB interface to supply power to the board
 - LCD module
 - Speaker
 - 256 byte Serial EEPROM
 - UART Header at J6
 - Test Points Headers for all pins of MCU
 - MCU current measurement Test Points J2 and J3
 - Pin P47/AD7 level adjustable with potentiometer R11
 - Push Buttons
- S3 Flash In-System Programmer II (S3 Flash ISP II)



- ZDSII software, samples, and documentation available free for download
 - Sample programs

Supported Host Environments

The S3F8S8B Development Board supports the following operating systems:

- Microsoft Windows 7 (32-bit/64-bit)
- Microsoft Windows 8 (32-bit/64-bit)

Install the ZDSII Software and Documentation

Observe the following steps to download and install your ZDSII software and documentation.

▶ Note: If you have already installed ZDSII – S3 <version> and have downloaded the software and documentation by following the procedure on the paper insert in your kit (FL0171), skip ahead to the next section.

- 1. Prior to connecting the S3F8S8B Development Board to your development PC, download ZDS II for S3 v5.3.0 (or later) from the Downloadable Software category in the Zilog Store.
- 2. When the download is complete, unzip the file to your hard drive, then double-click the installation file named ZDS2_S3_<Version>.exe and follow the on-screen instructions.
- 3. When the ZDS II installation is complete, double-click the installation file named DOCS S3<version>.exe and follow the on-screen instructions.
- 4. When these installations are complete, view the S3F8S8B Development Kit User Manual (<u>UM0273</u>); this document will be located in the following path, by default: C:\Zilog\ZDSII_S3_

Establish a Connection with the PC

Observe the following procedure to connect the S3 Flash ISP II and S3F8S8B Development Board to your PC.



Caution: Disconnect or turn off the power to the S3F8S8B Development Board before connecting or disconnecting the S3 Flash ISP II.

1. Connect the Mini-B side of the USB A (male)-to-Mini-B cable to the S3 Flash ISP II. Connect the other end of this cable to the PC, as shown in Figure 2.



Figure 2. Connecting the S3 Flash ISPII to the Development PC

2. Connect the 10p 5x2 ribbon cable to the S3 Flash ISP II, as shown in Figure 3.



Figure 3. Connecting the 10-pin Ribbon Cable to the S3 Flash ISPII

3. Connect the other end of the ribbon cable to Debug Connector J1 on the Development Board. See Figure 4.





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Figure 4. Debug Connector J1

4. After completing the procedure to connect the S3F8S8B Development Board to the PC, the complete setup appears as shown in Figure 5.



Figure 5. The Completed ISP II and Development Board Assembly



Start the S3F8S8B Ledblink Sample Program

The S3F8S8B Development Kit includes a sample program that demonstrates an LED blinking application. To start the S3F8S8B Ledblink sample program, observe the following procedure.

- 1. Launch ZDSII by navigating from the Windows Start menu to Programs → Zilog ZDSII S3 <Version> → ZDSII S3 <Version>.
- 2. From the **File** menu in ZDSII, select **Open Project** as indicated in Figure 6, and navigate to the following filepath:

<ZDS Install>\samples\S3F8S8B\ledblink_asm



Figure 6. The Open Project Selection in the File Menu

3. Select the ledblink.zdsproj project from within the **ledblink_asm** folder as indicated in Figure 7 and click **Open**. A list of source files will appear in the Workspace panel.

Open

Cancel

•



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Open Project			×
Look in: 🔒 ledblink_asm 💌	← 🗈 📸 🐨		
Name	Date modified	Size	
Iedblink.zdsproj	7/20/2016 10:54 AM	24 KB	

Figure 7. Select the ledblink.zdsproj Project

Z Open Projec Look in:

File name:

ledblink.zdsproj

Files of type: ZDS II Project Files (*.zdsproj)

- 4. From the Build menu, select Set Active Configuration to open the Select Configuration dialog box.
- 5. Select **Debug**, then click **OK** to close the Select Configuration dialog box.
- 6. From the **Project** menu in ZDSII, select **Settings** to open the Project Settings dialog box. In the Project Settings dialog box, click the **Debugger** tab.



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7. On the Debugger page, select **S3F8SXB_FlashIspII** from the Target list, then select **S3FlashIspII** from the **Debug Tool** drop-down menu, as indicated in Figure 8.

Project Settings		×
Configuration: Debug	•	
General	录 Debugger	
Assembler Assembler Linker Objects and Libraries Address Spaces Warnings Output Debugger Flash Options	 Include ISP debug library (ResetGo only) ✓ Include Enhanced ISP Debug Library (Step into, Step Over, Step Out, Go, Run to Cursor, Reset and Reset+Go) Target Target Target Name Location ✓ S3F8SXB_RashIspII Project 	
	Setup Add Copy Delete Debug Tool	
Note This ZDSII version requires firmware 1. To upgrade the firmware, please select	5 or later if the selected debug tool is S3 Flash ISP II. the Tools menu -> Firmware Upgrade (selected debug tool) OK Cancel	1elp

Figure 8. Select the Target and Debug Tool



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8. After selecting **S3FlashIsplI** from the Debug Tool drop-down menu, click **Setup** to select the serial number of the S3 Flash ISP II you are using, as indicated in Figure 9. Click OK to close the Setup USB Communicationdialog box.

Setup USB Communication	
Serial Number: 1504080006	
Cancel	ppy Delete
Debug Tool	
Current: S3FlashIspII	Setup

Figure 9. The Setup USB Communication Dialog

Note: The serial number you see on your screen will be different from the serial number shown in Figure 9.

- 9. After selecting the serial number of the S3 Flash ISP II that you are using, select **Setup** from the Target field to select the Target Voltage..
- From the Target Configuration dialog, enter "0" on ISP_DBG_IDX and select the 3.3V by ISP button and Click OK. See Figure 10.

Target Configuration	x
ISP Baudrate Adjustment	
ISP_BRG_IDX: 0	
Note: ISP baud Rate = CPU Clock /(32 + ISP_BRG_IDX) Where CPU Clock = fosc /CPU_Div Where CPU_Div is determined by the CLKCON value	
Target Voltage:	
C 5.0 V by ISP	
Cancel	

Figure 10. Target Configuration Dialog



- 11. Make sure that the **Enhanced ISP Debug Library** is selcted fom the Debugger window
- 12. Click **OK** to close the Project Settings dialog box.
- 13. If you are prompted to rebuild any affected files, click **Yes**. Otherwise, choose **Build** from the menu bar, then click **Rebuild All**. The following example message is displayed.

Note: This Output Checksum message is an example and may not match the actual checksum of the project for a particular release of the ZDS installation software.

14. To run the application, select **Reset+Go** from the **Debug** menu, as indicated in Figure 11. As a result, LEDs D2, D3, and D4 will blink in sequence.



Figure 11. Select Reset+ Go from the Debug Menu



Troubleshooting Tips

The following troubleshooting tips are useful when starting the S3F8S8B Ledblink sample program.

- Ensure that the LED D4/POWER indicator on the S3 Flash ISP II lights up upon connecting to the USB port of your PC.
- Navigate to **Project** → **Settings** → **Debugger** → **Debug Tool** → **Setup**. Upon clicking **Setup** on the Setup USB Communication dialog box, verify that S3FlashIspII serial number is displayed.
- Remove and reconnect the S3 Flash ISP II on the USB port of your PC.
- Refer to Figure 14 on page 13 to learn more about the operations and power options of the S3F8S8B Development Board.

S3F8S8B Development Board

The purpose of the S3F8S8B Development Kit is to provide a set of hardware and software tools for the development of hardware and firmware for applications based on the S3F8S8B microcontroller. An image of the S3F8S8B Development Board is shown in Figure 12; a block diagram is shown in Figure 13.



Figure 12. The S3F8S8B Development Board



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Figure 13. The S3F8S8B Development Board Block Diagram



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Operations and Power Options

The operations and power options of the S3F8S8B Development Board are listed in Figure 14.

Operati	ons and Pow	er Optio	ons										
Option	Operations	ISP II USB Cable		ISP II USB Cable		ISP II USB Cable Target Voltage		Notes					
		cable on	on P1										
		J1											
1	Programming/	ON	OFF	3.3V by ISP	VDD = 3.3V	MCU power from S3 ISP II cable							
	Debugging				VCC_5V = 3.3V								
2	Programming/	ON	OFF	5.0V by ISP	VDD = 5.0V	MCU power from S3 ISP II cable							
	Debugging				VCC_5V = 5.0V								
3	Programming/	ON	See Notes	By External Source	VDD = VCC_5V = Vin	MCU power from External Source							
	Debugging					via P1 or J12							
4	Standalone	OFF	ON	Vin at P1	VDD = VCC_5V = Vin	MCU power from External Source							
						via P1							
5	Standalone	OFF	OFF	Vin at J12	VDD = VCC_5V = Vin	MCU power from External Source							
						via J12							

Figure 14	. Operations and	Power Options	of the S3F8S8B	Development Board
•				•

S3F8S8B MCU

Key features of the S3F8S8B MCU include:

- SAM88RC CPU core
- 64K x 8 bits program memory
- $2,134 \times 8$ bits data memory
- Endurance: 10,000 Erase/Program cycles
- 78 instructions
- Twelve programmable I/O ports, including eleven 8-bit ports, and one 2-bit port, for a total of 90 pins
- Sixteen bit-programmable pins for external interrupts
- One 8-bit basic timer for oscillation stabilization and watchdog functions (system r set)
- Four 8-bit timer/counter and two 16-bit timer/counter with selectable operating modes
- Watch timer for real time
- LCD Controller/driver
- A/D converter with 8 selectable input pins



- D/A converter with 1 selectable output pin
- Synchronous SIO modules
- Two asynchronous UART modules
- External data memory
- Battery level detector
- Pattern generation module

To learn more about the S3F8S8B MCU, refer to the S3F8S8B Product Specification (<u>PS0326</u>).

Magnetic Speaker

The CVS-1508 Speaker (SP1) manufactured by CUI Inc. is rated at a frequency of 1700Hz. An image of the CVS-1508 device is shown in Figure 15.



Figure 15. Magnetic Speaker

This speaker is activated by removing the shunt on J7.

To learn more about the CVS-1508 device, visit <u>http://www.cui.com/product/resource/</u> <u>cvs-1508.pdf.</u>



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Reset Circuit

The reset circuit features a $100 \text{K}\Omega$ pull-up resistor R3 and SW1. This circuit resets the S3F8S8B MCU when SW1 is pressed. See Figure 16 for a representation of the reset circuit.



Figure 16. The Reset Circuit

ISP II Connector

The ISP connector (J1) provides an interface between the S3 Flash ISP II tool and the S3F8S8B device. See Figure 17 for an illustration of the ISP connector.



Figure 17. The ISP II Connector



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LCD

The VIM-878-DP-FC-S-LV LCD manufactured by Varitronix Ltd. is a 36-pin module seated on both J4 and J5. Figure 18 shows an image of this LCD.



Figure 18. LCD

This eight-digit LCD is activated by selecting the segment of each digit that must light up. Figure 19 shows the LCD pin configuration and assignments.



PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
COM	1D	1L	2D	2L	3D	3	4D	4L	5D	5L	6D	6L	7D	7L	8D	8L	сомо				DP8	8M	DP7	7M	DP6	6M	DP5	5M	DP4	4M	DP3	3M	DP2	2M	DP1	1M
COM	1 1E	1K	2E	2K	3E	3K	4E	4K	5E	5K	6E	6K	7E	7K	8E	8K		COM1			8C	8N	7C	7N	6C	6N	5C	5N	4C	4N	3C	3N	2C	2N	1C	1N
COM	2 1F	1J	2F	2J	3F	3J	4F	4J	5F	5J	6F	6J	7F	7J	8F	8J			COM2		8B	8G	7B	7G	6B	6G	5B	5G	4B	4G	3B	3G	2B	2G	1B	1G
COM:	CA1	11	CA2	21	CA3	31	CA4	41	CA5	51	CA6	61	CA7	71	CA8	81				COM3	8A	8H	7A	7H	6A	6H	5A	5H	4A	4H	3A	ЗH	2A	2H	1A	18

Figure 19. LCD Pin Configuration and Assignments



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Serial EEPROM

The 93C56B is enabled through the Chip Select pin (CS) and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded, and the data is clocked out serially on the DO pin. Figure 20 shows the Serial EEPROM schematics.



Figure 20. Serial EEPROM Schematic



ZDS Flash Loader Utility

A Flash Loader utility is included in Zilog Developer Studio II via the Tools menu. Figure 21 shows an image of the Flash Programming screen.

Hex File	9:					ISP Serial Number
				[Pad File With	
log\zds	sii_s3_5.3.0\samples\s	3f8s5a\ledblink_asm\d	ebug\ledblink.het			1607140002 • C
					• None C Uther: [38	
Flash Op	ptions				Serialization	
Ena	able Read Protection			^	Method	Serial Address (Hex)
Ena	able HardLock Prote	ction			None	0000
M 2m	From the new file				C Pseudorandom	
ő	Custom			-	C Increment/Decrement(+/-)	- Serial Number Size
Y	Option Byte 0x0	03E			increments or coronicit ((*/*)	
	· ISP Reset Ve	ctor			0	# Bytes 1
	- O 200H					
	O 300H				Serial Number (Hex)	
	O 500H				00	
	O 900H					
	⊙ 100H (de	efault)		-		Read Serial Burn Seria
Operati	ions Options				- Status	
₩ Er	rase Before Programmi	na				
□ In	clude Serial Number					
Ir In	clude Flash Options					
Operati	ions					
	Erase	Program + Verify	Program			
	Verify	Program Options	Read Options			
	Device Checkum	File Checksum	View Memory		4	

Figure 21. The Flash Programming Screen

You can program the S3F8S8B MCU directly using the hex code generated from the ZDS IDE tools.



S3F8S8B Development Kit Documentation

The documents associated with the S3F8S8B Development Kit are listed in Table 1. Each of these documents can be obtained from the Zilog website by clicking the link associated with its Document Number. Alternatively, navigate to the directory listed in the Location column in your installed application.

Table 1. S3F8S8B Development Kit Documen
--

Document	Description	Location
<u>UM0273</u>	S3F8S8B Development Kit User Manual	Documentation\Tools_Documentation
PS0326	S3F8S8B Product Specification	Documentation\Chip_Documentation
<u>UM0266</u>	S3 Flash In-System Programmer User Manual	Documentation\Tools_Documentation
FL0171	S3F8S8B0100ZCOG Development Kit Insert	Documentation\Tools_Documentation
FL0165	S3 Flash In-System Programmer Insert	Documentation\Tools_Documentation
Online Help	ZDS II-S3 IDE, Assembler and C Compiler On-Line Help	ZDS II-S3 >Help >Help Topics

S3F8S8B Sample Projects

Table 2 lists the sample projects developed for this application. Follow the filepath stated in the Location column to access the associated project.

Project	Location	
SB8_Demo	samples\S3F8S8B\ISP_BL_Demo	
lcd	samples\S3F8S8B\S8B_LCD_asm	
lcd	samples\S3F8S8B\S8B_LCD_C	
ledblink	samples\S3F8S8B\ledblink_asm	
ledblink	samples\S3F8S8B\ledblink_c	
eeprom	samples\S3F8S8B\EEPROM_c	

 Table 2. S3F8S8B Sample Projects



Appendix A. Schematic Diagrams

Figures 22 and 23 present schematic diagrams of the S3F8S8B Development Board.









Figure 23. S3F8S8B Development Board Schematic Diagram, #2 of 2



Customer Support

To share comments, get your technical questions answered, or report issues you may be experiencing with our products, please visit Zilog's Technical Support page at <u>http://support.zilog.com</u>.

To learn more about this product, find additional documentation, or to discover other facets about Zilog product offerings, please visit the <u>Zilog Knowledge Base</u> or consider participating in the <u>Zilog Forum</u>.

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