



CUSTOMER PROCUREMENT SPECIFICATION

**Z86E2112PSC1468**  
**Z86E2112VSC1468**  
CMOS Z8® OTP  
MICROCONTROLLER

**GENERAL DESCRIPTION**

The Z86E21 microcontroller (MCU) introduces the next level of sophistication to single-chip architecture. The Z86E21 is a member of the Z8 single-chip microcontroller family with 8 Kbytes of EPROM and 236 bytes of general purpose RAM.

The Z86E21 is a pin compatible, One-Time-Programmable (OTP) version of the Z86C21. The Z86E21 contains 8 Kbytes of EPROM memory in place of the 8 Kbyte of ROM on the Z86C21.

The MCU is housed in a 40-pin DIP, 44-pin Leaded Chip-Carrier, or a 44-pin Quad Flat Pack, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin versions only. The MCU can address both external memory and preprogrammed ROM which enables this Z8 microcomputer to be used in high volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E21 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The Z86E21 fulfills this with 32-pin dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory and 236 General-Purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and serial data communication, the Z86E21 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Functional Block Description).

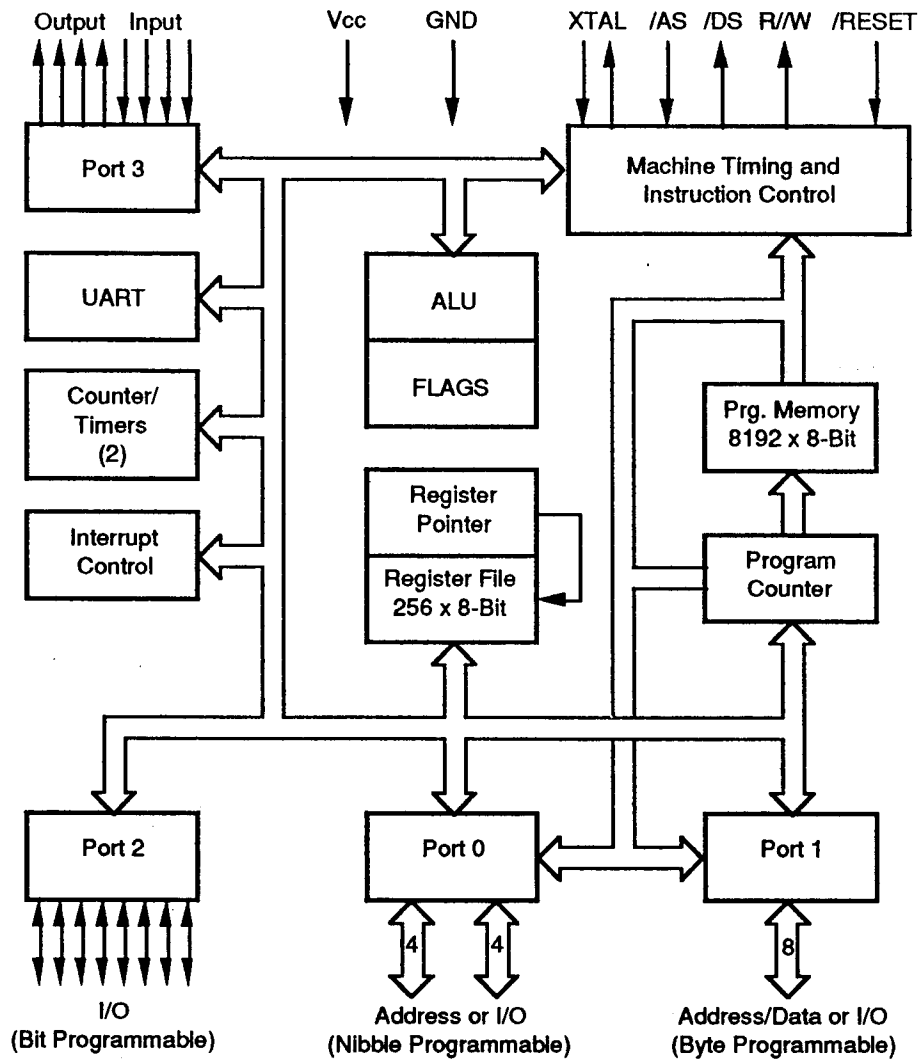
**Notes:**

All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power Ground	V <sub>CC</sub> GND	V <sub>DD</sub> V <sub>SS</sub>

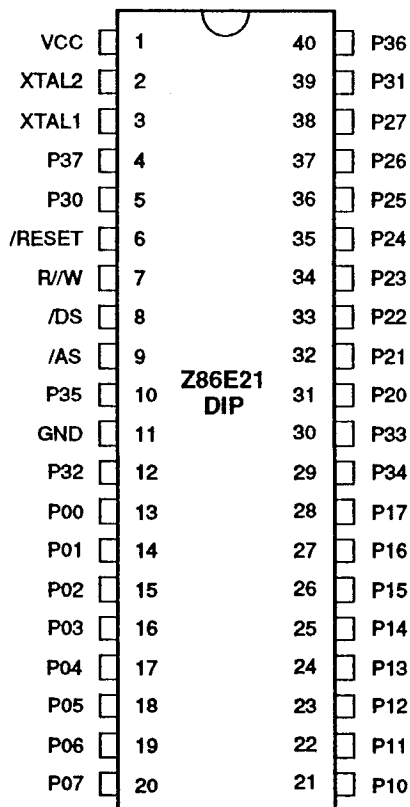
**GENERAL DESCRIPTION** (Continued)



**Functional Block Diagram**

## PIN DESCRIPTION

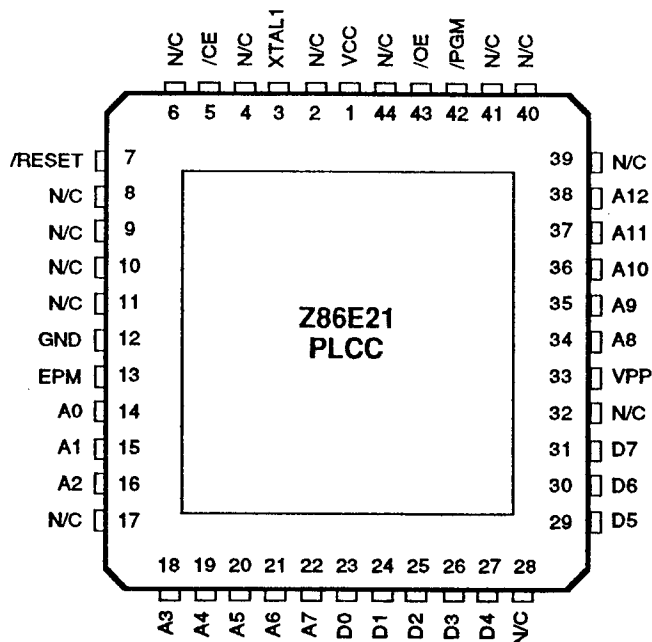
Standard Mode



### 40-Pin DIP Pin Assignments

#### 40-Pin DIP Pin Identification (Standard Mode)

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V <sub>cc</sub>	Power Supply	Input	11	GND	Ground, GND	Input
2	XTAL1	Crystal, Oscillator Clock	Output	12	P32	Port 3 pin 2	Input
3	XTAL2	Crystal, Oscillator Clock	Input	13-20	P00-P07	Port 0 pin 0,1,2,3,4,5,6,7	In/Output
4	P37	Port 3 pin 7	Output	21-28	P10-P17	Port 1 pin 0,1,2,3,4,5,6,7	In/Output
5	P30	Port 3 pin 0	Input	29	P34	Port 3 pin 4	Output
6	/RESET	Reset	Input	30	P33	Port 3 pin 3	Input
7	R/W	Read/Write	Output	31-38	P20-P27	Port 2 pin 0,1,2,3,4,5,6,7	In/Output
8	/DS	Data Strobe	Output	39	P31	Port 3 pin 1	Input
9	/AS	Address Strobe	Output	40	P36	Port 3 pin 6	Output
10	P35	Port 3 pin 5	Output				



**44-Pin PLCC Pin Assignments**

**44-Pin PLCC Pin Identification (EPROM Mode)**

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V <sub>CC</sub>	Power Supply	Input	18-22	A3-A7	Address 3,4,5,6,7	Input
2	N/C	Not Connected	Input	23-27	D0-D4	Data 0,1,2,3,4	In/Output
3	XTAL1	Crystal, Oscillator Clock	Input	28	N/C	Not Connected	Input
4	N/C	Not Connected	Input	29-31	D5-D7	Data 5,6,7	In/Output
5	/CE	Chip Enable	Input	32	N/C	Not Connected	Input
6	N/C	Not Connected	Input	33	V <sub>PP</sub>	Prog Voltage	Input
7	/RESET	Reset	Input	34-38	A8-A12	Address 8,9,10,11,12	Input
8-11	N/C	Not Connected	Input	39-41	N/C	Not Connected	Input
12	GND	Ground, GND	Input	42	/PGM	Prog Mode	Input
13	EPM	EPROM Prog Mode	Input	43	/OE	Output Enable	Input
14-16	A0-A2	Address 0,1,2	Input	44	N/C	Not Connected	Input
17	N/C	Not Connected	Input				

## ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply Voltage*	-0.3	+7.0	V
$T_{STG}$	Storage Temp	-65	+150	C
$T_A$	Oper Ambient Temp		†	C

### Notes:

\* Voltages on all pins with respect to GND.

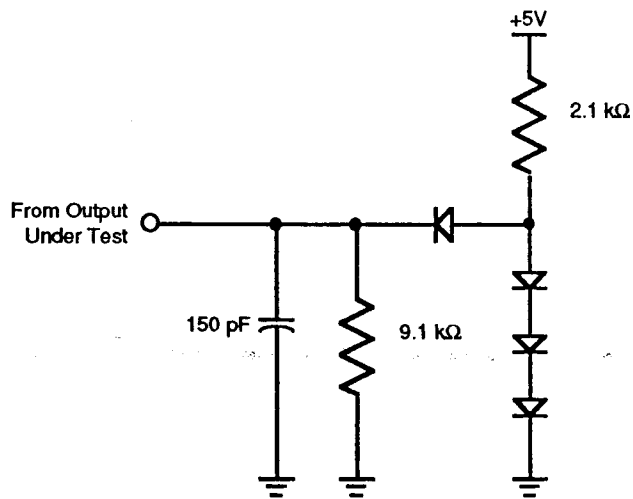
13.0 V Maximum on P30-P33.

† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram).



Test Load Diagram

## DC CHARACTERISTICS

Sym	Parameter	$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$		Typical at $25^\circ\text{C}$	Units	Conditions
		Min	Max	Min	Max			
	Max Input Voltage		7	7			V	$I_N = 250 \mu\text{A}$
	Max Input Voltage		13	13			V	P30-P33 Only
$V_{CH}$	Clock Input High Voltage	3.8	$V_{CC}$	3.8	$V_{CC}$		V	Driven by External Clock Generator
$V_{CL}$	Clock Input Low Voltage	-0.03	0.8	-0.03	0.8		V	Driven by External Clock Generator
$V_{IH}$	Input High Voltage	2.0	$V_{CC}$	2.0	$V_{CC}$		V	
$V_{IL}$	Input Low Voltage	-0.3	0.8	-0.3	0.8		V	
$V_{OH}$	Output High Voltage	2.4		2.4			V	$I_{OH} = -2.0 \text{ mA}$
$V_{OL}$	Output Low Voltage		0.4	0.4			V	$I_{OL} = +2.0 \text{ mA}$
$V_{RH}$	Reset Input High Voltage	3.8	$V_{CC}$	3.8	$V_{CC}$		V	
$V_{RL}$	Reset Input Low Voltage	-0.03	0.8	-0.03	0.8		V	
$I_{IL}$	Input Leakage	-10	10	-10	10		$\mu\text{A}$	$0\text{V } V_N, +5.25\text{V}$
$I_{OL}$	Output Leakage	-10	10	-10	10		$\mu\text{A}$	$0\text{V } V_N, +5.25\text{V}$
$I_{IR}$	Reset Input Current		-50	-50			$\mu\text{A}$	$V_{CC} = +5.25\text{V}, V_{RL} = 0\text{V}$
$I_{CC}$	Supply Current		50	50	25		mA	@ 12 MHz
			60	60	35		mA	@ 16 MHz
$I_{CC1}$	Standby Current		15	15	5		mA	HALT Mode $V_N = 0\text{V}, V_{CC} @ 12 \text{ MHz}$
			20	20	10		mA	HALT Mode $V_N = 0\text{V}, V_{CC} @ 16 \text{ MHz}$
$I_{CC2}$	Standby Current		20	20	5		$\mu\text{A}$	STOP Mode $V_N = 0\text{V}, V_{CC} @ 12 \text{ MHz}$
			20	20	5		$\mu\text{A}$	STOP Mode $V_N = 0\text{V}, V_{CC} @ 16 \text{ MHz}$

### Notes:

$I_{CC2}$  requires loading TMR (%F1H) with any value prior to STOP execution.

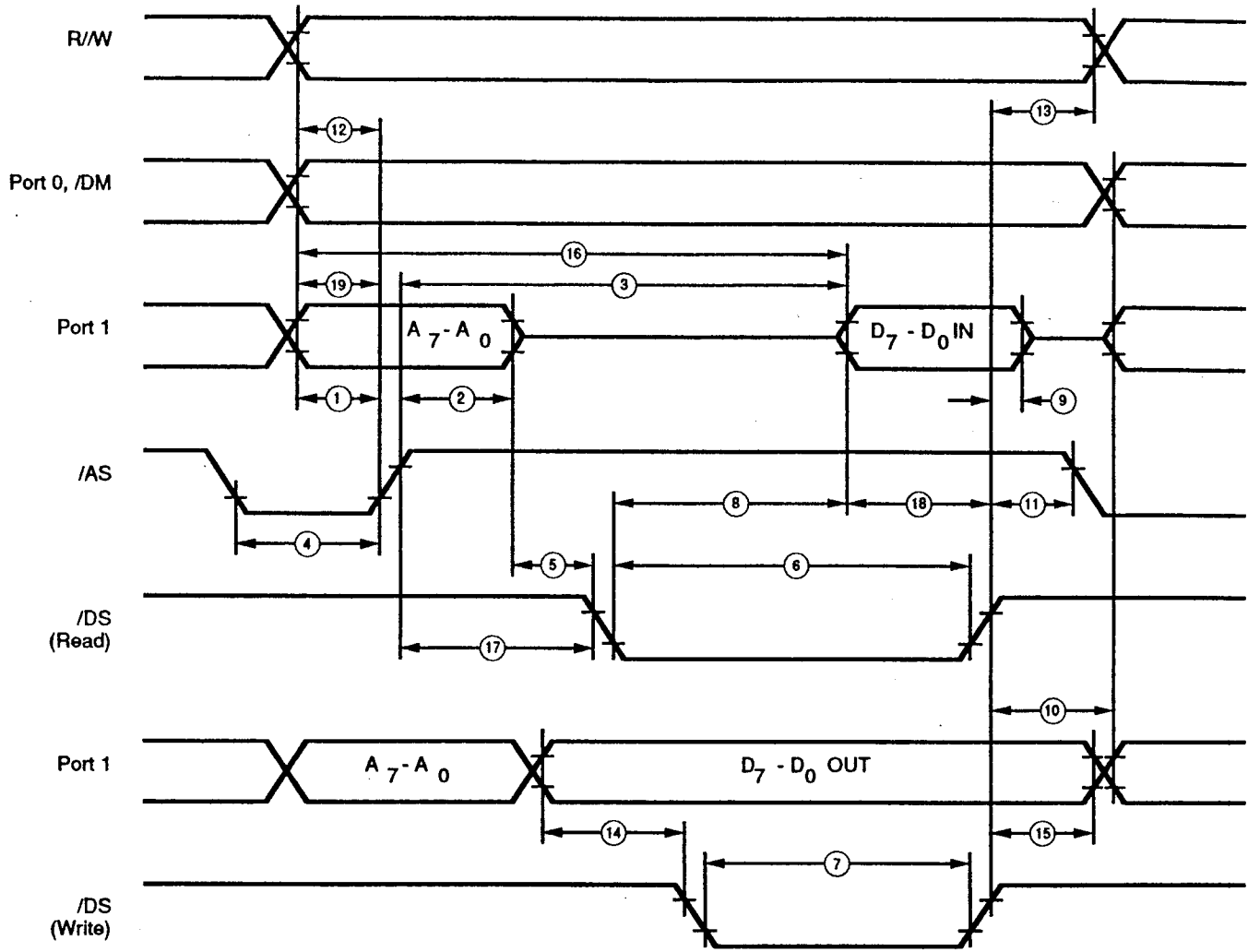
Use this sequence:

```
LD TMR,#00
```

```
NOP
```

# AC CHARACTERISTICS

## External I/O or Memory Read or Write Timing Diagram



External I/O or Memory Read/Write Timing

## AC CHARACTERISTICS

### External I/O or Memory Read and Write Timing Table

No	Symbol	Parameter	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$				$T_A = -40^\circ\text{C to } 105^\circ\text{C}$				Units	Notes
			12 MHz		16 MHz		12 MHz		16 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS Rise Delay	35		20		35		25		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		30		45		35		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		220		180		250		180	ns	[1,2,3]
4	TwAS	/AS Low Width	55		35		55		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		185		135		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		110		80		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75		130		75	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	45		35		65		50		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	55		30		45		35		ns	[2,3]
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	30		20		33		25		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	35		30		50		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		35		25		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	35		30		55		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		255		200		310		230	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	55		40		65		45		ns	[2,3]
18	TdDI(DS)	Data Input Setup to /DS Rise	75		60		75		60		ns	[1,2,3]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	50		30		50		30		ns	[2,3]

#### Notes:

- [1] When using extended memory timing add 2 TpC.  
 [2] Timing numbers given are for minimum TpC.  
 [3] See clock cycle dependent characteristics table.

#### Standard Test Load

All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

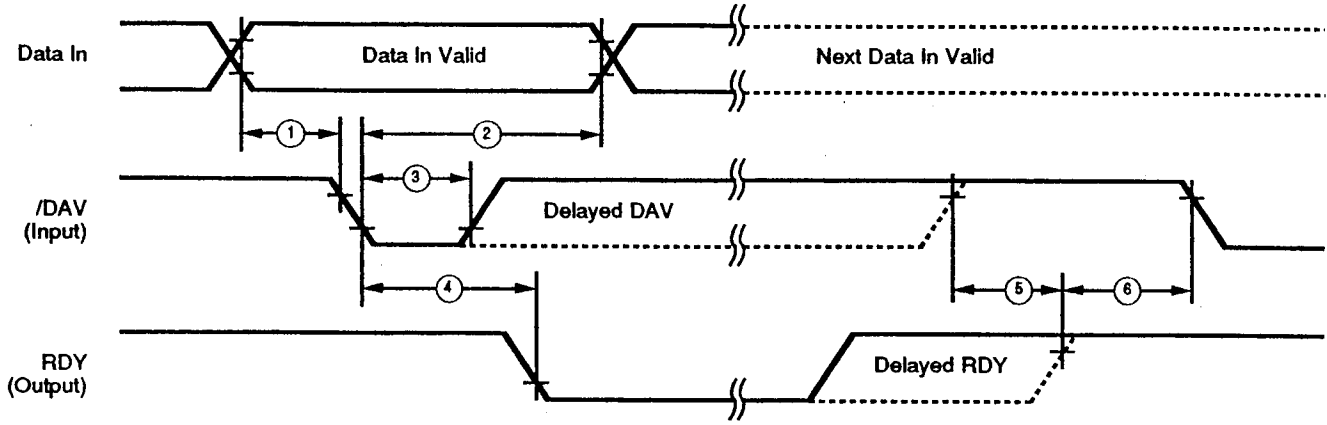
#### Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	$0.40\text{TpC} + 0.32$
2	TdAS(A)	$0.59\text{TpC} - 3.25$
3	TdAS(DR)	$2.38\text{TpC} + 6.14$
4	TwAS	$0.66\text{TpC} - 1.65$
6	TwDSR	$2.33\text{TpC} - 10.56$
7	TwDSW	$1.27\text{TpC} + 1.67$
8	TdDSR(DR)	$1.97\text{TpC} - 42.5$
10	TdDS(A)	$0.8\text{TpC}$
11	TdDS(AS)	$0.59\text{TpC} - 3.14$
12	TdR/W(AS)	$0.4\text{TpC}$
13	TdDS(R/W)	$0.8\text{TpC} - 15$
14	TdDW(DSW)	$0.4\text{TpC}$
15	TdDS(DW)	$0.88\text{TpC} - 19$
16	TdA(DR)	$4\text{TpC} - 20$
17	TdAS(DS)	$0.91\text{TpC} - 10.7$
18	TsDI(DS)	$0.8\text{TpC} - 10$
19	TdDM(AS)	$0.9\text{TpC} - 26.3$

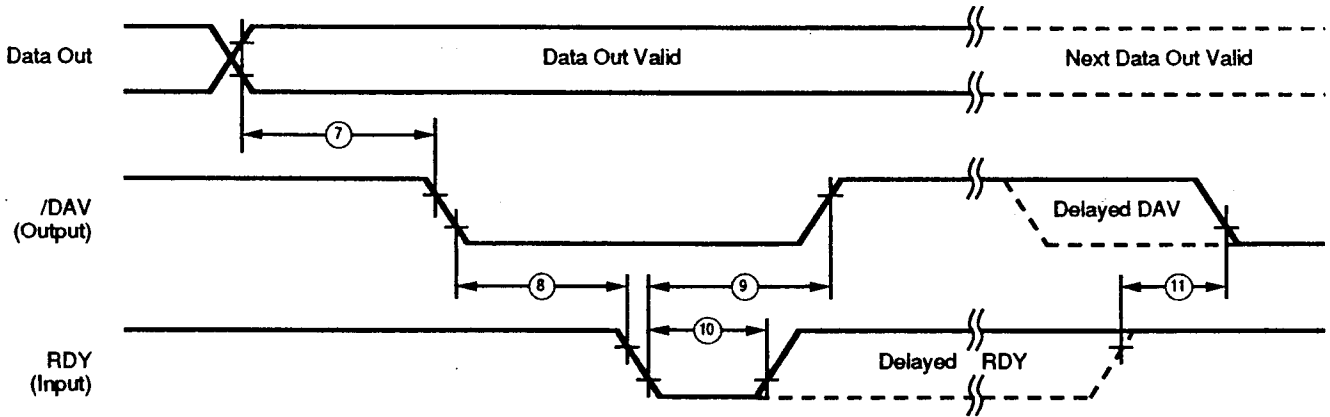


# AC CHARACTERISTICS

## Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

## AC CHARACTERISTICS

### Handshake Timing Table

No	Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$				$T_A = -40^\circ\text{C to } +105^\circ\text{C}$				Notes Data Direction
			12 MHz		16 MHz		12 MHz		16 MHz		
			Min	Max	Min	Max	Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	0		0		0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		145		145		IN
3	TwDAV	Data Available Width	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115		115		115	IN
5	TdDAVI(dRDY)	DAV Rise to RDY Rise Delay		115		115		115		115	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	0		0		0		0		IN
7	TcLDAVO(RDY)	Data Out to DAV Fall Delay		TpC		TpC		TpC		TpC	OUT
8	TcLDAVO(RDY)	DAV Fall to RDY Fall Delay	0		0		0		0		OUT
9	TdRDYQ(DAV)	RDY Fall to DAV Rise Delay		115		115		115		115	OUT
10	TwRDY	RDY Width	110		110		110		110		OUT
11	TdRDYOd(DAV)	RDY Rise to DAV Fall Delay		115		115		115		115	OUT

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