Application Note

Enabling Low Power Modes on the ZNEO® CPU

AN032401-0711

Abstract

This application note provides a blueprint for ZNEO Z16F Series MCU power management. It covers the ACTIVE, HALT and STOP CPU operating modes in which peripherals can be controlled to enable or disable power, as well as setting programmable option bits for additional power reduction. Also discussed is the recovery set-up routine to bring the MCU out from HALT or STOP modes.

Note: The source code file associated with this application note, AN0324-SC01.zip, is available for download on zilog.com. This source code has been tested with version 4.12.0 of ZDSII for MCUs based on the ZNEO CPU. Subsequent releases of ZDSII may require you to modify the code supplied with this application note.

Features

The power-saving features of the ZNEO Z16F Series MCU discussed in this Application Note are:

- Low-power modes that can be set by the user
- A Peripheral Control Register that allows users to enable/disable unused peripherals
- Programmable option bits for additional power reduction

Discussion

Zilog's ZNEO Z16F Series of Microcontroller products contains advanced integrated power-saving features, including power management functions which are divided into three categories to include CPU operating modes. These three categories are: ACTIVE, HALT and STOP modes, peripheral power control, and programmable option bits. The highest level of power reduction can be set through a combination of all three types of functions. For the purpose of this application note, we depopulated a ZNEO Development Board of all extra chips to gather current consumption readings.

Figure 1 shows both populated and depopulated boards, the latter containing a ZNEO MCU as the only remaining chip.

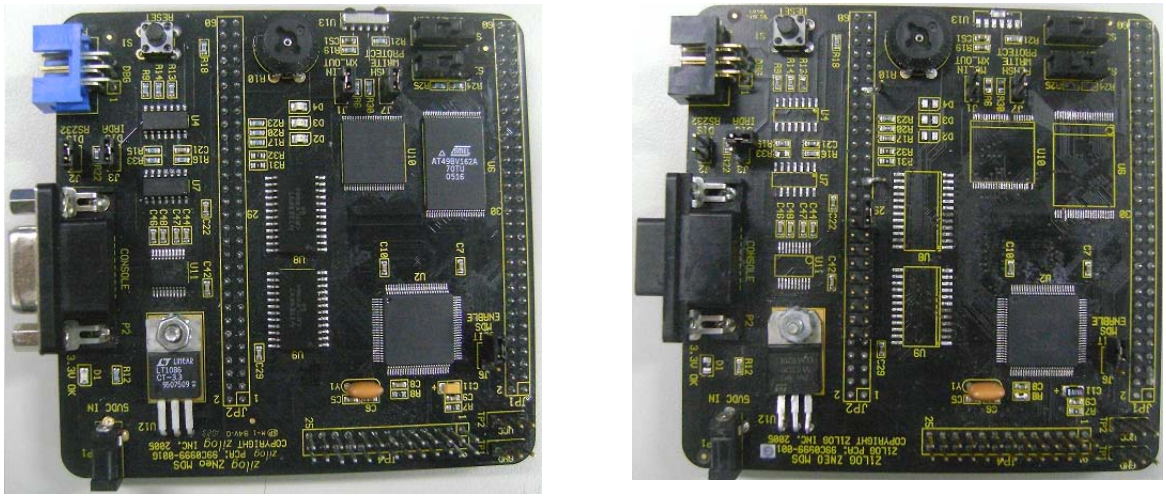

Figure 1. The ZNEO Development Board: Populated (left) and Depopulated (right)

HALT Mode

Execution of the ZNEO CPU's HALT instruction places the device into HALT Mode. The following operating characteristics are defined for HALT Mode:

- The system clock is enabled and continues to operate
- The ZNEO CPU is stopped
- The program counter stops incrementing
- The WDT's internal RC oscillator continues to operate
- If enabled, the WDT continues to operate
- All other on-chip peripherals continue to operate

The ZNEO CPU can be brought out of HALT Mode by any of the following operations:

- An interrupt or system exception
- A WDT time-out (system exception or RESET)
- Power-On Reset
- VBO reset
- External RESET pin assertion
- Instantaneous HALT-Mode Recovery

To minimize current in HALT Mode, all GPIO pins which are configured as inputs must be driven to one of the supply rails (V_{DD} or V_{SS}).

Note: You can place the ZNEO device into HALT Mode if the system has no processes to execute but the peripherals must still continue operation and are waiting for an interrupt to bring the CPU out from HALT Mode.

STOP Mode

Execution of the ZNEO CPU's STOP instruction places the device into STOP Mode. In STOP Mode, the operating characteristics are:

- The IPO is stopped; the XIN and XOUT pins are driven to VSS
- The system clock is stopped
- The ZNEO CPU is stopped
- The program counter stops incrementing
- If enabled for operation during STOP Mode, the WDT and its internal RC oscillator continue to operate
- If enabled for operation in STOP Mode via the associated option bit, the VBO protection circuit continues to operate
- All other on-chip peripherals are not active

To minimize current in STOP Mode, all GPIO pins that are configured as digital inputs must be driven to one of the supply rails (VDD or VSS), the VBO protection must be disabled, and WDT must be disabled.

The device is brought out of STOP Mode with a Stop-Mode Recovery. When the ZNEO CPU is in STOP Mode, Stop-Mode Recovery is initiated by:

- A WDT Time-Out
- A GPIO port input pin transition on an enabled Stop-Mode Recovery pin

Note: To prevent excess current consumption when using an external clock source in STOP Mode, the external clock must be disabled. If the system has no processes to execute, it can be placed into STOP Mode to await any transition in the STOP-Mode Recovery assignment pin to bring the CPU out from STOP Mode.

Tables 1 through 3 provide current and power consumption comparisons for the three different modes. In each of these tables, data is measured individually per condition, not in cumulative order.

Table 1. ACTIVE Mode

Current Consumed	Power	Condition
9.54	28.62	FSYSCLK = 20MHz; all peripherals enabled.
9.52	28.56	FSYSCLK = 20MHz; ADC is ON.
6.09	18.27	FSYSCLK = 20MHz; I^2C is ON.
6.09	18.27	FSYSCLK = 20MHz; ESPI is ON.
6.09	18.27	FSYSCLK = 20MHz; LIN-UART is ON.
6.09	18.27	FSYSCLK = 20MHz; PWM is ON.
6.08	18.24	FSYSCLK = 20MHz; all peripherals disabled.

Note: When the ZNEO CPU is in ACTIVE Mode, current is measured in milliAmps (mA) and the 3.0V power supply is measured in milliWatts (mW).

Table 2. HALT Mode

Current Consumed	Power	Condition
5.41	16.23	FSYSCLK = 20MHz; Timer0 running; all peripherals enabled.
5.38	16.14	FSYSCLK = 20MHz; Timer0 running; ADC is ON.
1.91	5.73	FSYSCLK = 20MHz; Timer0 running; I^2C is ON.
1.91	5.73	FSYSCLK = 20MHz; Timer0 running; ESPI is ON.
1.91	5.73	FSYSCLK = 20MHz; Timer0 running; LIN-UART is ON.
1.92	5.76	FSYSCLK = 20MHz; Timer0 running; PWM is ON.
1.91	5.73	FSYSCLK = 20MHz; Timer0 running; all peripherals disabled.
1.90	5.70	FSYSCLK = 20MHz; Timer0 disabled; all peripherals disabled.

Note: When the ZNEO CPU is in HALT Mode, current is measured in milliAmps (mA) and the 3.0V power supply is measured in milliWatts (mW).

Table 3. STOP Mode

Current Consumed	Power	Condition
458.2	1375	WDT running; VBO enabled; all peripherals disabled.
456.1	1368	WDT not running; VBO enabled; all peripherals disabled.
2.4	7.2	WDT running; VBO disabled; all peripherals disabled.
0.2	0.6	WDT not running; VBO disabled; all peripherals disabled.

Note: When the ZNEO CPU is in STOP Mode, current is measured in microAmps (µA) and the 3.0V power supply is measured in microWatts (µW).

Peripheral-Level Power Control

The on-chip peripheral functions on the ZNEO Z16F Series of MCUs automatically enter a low-power mode after RESET and whenever a peripheral function is disabled. To minimize power consumption, unused peripherals must be disabled. See the individual peripheral chapters in the ZNEO Z16F Series Product Specification (PS0220) for specific register settings to enable or disable each peripheral.

Note: If peripherals are not used, the user can turn them off to reduce power consumption in all modes.

Power Control Option Bits

See the individual peripheral chapters for specific register settings to enable or disable each peripheral. User-programmable option bits are available in some versions of the devices that enable very-low-power STOP Mode operation. These options include disabling the VBO protection circuits and disabling the WDT oscillator. For a detailed description of the user options that affect power management, see the Option Bits chapter in the ZNEO Z16F Series Product Specification (PS0220).

Hardware Architecture

The ZNEO CPU is equipped with several user-controlled power saving features. By placing the CPU into STOP or HALT modes, or by disabling the peripherals via the Control Register when specific functions are not needed, power consumption can be minimized. See Appendix A. ZNEO CPU Architecture on page 10 for a block diagram of the ZNEO CPU hardware architecture.

Software Implementation

This reference design makes use of ZDSII – ZNEO 4.12.0 and the ZNEO 16F Series of MCUs to simulate low-power operation using STOP and HALT modes; it also employs the Peripheral Control Register and option bits settings. Our purpose is to implement these low power operations in a blinker program. To begin, we configured Flash Option bits 0–3 with the corresponding values listed below.

```
FLASH_OPTION0 = 0xF7;
FLASH_OPTION1 = 0xFC;
FLASH_OPTION2 = 0xFF;
FLASH_OPTION3 = 0x3F;
```

The above values serve to disable both the VBO protection circuit and the WDT oscillator.

Warning: The operation will program the Flash Option bits at addresses 0–3 with data other than FF. You may lose your ability to reconnect to the target if incorrect option bits are programmed. Please review the Option Bits chapter of the ZNEO Z16F Series Product Specification (PS0220) for the appropriate option bits data.

Next, we configured the GPIO pins for output, with the exception of the pins that govern Stop-Mode Recovery. Here, we use PA4–PA7 as the Stop-Mode Recovery pin using the following value.

```
PASMRE = 0xF0;
```

We next configured all peripherals to be disabled; these peripherals can be enabled anywhere in the code, as required.

To achieve additional power savings, we can turn the peripherals ON and OFF using their respective control registers; these values can be changed from 0x0000 to 0xFFFF depending on your configuration requirements. By setting or clearing the EN bit of the Peripheral Control Register, the peripheral block will be enabled or disabled, respectively.

Example 1. Blinker Program

The following code segment demonstrates where to insert your low power mode instructions after the blinker routine. This code segment will work for 15 cycles/blinks. After 15 cycles, if the CPU has no data to execute, it will return to STOP or HALT mode and await an interrupt to repeat blinker code execution.

```
    while(1)
    {
        for(y=0;y<30;y++)
        {
            PAOUT = ~PAOUT;
            delay();
        }
        PAOUT = 0xFF;

/********* Place your mode instructions here **********/
    }
```

Mode Instructions and Definitions

This section describes the Low Power Mode instructions and how the ZNEO CPU functions upon their execution.

The ASM("STOP") instruction places the device into STOP Mode.

The ASM("HALT") instruction places the device into HALT Mode.

void Init_osc(void); This function initializes the oscillator; it is required in both HALT and STOP modes to enable the internal precision, crystal and watchdog timer oscillators.

void Init_wdt(void); This function initializes the Watchdog Timer. Set its reload values to specify a time-out delay. The typical value of the WDT Reload Register is `0x0400`, which yields 102.4ms; a maximum value of `0xFFFF` corresponds to a 6.55-second time-out delay before RESET.

Caution: The 16-bit WDT Reload Value must not be set to a value less than `0004H`.

void Init_Timer0(void); This function initializes Timer0 for HALT recovery time. Set the mode, pre-scalar, initial and reload values to allow the ZNEO CPU to reset from HALT Mode for a specified time.

void GPIO_init(void); This function initializes the GPIO. It sets functions, directions and other operations related to GPIO.

void Timer_init(void); This function initializes a timer that was not used in the application.

void wdt_en(void); Enable the WDT to RESET for a specified time-out delay. Start the WDT.

void init_t0int(void); Enable Timer0 to RESET for a specified time. Start Timer0.

For additional code detail, refer to the AN0324-SC01.zip source code file that accompanies this application note.

Equipment Used

- ZNEO Z16F Series Development Kit (Z16F2800100ZCOG)
- ZDSII version 4.12.0 for the ZNEO CPU
- Multimeter
- Power supply

Setup

Figure 2 illustrates the connection of the ZNEO CPU to the power supply with an ammeter inserted in series between them. In Figure 3, a depopulated ZNEO Development Board is shown to ensure that only the ZNEO MCU consumes current from the source.

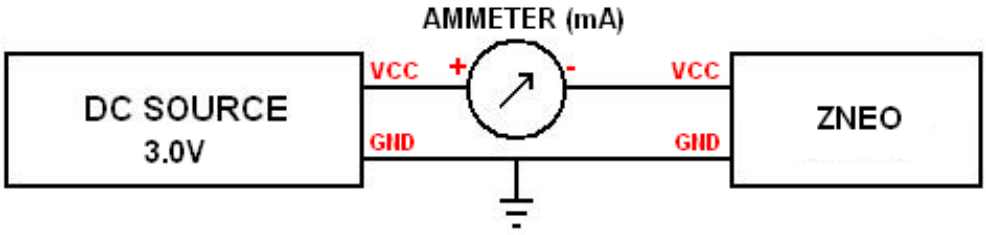

Figure 2. Setup Block Diagram

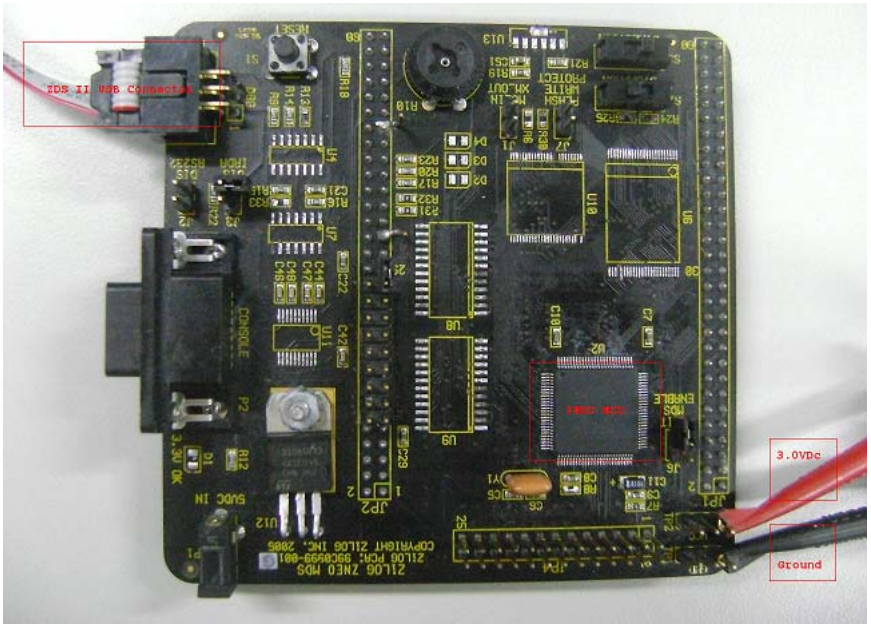

Figure 3. Depopulated ZNEO Board Showing Connections

Results

Each mode of operation offers a significant reduction in power consumption. See Tables 1 through 3 for measurements of current and power in different modes under differing conditions.

When taking the other components in the ZNEO Z16F Series Development Kit into account, the data resulting from this project shows current consumption to be higher than is indicated in the ZNEO Z16F Series Product Specification (PS0220).

Summary

This Application Note provides a template to utilize the low-power features of the ZNEO Z16F Series of MCUs. Differing conditions shown in Tables 1 through 3 are provided to illustrate the different low-power mode possibilities. The software is modular and easy to customize for any low-power application.

References

The following documents associated with the ZNEO Z16F Series of MCUs are available on www.zilog.com.

- ZNEO Z16F Series Product Specification (PS0220)
- ZNEO Z16F Series Development Kit User Manual (UM0202)

Appendix A. ZNEO CPU Architecture

Figure 4 displays the architecture of the ZNEO Z16F Series of MCUs.

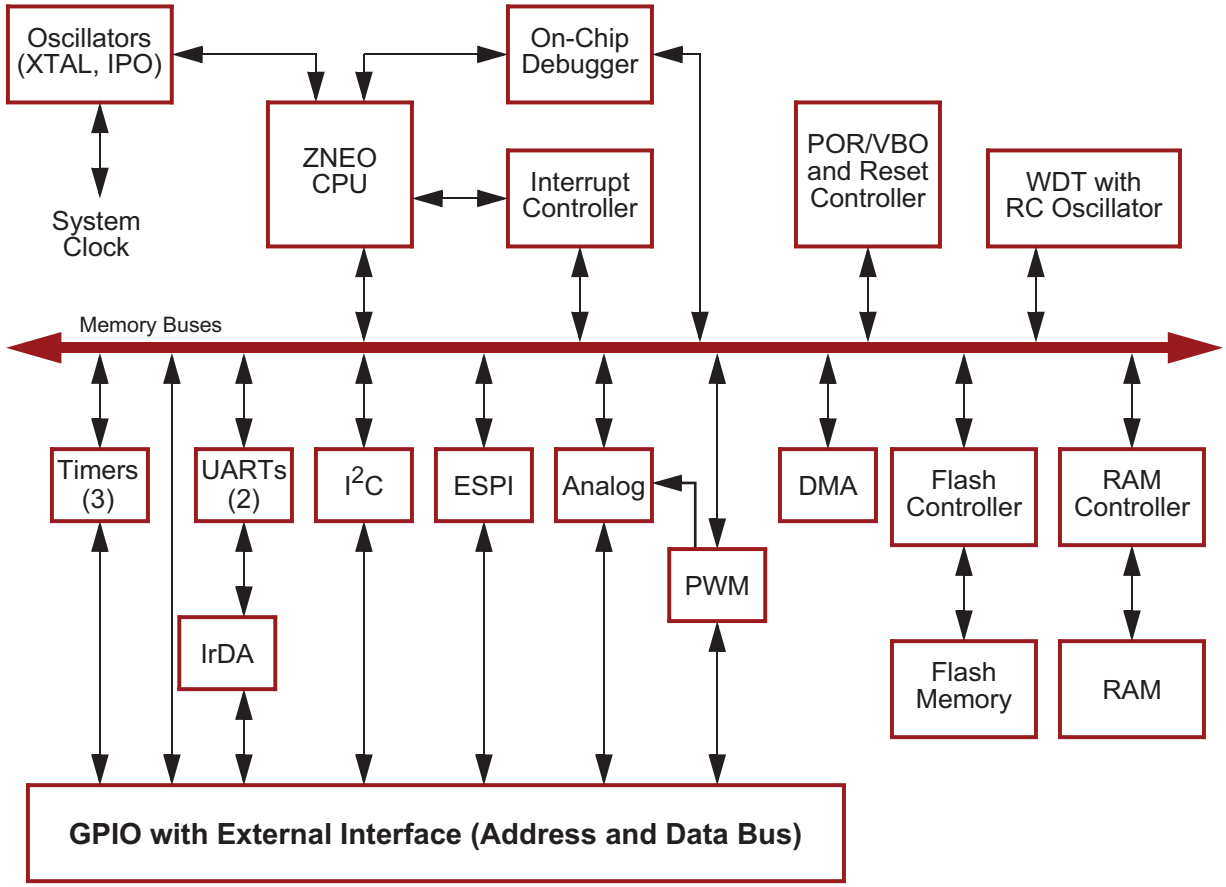

Figure 4. ZNEO Z16F Series Block Diagram

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