

Product Update

UP008706-0207

Errata for ZNEO[™] Z16F Series Devices

ZNEO Z16F Series MCU with Any Date Code

The errata listed in Table 1 are found in the Revision AB silicon for the ZNEO Z16F Series product with any package date code.

No.	Issue	Detailed Description
1	ADC INL error does not meet specification lim- its when analog inputs, ANA[11:0], are below 100 mV.	The ADC INL error is greater than 3 LSB when the analog inputs, ANA[11:0], are below 100 mV. The INL error can be as high as 5 LSB when below 100 mV.
2	ADC Gain error does not meet specification limits.	The ADC Gain error for worst case conditions is $\pm 2.5\%$ of the full range instead of the ± 4.5 LSB specified. The typical gain is less than 1%.
3	64K Flash parts can- not be set to 32K by the user.	There are two control bits that set the usable Flash size in the ZNEO Z16F Series parts. They are decoded as follows: 00 - 128K 01 - 64 K 10 - 32K 11 - no memory - ROMless These bits are in the EXTCT register describe in the "External Interface" chapter of the ZNEO Product Specification. The register allows the user to select a smaller usable Flash memory size but not a larger Flash memory size.
4	POPF instruction corrupts R3	The execution of the POPF instruction results in the R3 register being over- written by random data. As a workaround, in place of POPF, the following instruction sequence can be used: PUSH #NextInst IRET2 NextInst: Here, IRET2 is an alternative form of IRET, which is required in this context to avoid problems with chained interrupts. Its op code is FFF6. The ZiLOG assembler currently applies this substitution for POPF automat- ically.

Table 1. Errata to the ZNEO Z16F Series Devices



Table 1. Errata to the ZNEO Z16F Series Devices (Continued)

No.	Issue	Detailed Description
5	Hardware breakpoint does not catch word accesses of the byte	When a hardware breakpoint is configured to break on an address byte, the breakpoint does not catch word accesses of the byte.
		Workaround There is an address mask to break on a range of addresses. Configure the mask to ignore address bit 0.



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