Technical Note

Enhancing ADC Resolution of Z8 Encore! XP® MCU from 10 bits to 12 bits

TN005402-1107

Introduction

This Technical Note discusses a method of enhancing on-chip 10-bit analog-to-digital converter (ADC) to 12-bit resolution. This Technical Note describes the algorithm that can be used with Zilog's Z8 Encore! XP® MCU for the applications that need 12-bit ADC resolution.

In applications such as intelligent battery charging, feedback control systems, and precision temperature measurement, an ADC with 10-bit resolution may not be sufficient to obtain appropriate results. In these applications 12-bit resolution may be required. However, using a separate higher-resolution ADC for accurate measurement increases the system hardware cost. An alternative approach is to utilize signal processing techniques in conjunction with the 10-bit ADC conversion to achieve 12-bit resolution.

The source code library for the algorithm explained in this document is available as Z8 Encore! XP utility on www.zilog.com.

Overview of ADC in Z8 Encore! XP MCU

Z8 Encore! XP has an on-chip Sigma-Delta ADC. It can be used in SINGLE-ENDED or DIFFERENTIAL mode. In SINGLE-ENDED mode, there are 8 individual channels which can be used for measurement. In DIFFERENTIAL mode, 11 pairs of differential inputs are available.

Internally, ADC provides 13 bits of data (12 data bits + 1 sign bit). Two least-significant bits (lsb) out of these 12 data bits are used for rounding purpose. After rounding, ADC provides 10 data bits for DIFFERENTIAL/SINGLE-ENDED mode and 1 sign bit for DIFFERENTIAL mode.

The ADC can be configured for single-shot conversion or continuous conversion mode. In SINGLE-SHOT mode, ADC requires 5129 clock cycles for conversion while in CONTINUOUS mode, it requires 256 clock cycles.

Discussion

In any ADC, quantization noise is present. This is because the digital signal can be represented as either 0 or 1. If the digital signal is in-between 0 and 1, then the digital signal appears as 0 or 1. The rounding error between the analog input and the digitized output is termed as quantization noise.

If the signal to be measured is oversampled, this quantization noise is spread over a large spectrum and by passing this through a digital filter that has a narrow bandwidth, the quantization error can be reduced and thereby increasing the resolution. The Sigma-Delta ADC utilizes this technique by using a modulator which oversamples the signal to spread the quantization noise over a large spectrum. The signal from the modulator is passed through a digital 'low pass filter', which has a sharp roll-off.

Figure 1 displays the two blocks of a Sigma-Delta ADC.

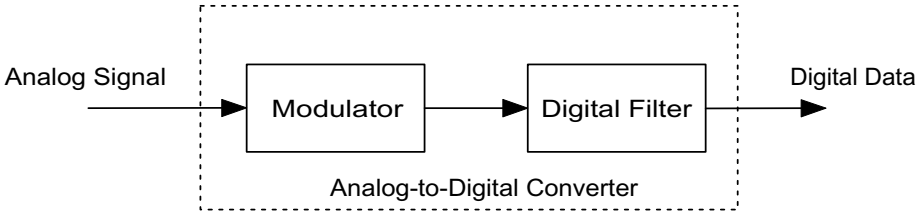

Figure 1. Block Diagram of Sigma-Delta ADC

The Modulator block has high speed clock source which is required for oversampling. Due to this high speed clock, noise is generated and imposed on the signal. This noise can be characterized and therefore an algorithm is developed using signal processing techniques to increase ADC resolution. Figure 2 displays the effect on the signal after oversampling and using digital filter in a Sigma-Delta ADC.

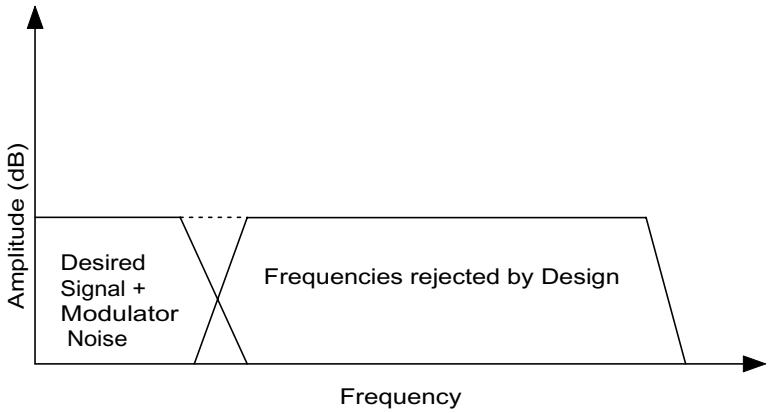

Figure 2. Frequency Response of Sigma-Delta ADC

The Modulator noise limits the actual ADC resolution. In Z8 Encore! XP quantization error is expected to be within ½ LSB at 12-bit resolution. The energy of non-linear product of modulator noise and quantization can be reduced by reducing bandwidth of the signal thus increasing resolution. The proposed algorithm is based on additional averaging of ADC data samples and utilizing the SINGLE-SHOT and CONTINUOUS ADC modes.

Algorithm

This technical note describes the algorithm implemented in the software to eliminate the modulator noise. Figure 3 illustrates the flow of algorithm.

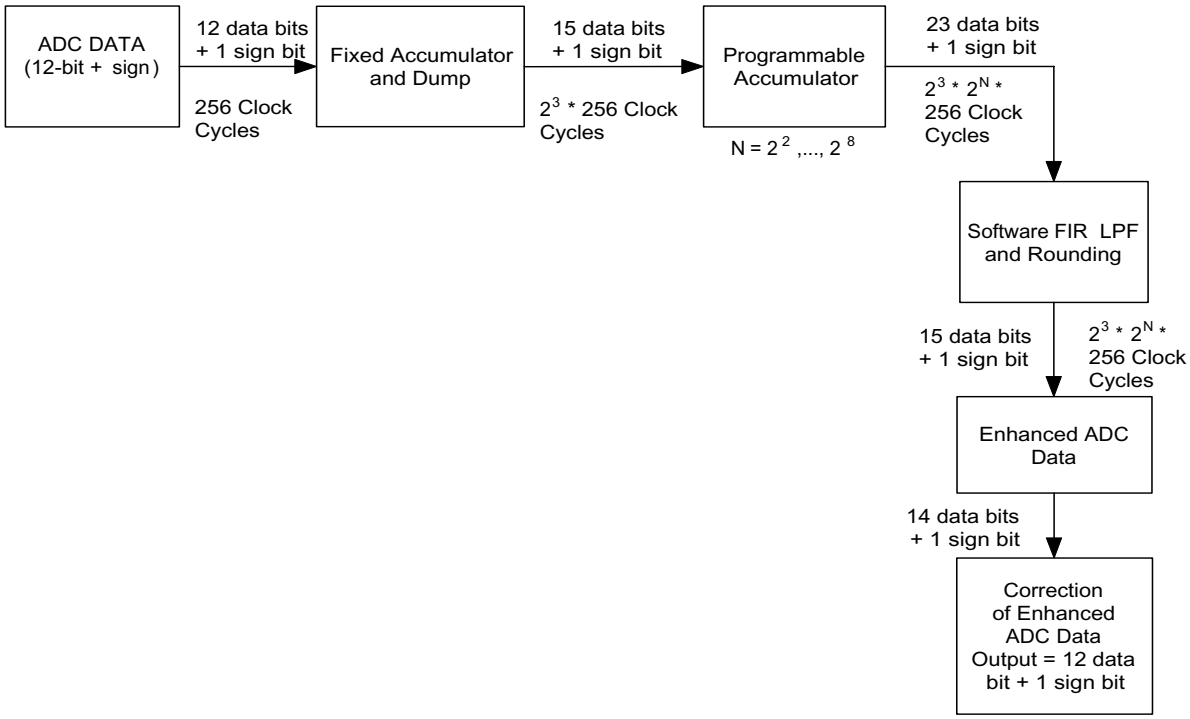

Figure 3. Block Diagram of the Algorithm Implemented

In the above algorithm, ADC is configured for CONTINUOUS mode, where a sample is available at every 256 clock cycles, except the first conversion. These samples are accumulated and passed through a filter (that is, signal value is multiplied with filter response) to get an average value. This average value has a resolution of 14 bits. Finally, this average value is multiplied with a correction factor (by reading offset and gain calibration constants) to get a 12-bit accurate value.

Conclusion

Using this algorithm the Z8 Encore! XP on-chip ADC precision can be greatly enhanced. This example describes how the ADC can be improved to 12-bit resolution. The same approach can be used further to enhance the ADC accuracy by increasing the over-sampling rate. The trade-off for this improvement is reduced ADC sample speed and increased code size.

In the sample provided the entire code size is 1K of memory with algorithm taking 760 bytes and rest of the code is used for printing data to the UART. The code is implemented in such a way that it can be ported and integrated to any other application with minimum changes. This software is specific to the Z8 Encore! XP on-chip ADC.

References

For more information on Z8 Encore! XP, refer to the following documents:

- PS0228 - Z8 Encore! XP 4K Series Product Specification
- UM0187 - Z8F04A08100KIT Z8 Encore! XP 4K Series 8-Pin Development Kit User Manual

These documents are available for download at www.zilog.com.

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