Application Note

Migrating from the Z8 Encore! XP® F640x to the Z8 Encore! XP® F64XX MCU

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Z8 Encore! XP® Flash Microcontrollers

Abstract

In an effort to provide you with the highest-quality embedded microcontroller (MCU) solutions, Zilog® has implemented a policy of continuous product improvement. With each opportunity to revise silicon, Zilog will implement product improvements and feature enhancements. These changes will be implemented in backward-compatible fashion so that the effort to migrate from the current version of the silicon to the new version is easy.

In addition, Zilog will maintain all versions of available products for the longest possible time. If you are committed to use an earlier version of a product appropriate for your project requirements, then you will not be forced to requalify and migrate to a newer version. As a result, you have the flexibility to take advantage of new product features, and if so, the impact to your existing design will be minimal.

Zilog's Z8F64XX devices are members of Zilog's Z8 Encore! XP® Flash MCU family. They are the first products in the Zilog portfolio to undergo this approach. This application note highlights the differences between the Z8F640x and the Z8F64XX devices. It reviews what needs to be addressed when migrating an application/design from a Z8F640x device to a Z8F64XX device.

In this migration, there are three Z8F642 differences that impacts an existing design. All other differences are unlikely to impact existing application designs. Table 1 lists the applicable devices.

Table 1. Device Migration Cross-Reference Table

From	Z8F6401 Z8F6402 Z8F6403	Z8F4801 Z8F4802 Z8F4803	Z8F3201 Z8F3202	Z8F2401 Z8F2402	Z8F1601 Z8F1602
To	Z8F6421 Z8F6422 Z8F6423	Z8F4821 Z8F4822 Z8F4823	Z8F3221 Z8F3222	Z8F2421 Z8F2422	Z8F1621 Z8F1622

Feature Differences

There are three categories of change between Z8F640x and Z8F64XX in Zilog's Z8 Encore! XP® block diagram. They are as follows:

New, upward-compatible feature additions	Modules in this category are upward-compatible and contain new features. Existing features are not affected. Upward-compatible is defined as new features using unimplemented register bits and the modules operate similarly as long as the bits were written as 0. Existing application designs are not impacted.
Modified and enhanced	Modules in this category contain some modified and/or enhanced features. Application designs might be impacted by this change.
No change	Modules in this category contain identical features, are functionally compatible, and application design is not impacted.

Figure 1 displays an overview of the modules that are different between Z8F640x and Z8F64XX.

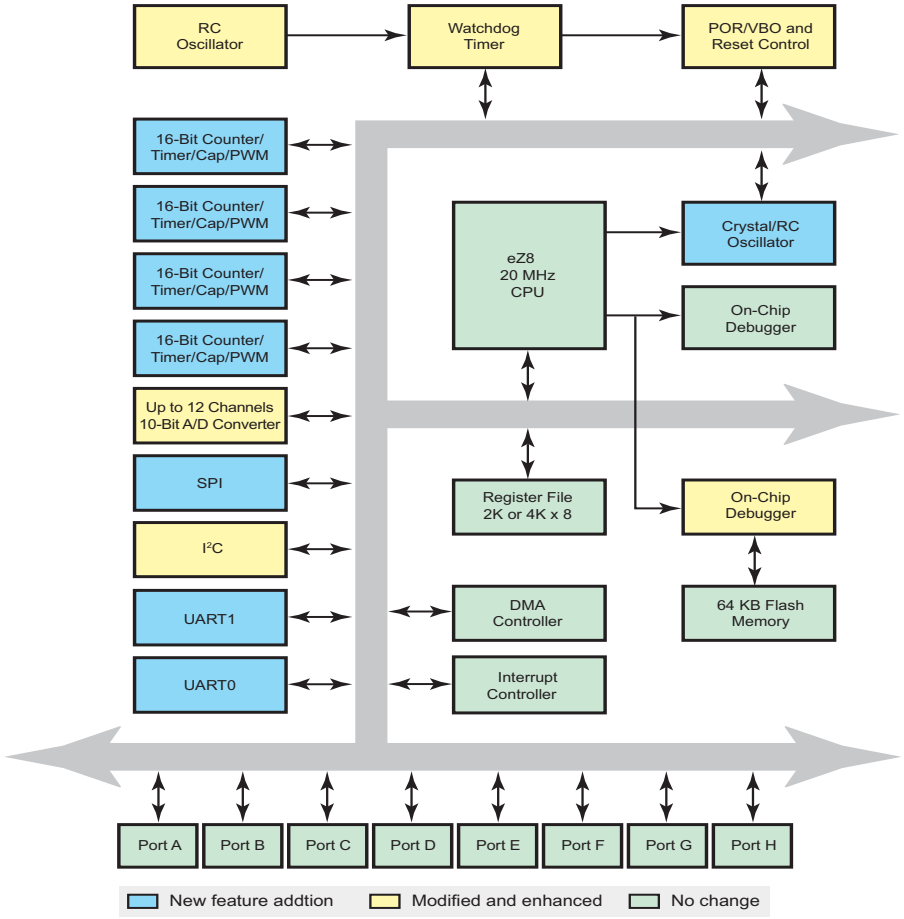

Figure 1. Z8 Encore! XP® Z8F64XX Block Diagram

Table 2 lists the feature differences and impact between Z8F640x and Z8F64XX. For convenience, it is color-coded to correspond to Figure 1 on page 2.

Table 2. Feature Differences Summary

Z8F640x Feature	Z8F64XX Difference	Description	Existing Design Impact
Data RAM	No change	2 KB or 4 KB SRAM.	No impact
eZ8 CPU		20 MHz operation.	
GPIO pins		Up to 60 GPIO pins.	
Infrared endecs		2 IrDA-compliant encoder/decoders.	
Interrupt controller		24 interrupts with configurable priority.	
On-chip debug		1-pin interface.	
Package and pin compatibility		80-pin QFP, 68-pin PLCC, 64-pin LQFP, 44-pin PLCC, 44-pin-LQFP, 40-pin PDIP.	
Peripherals, register map, and bit locations		256 locations; only previously reserved locations and bits used to add new features.	
Power supply		3.0–3.6 V.	
Program memory		Up to 64 KB Flash.	
WDT RC oscillator	Modified and/or enhanced	Modified to 10 kHz low-current RC oscillator.	Software: WDT time-out delay impacted.
Reset, DBG, and SMR pin filtering		Filtering on select pins to improve noise immunity.	Reset pulse must be a minimum of 4 system clock cycles.
Flash protection		Enhanced multiple sector protection.	Software: Flash program/erase procedure impacted
I^2C		The START, STOP, and NAK bits in the I^2C Control Register can be cleared by writing a 0 to these bits.	Software: Writes to the I^2C Control Register are impacted.
I/O pads		All digital pads are 5 V-tolerant.	No impact
Reset and STOP mode timing		Modified to 66 RC clocks to accommodate change to 10 kHz low-current RC oscillator.	
Power and EMI reduction		Automatically disables clock to idle and disables peripherals.	
ADC		• Interrupt after every conversion in CONTINUOUS mode • Latch ADC low byte during read • ADC defaults to external V_{REF} upon reset	
VBO		Flash option to disable VBO in STOP mode.	

Table 2. Feature Differences Summary (Continued)

Z8F640x Feature	Z8F64XX Difference	Description	Existing Design Impact
Crystal/RC Oscillator	New, upward-compatible feature addition	Two additional power modes and an external RC mode.	No impact
UART		• Automatic address matching in MULTIPROCESSOR mode • Optional driver enable output for external bus transceivers • All UART interrupts that were formerly of the CONTINUOUS assertion type are now of the ONE-SHOT type	
Timers		New cascade feature to connect the output from one timer to the input of the next timer.	
SPI		New bit to indicate Slave mode transaction abort.	

Modifications and Migration Impact

The following sections describe the features that are modified and/or enhanced in the Z8F64XX, and their impact on any Z8F640x designs.

Watchdog Timer (WDT)/RC Oscillator

Modifications

There are two changes to the WDT peripheral for Z8F64XX devices:

1. A new low-power 10 kHz RC oscillator replaces 50 kHz oscillator of Z8F640x, resulting in a WDT time-out delay range of 400 µs to 1677.5 s.
2. The WDT Control Register at address FF0h permits a new control sequence to disable the WDT/RC oscillator in STOP mode.

Impact

Following are the impacts:

- Because of the new RC oscillator, the typical STOP Mode current with the WDT running is reduced and expected to be in the range 2 to 5 µA.
- The WDT time-out delay calculation is now based on the new 10 kHz RC oscillator frequency. Therefore, software initialization of the WDT reload registers could require modification for new delay constants.
- Application software can now optionally disable the WDT/RC oscillator to further reduce STOP Mode current.

Reset and Stop Mode Latency

Modifications

The latency for System Reset and Stop Mode Recovery of Z8F64XX devices is changed to 66 WDT clock cycles plus 16 system clock cycles. In Z8F640x devices, this value was 514 WDT clock cycles plus 16 system clock cycles. This modification accommodates a WDT/RC oscillator frequency change from 50 kHz to 10 kHz. With this change, overall Stop Mode Recovery delay is reduced.

Impact

There is no direct impact on existing Z8F640x designs because of this change. Overall, the system recovers from Reset and STOP mode faster.

Table 3 lists the timing differences between Z8F640x and Z8F64XX.

Table 3. Timing Differences

Reset Type	Z8F640x (ms)	Z8F64XX (ms)
System	10.28	6.6
Short*	1.32	6.6
Stop	10.28	6.6

Note: *Short Reset is replaced by System Reset in Z8F64XX.

Flash Protection

Modifications

The Flash protection scheme is enhanced in Z8F64XX silicon. The following modifications achieve a higher granularity of protection and flexibility:

- Flash Memory is divided into eight sectors, each of which can be individually protected. User software can select different Flash sectors for protection.
- Page-level division of Flash Memory is maintained. Only pages of an unprotected sector can be programmed or erased. For an added level of protection, user software must reconfirm any page number selected for unlocking.
- Page-level protection is enhanced to confine byte programming only within an unlocked page.
- A mass erase is permitted only through the debug port. Application software cannot perform a mass erase.

Impact

Application-level Flash Erase and Flash Program routines are impacted by this change.

I^2C

Modifications

The START, STOP, and NAK bits in the I^2C Control Register is cleared by writing a 0 to these bits. In Z8F640x devices software can only set, but not clear these three bits.

Impact

Software should not inadvertently clear the I^2C Control Register bits.

I/O Pads

Modifications

In Z8F64XX silicon, the digital I/O pads are 5 V tolerant except for the Port B and Port H pins that support the ADC alternate function. The remaining port pins (ports A, C, D, E, F, and G) tolerate up to 5.5 V.

Impact

This modification adds flexibility so that applications can use 3.3 V compatible interfacing to lower power consumption, and 5 V compatible interfacing where it cannot be avoided. There is no direct impact on existing Z8F640x designs.

Reset, Debug, and Stop Mode Recovery Filtering

Modifications

The following modifications are incorporated to improve noise immunity in Z8F64XX devices:

- A digital filter is added to the $\overline{\text{RESET}}$ input pin signal to reject pulses less than four system clock periods. This filter works only in ACTIVE and HALT modes. It does not work in STOP mode when the System Clock is disabled. When the $\overline{\text{RESET}}$ pin is asserted for at least four system clock cycles the device progresses through the System Reset sequence.
- A 10 ns (min) analog glitch filter was added to the Stop Mode Recovery signals, DBG, and $\overline{\text{RESET}}$, to prevent glitches from causing an exit from STOP mode. All Stop Mode Recovery sources are ORed together and then filtered. The DBG and $\overline{\text{RESET}}$ pins contain their own filters.

Impact

Applications using external $\overline{\text{RESET}}$ input must ensure the reset pulse is, at minimum, four system clock periods.

Power and EMI Reduction

Modifications

The clock to any idle or disabled peripherals is automatically disabled, reducing switching currents. As a result, power and EMI are reduced.

Impact

Existing designs are not impacted by this change.

Analog-to-Digital Converter

Modifications

The following modification are incorporated:

- In CONTINUOUS mode, the Analog-to-Digital Converter (ADC) generates an interrupt request after every conversion. In Z8F640x devices, an interrupt is generated only once, and only after the first conversion. New data is generated every 256 cycles. An interrupt request is not sent for subsequent conversions.
- Reading the ADC High Byte register latches data in the ADC Low Bits register.
- ADC defaults to external V_{REF} up on reset. In Z8F640x devices, the default is internal V_{REF}. This change avoids any contention on V_{REF} pins if using an external voltage reference.

Impact

As an interrupt is generated after every conversion, there is no need to perform a Busy Wait. Nor there is a need to use up a system timer to generate interrupts, every 256 cycles, before reading subsequent data.

Voltage Brownout

Modifications

A new Flash option bit allows Voltage Brownout (VBO) to be either enabled or disabled in STOP mode.

Impact

The Flash option bit is a feature that aids power reduction in STOP mode. Existing designs are not impacted by this change.

New Features

This section reviews the new features supported in the Z8F64XX family. For complete descriptions, refer to the appropriate Z8 Encore! XP product specification.

Oscillator Modes

The Z8F64XX product supports three new oscillator power modes in addition to the default maximum power high-frequency crystal mode in Z8F640x devices. These modes are:

- External RC mode—for use of the on-chip oscillator with external RC networks (< 4 MHz).
- A minimum power mode—for use with very low-frequency crystals (32 kHz to 1.0 MHz).
- A medium power mode—for use with medium-frequency crystals or ceramic resonators (0.5 MHz to 10.0 MHz).
- A maximum power mode—for use with high-frequency crystals (8 MHz to 20 MHz).

The oscillator mode is selectable using the user-programmable Flash option bits.

Universal Asynchronous Receiver/ Transmitter

The Z8F64XX Universal Asynchronous Receiver/ Transmitter (UART) supports three new upward-compatible feature additions as described below:

1. An automatic Address Compare feature in MULTIPROCESSOR mode
2. An optional Driver Enable signal
3. One Shot interrupts

Address Compare

When enabled, the UART automatically checks whether incoming address bytes match the address of the UART. When an incoming address byte does not match the UART's address, it is ignored. All successive data bytes contained in the frame are also ignored. When a matching address byte occurs, an interrupt is optionally issued and further interrupts occur up on each successive data byte. The Address Compare feature reduces the load on the CPU because it does not need to access the UART when it receives data directed to other devices on the multi-node network.

External Driver Enable

The UART provides an optional Driver Enable (DE) signal for off-chip transceivers. This feature reduces the software overhead associated with using a GPIO pin to control the transceiver when communicating on a multi-transceiver bus such as an RS-485. This DE feature also improves bus availability.

One Shot Interrupts

One Shot Interrupts have replaced Continuous Interrupts for the UART and are cleared by accessing only the UART TxD register for transmits or the UART RxD register for receives. This feature reduces software overhead associated with handling UART Interrupts.

Timers

The Z8F64XX Timer Control register supports a new cascade control bit, which allows the output from one timer to be connected as the input of the next. This feature allows applications to cascade one timer to another without connecting two external pins. Timer cascading can be used to generate a very low-frequency timing control while running the eZ8 CPU at high clock speeds.

SPI

To improve abort recovery and reduce data error, the Z8F64XX SPI Status register supports a new Slave mode transaction Abort bit (ABT). Application software can check this bit to determine if a Slave mode transaction is aborted before completion.

References

The document associated with Z8 Encore! XP® available on www.zilog.com is provided below:

- Z8 Encore! XP F64XX Series Product Specification (PS0199). This document discusses Z8F64XX, Z8F482x, Z8F322x, Z8F242x, and Z8F162x devices.

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