Errata for Z8 Encore! XP® F0822 Series MCUs

UP005812-0811 **Product Update**

When reviewing the following errata, note that date codes are in the format YYWW, representing the year and week of assembly. Zilog recommends downloading the most recent version of the Z8 Encore! XP F0822 Series Product Specification from zilog.com. For further assistance, contact Zilog Customer Service.

Z8 Encore! XP F0822 Series with All Date Codes

The errata listed in Table 1 are found in F0822 Series devices with all date codes.

Table 1. Z8 Encore! XP F0822 Series Errata for Devices with All Date Codes

No.	Summary	Description
1	IrDA has excessive error rate.	Due to insufficient synchronization, pulse widths less than 2.17µs can result in data corruption or loss of synchronization depending on the data being sent. The IrDA specification permits a minimum pulse width of 1.41µs. **Workaround** An external synchronizing circuit can be used to capture and synchronize data to the device. Possible software solutions exist. Contact Zilog technical support for further information.

Z8 Encore! XP F0822 Series with Date Codes 0402 to 0850

The errata listed in Table 2 are found in F0822 Series devices with date codes 0402 to 0850.

Table 2. Z8 Encore! XP F0822 Series Errata for Devices with Date Codes 0402 to 0850

No.	Summary	Description
1	Read Protect Option Bit may be bypassed.	The Read Protect (RP) Option Bit does not prevent Flash access when bypassing the Flash Controller, as described in the Third Party Flash Programming Support for Z8 Encore! MCUs Application Note (AN0117). User code cannot be read through the On-Chip Debugger when Read Protect is enabled. User code can only be read out when bypassing the Flash Controller. **Workaround** None.
2	Device may not complete Stop Mode Recovery initiated by a GPIO pin transition.	When Stop Mode Recovery (SMR) is initiated by a GPIO pin transition, multiple pin transitions within (approximately) 200ms of each other can cause the device to only partially wake from STOP Mode. In this situation, the device idles in a state between STOP Mode and normal operation. The crystal oscillator is oscillating, but code does not execute. When stuck in this idle state, assertion of the external RESET pin does not initiate a system Reset. **Workarounds** 1. Add external filtering to the Stop Mode Recovery pin input signal to prevent multiple transitions during periods less than 200ms. 2. Next, enable the Watchdog Timer (WDT) in STOP Mode to allow a WDT to complete the Stop Mode Recovery process in the event that the device does not successfully complete the Stop Mode Recovery initiated by the GPIO pin transition.

Z8 Encore! XP F0822 Series with Date Codes Prior to 0402

The errata listed in Table 3 are found in F0822 Series devices with date codes prior to 0402.

Table 3. Z8 Encore! XP F0822 Series Errata for Devices with Date Codes Prior to 0402

No.	Summary	Description
1	When the CPU exits from Halt mode, it fails to reset the master Interrupt Request Enable (IRQE) bit.	When the CPU exits from HALT Mode, it fails to reset the master Interrupt Request Enable (IRQE) bit (bit 7 of the Interrupt Control Register). WDT interrupts cause the Program Counter (PC) and flags to be pushed twice onto the stack. The first push is the PC and flags from where the interrupt occurred. The second push is the starting address and flags of the Interrupt Service Routine (ISR). This problem also affects exits from HALT Mode caused by other interrupt sources if more than one interrupt is pending. If only a single interrupt is pending, then the routine executes normally, with the exception that interrupts are not disabled. **Workaround** To mimic standard interrupt operation, the ISR executes a Disable Interrupts (DI) instruction to reset the master Interrupt Request Enable (IRQE) bit to 0. Furthermore, on WDT interrupts before exiting, the ISR adds three (3) to the Stack Pointer (SP). Upon a normal interrupt, the ISR checks the Program Counter on the stack. If this Program Counter contains the starting address of the ISR, then the ISR adds three (3) to the Stack Pointer (SP). This problem only affects exits from HALT Mode.
2	On-Chip Debugger does not support hardware breakpoints.	The On-Chip Debugger does not break when the Program Counter (PC) equals the value written to the OCD Counter Register or when the OCD Counter decrements to zero. **Workaround** The other breakpoint functions available from the On-Chip Debugger can be used for debug operations.
3	System Reset latency may exceed specification limits.	When exiting STOP Mode, and after a POR/VBO reset, the System Reset Latency is 514 WDT cycles plus 16 System Clock cycles, rather than the 66 WDT cycles plus 16 System Clock cycles, as specified. **Workaround** None. This error is unlikely to affect system operation.
4	UART NEWFRM status bit does not function.	The NEWFRM status bit (Bit 2 of the UART Status 1 Register) does not indicate the start of a new frame. **Workaround** None.
5	UART Address Compare function does not work.	Setting Bit 7 (MPMD[1]) of the UART Control 1 register to 1 does not produce the desired effect of enabling the UART Address Compare and associated interrupt functionality. **Workaround** MPMD[1] must remain in its reset state of 0.

Table 3. Z8 Encore! XP F0822 Series Errata for Devices with Date Codes Prior to 0402

No.	Summary	Description
6	UART Baud Rate Generator cannot be used as simple timer.	Setting BRGCTL (Bit 2 of the UART Control 1 register) to 1 when the UART receiver is disabled does not enable UART Baud Rate Generator interrupt. Thus, the UART Baud Rate Generator cannot be used as a simple timer. **Workaround** Use one of the 4 standard Timers or the Baud Rate Generators in the SPI or I^2C blocks to perform the appropriate timing operations.
7	Unlocking the Flash Controller allows program and erase operations on all Flash pages.	During the Flash Controller unlock sequence, the specification indicates that a second write to the Flash Page Select register is required (step 5 of the sequence) to unlock the Flash Controller for the selected Flash page. The Flash controller unlocks for all Flash pages once steps 1-4 of the unlock sequence have been completed. **Workaround** None.
8	Setting bits in the Flash Sector Protect register to 1 does not lock sectors.	Writing bits in the Flash Sector Protect register to 1 fails to prevent program and erase operations on the selected Flash memory sector. **Workaround** None.
9	Watchdog Timer cannot be disabled in STOP Mode.	The Watchdog Timer and its associated internal RC oscillator cannot be disabled in STOP Mode. **Workaround** None.
10	Watchdog Timer oscillator frequency is out of specification.	The typical Watchdog Timer internal oscillator frequency is 50 kHz rather than the currently specified 10 kHz. This frequency can result in WDT time-out values that are less than expected. **Workaround** Increase the WDT reload value by a factor of 5 to compensate for the frequency error.
11	Operating currents	Operating currents in the various mode (Normal, HALT, and STOP) may be higher than typical values. **Workaround** None.
12	RESET pin is not filtered.	The RESET pin does not properly filter the input signal. The device may enter Reset when the RESET pin is asserted for less than the specified 4 system clock cycles (from NORMAL Mode). **Workaround** None.
13	Timers can not be cascaded	Setting the CSC bit (bit 4) of the Timer Control 0 registers does not cascade the timers, as indicated in the F0822 Series specification. **Workaround** Timers can be cascaded using the Timer Out and Timer In functions using the general-purpose I/O pins.

Table 3. Z8 Encore! XP F0822 Series Errata for Devices with Date Codes Prior to 0402

No.	Summary	Description
14	The START, STOP and NAK bits in the I^2C Control Register can be cleared by software writing a 0 to these bits.	The START, STOP and NAK bits in the I^2C Control Register can be cleared by software writing a 0 to these bits. The F0822 Series Product Specification states that these bits cannot be cleared by writing a 0. **Workaround** When writing to the I^2C Control Register, use the OR and AND instructions to ensure that these bits are not accidentally cleared.
15	LDWX load instruction not supported.	The LDWX load instruction is not supported and should not be used. **Workaround** Utilize the LDX instruction two times, once for each byte of the word.

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