Application Note

Technical Considerations for Z80185 and Z80195 Regarding Interrupt Edge Mode

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Abstract

This Application Note describes a method of changing the Interrupt Edge Mode Select while executing the main program code to avoid an unexpected interrupt.

Overview

Zilog's Z80185 and Z80195 are the smart peripheral controller devices designed for general data communications applications. These devices are specifically designed to accommodate all the input and output (I/O) requirements for serial and parallel connectivity. The Z80185 and Z80195 devices are useful in a broad range of applications by combining a high-performance CPU core with a variety of system and I/O resources. The Z80195 is the ROM-less version of the device.

Discussion

It is observed that changing the interrupt edge mode (by configuring the Interrupt Edge Register (IER)) and clearing the interrupt at the same time may result in an unexpected interrupt.

To resolve this issue, a procedure to change the IER is developed and is recommended for use in application using this feature of the Z80185.

Theory of Operation

The cause of this unexpected interrupt involves a race condition of the edge detect circuitry and the interrupt clear circuitry. Under normal circumstances, the edge mode select is changed by writing the edge mode select bits at the same time as the clear bits. However, it is possible that the edge detect circuit will latch in an interrupt before it is cleared. To avoid this situation, disable interrupts before the edge mode select is changed and later enable interrupts to continue with normal operation.

Changing the Interrupt Edge Mode Select

Using the following code segment, in the manner of changing the Interrupt Edge Mode Select and clearing it at the same time, may result in an unexpected interrupt.

```
LD A, #ACh
LD (DF), A
```

The above Opcode sets `INT1` and `INT2` to Falling Edge Detect and clears the interrupts at the same time. To avoid this unexpected interrupt, you must use the following code:

```
LD A, #ACh INT2
DI
LD (DF), A
EI
```

Summary

Based on testing and failure analysis, a race condition exists in the Z80185 that makes it possible for an unexpected interrupt to occur. This race condition involves only the IER. To avoid this situation it is recommended that while changing the IER, disable the interrupts before writing to IER and enable the interrupts once the write operation is complete to continue with normal operation.

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