Z86E02/E04/E08/E09 SL1995

Z8 CMOS OTP Microcontrollers

Programming Specification

PS009202-1203

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General Description

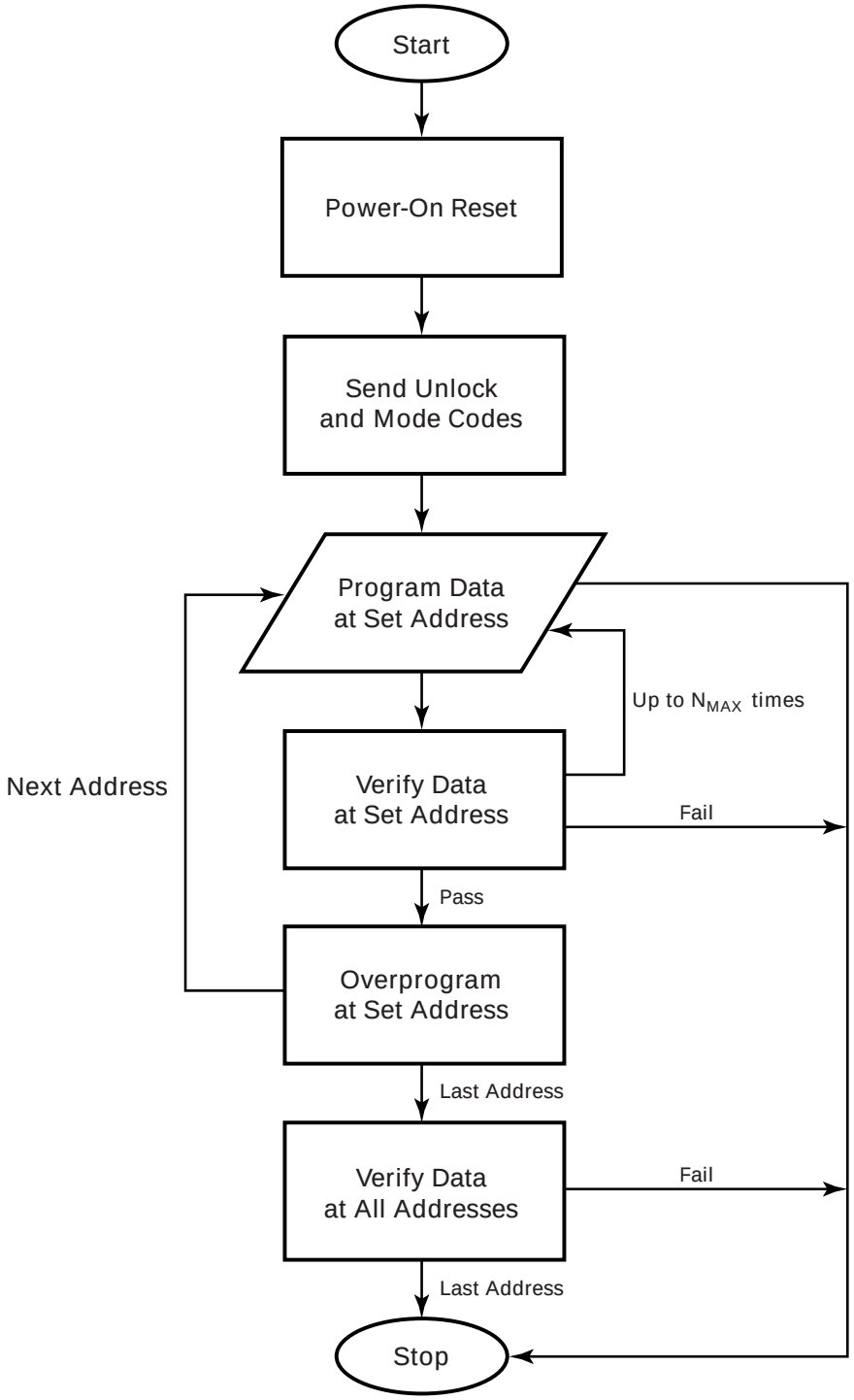
The EPROM Programming interface is a byte-wide data interface with 7 control inputs and a 17-wire connection. This document describes the EPROM interface pertinent to the following parts:

Z86E02 SL1995
Z86E04 SL1995
Z86E08 SL1995
Z86E09 SL1995

Top-Level Programming

After powering up, the programming sequence begins by sending the unlock code sequence, followed by the mode selection. The program address must be reset to 0000h after entering EPROM mode. The first data byte to be programmed is then loaded on Port 2. When the programming control sequence is applied, the programming pulse commences. Data is then verified for correct programming. If the data is incorrect, a count begins to record the number of programming pulse cycles before success is finally achieved. If the data is not programmed after N_{MAX} attempts, it is a failed part. If data is verified, then it must be *overprogrammed* for a minimum of 3 times the cumulative programming time. The address counter is then incremented to the next address. The next data byte is sent, and programming continues using the same basic algorithm. See Figure 1.

Figure 1. Top-Level Programming Sequence



Parallel Programming Interface

The EPROM interface is a 17-wire connection. Review the part-specific pin diagrams in Figures 2 through 5 for part pin-out.

Pin Diagrams

Device pin-out diagrams for the 18-pin DIP/SOIC and 20-pin SSOP are shown in Figures 2 through 5 . There are two configurations for the 20-pin SSOP device—the corresponding parts are identified in the diagrams.

Figure 2. 18-Pin DIP/SOIC Pin Configuration, STANDARD Mode

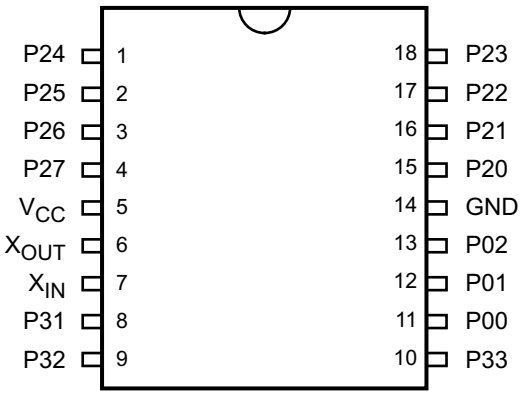


Figure 3. 18-Pin DIP/SOIC Pin Configuration, EPROM Mode

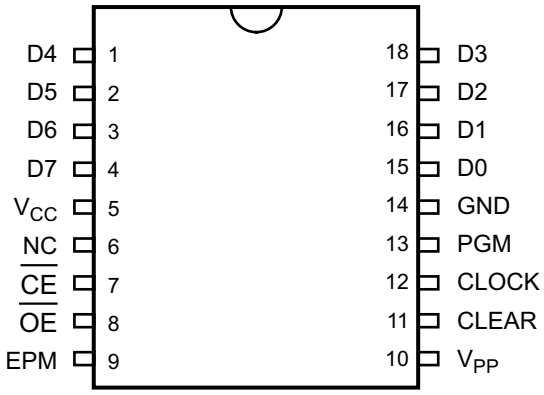


Figure 4. 20-Pin SSOP Pin Configuration, STANDARD Mode

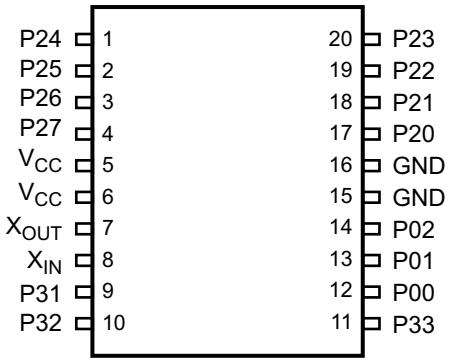
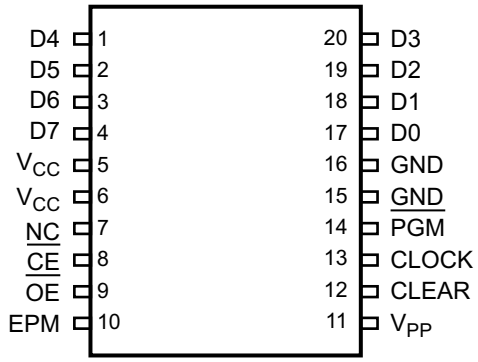


Figure 5. 20-Pin SSOP Pin Configuration, EPROM Mode



Tables 1 and 2 indicate the device's Port 2 input and output EPROM data.

Table 1. Output Parallel Byte

	Bit Number							
Port 2	7	6	5	4	3	2	1	0
Output EPROM data	7	6	5	4	3	2	1	0

Table 2. Input Parallel Byte

	Bit Number							
Port 2	7	6	5	4	3	2	1	0
Input EPROM data	7	6	5	4	3	2	1	0

OTP Memory Size

The device is offered in 4 memory configurations. Table 3 lists the available sizes of EPROM memory.

Table 3. EPROM Size

Devices	Memory Size	Last Address
Z86E02	0.5 KB	01FFh
Z86E04	1.0 KB	03FFh
Z86E08	2.0 KB	07FFh
Z86E09	4.0 KB	0FFFh

Device Operation

The device must first be unlocked before it can enter EPROM mode. Otherwise, the device remains in STANDARD mode. The device cannot be programmed in STANDARD mode. It can only be programmed in EPROM mode. The following sequence details the unlock procedure.

Unlock Sequence into EPROM Mode

The following unlock sequence is valid for all parts.

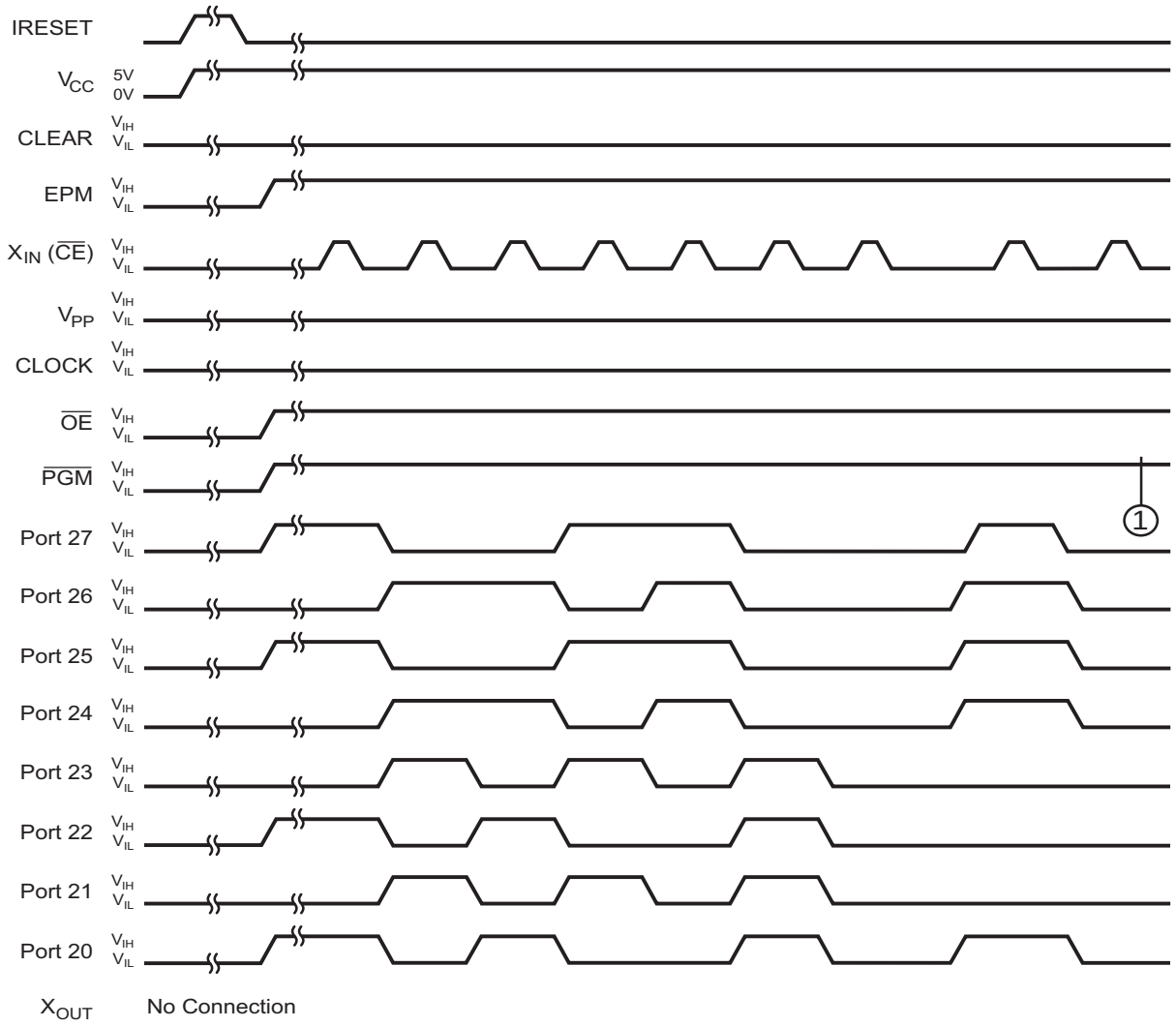
Note: Unlock clock cycles are the X_{IN} clock cycle entered by the programmer, not the internal Z8 SCLK cycles.

1. A POR must be completed before unlock operations begin. The X_{IN} pin must be in a V_{IL} state. Allow 50 ms minimum for the device to completely exit POR to allow the internal signal IRESET to go Low. See Table 5 for POR conditions.
2. Any time after POR, when the internal signal IRESET is Low. The unlock sequence can be sent. See Figure 6 and Table 4.
3. While the X_{IN} pin is in a V_{IL} state, force Port 2 pins with A5h.
4. Apply one clock pulse to X_{IN}. The clock pulses should be a minimum of 1 µsec in duration.
5. Force the Port 2 pins with 5Ah.
6. Apply one clock pulse to the X_{IN} pin.
7. Force the Port 2 pins with A5h.
8. Apply one clock pulse to X_{IN}.
9. Force the Port 2 pins with F0h.
10. Apply one clock pulse to X_{IN}.
11. Force the Port 2 pins with 0Fh.
12. Apply one clock pulse to X_{IN}.
13. Force the Port 2 pins with 00h.
14. Apply one clock pulse to X_{IN}.
15. Force the Port 2 pins with F1h.
16. Apply one clock pulse to X_{IN}.
17. Force the Port 2 pins with 00h.
18. Apply one clock pulse to X_{IN}.

19. The part is now in EPROM mode. The only way to exit EPROM mode is to perform a POR.

Note: All signals must be stable before the X_{IN} ($\overline{CE}$) pin is pulsed High and cannot change until X_{IN} (CE) pin is in a V_{IL} state. The signal should be stable for a minimum of 1 µsec.

Figure 6. Unlock Sequence



Note:
1. The device enters EPROM mode at this point when X_{IN} goes Low.

Table 4. Unlock Sequence Conditions

EPROM Signal	18-Pin DIP/SOIC	20-Pin SSOP	Forced State
D0–D3	Pins 15, 16, 17, 18	Pins 17, 18, 19, 20	See Figure 6
D4–D7	Pins 1, 2, 3, 4	Pins 1, 2, 3, 4	See Figure 6
GND	Pin 14	Pins 15, 16	GND
V_{CC}	Pin 5	Pins 5, 6	5V
$\overline{CE}$ (X_{IN})	Pin 7	Pin 8	See Figure 6
NC (X_{OUT})	Pin 6	Pin 7	No Connection
$\overline{OE}$	Pin 8	Pin 9	V_{IH}
EPM	Pin 9	Pin 10	V_{IH}
V_{PP}	Pin 10	Pin 11	V_{IL}
CLEAR	Pin 11	Pin 12	V_{IL}
CLOCK	Pin 12	Pin 13	V_{IL}
$\overline{PGM}$	Pin 13	Pin 14	V_{IH}

Table 5. Power-On Reset Pin Conditions

EPROM Signal	18-Pin DIP/SOIC	20-Pin SSOP	State
D0–D3	Pins 15, 16, 17, 18	Pins 17, 18, 19, 20	GND
D4–D7	Pins 1, 2, 3, 4	Pins 1, 2, 3, 4	GND
GND	Pin 14	Pins 15, 16	GND
V_{CC}	Pin 5	Pins 5, 6	Ramp to 5V
$\overline{CE}$ (X_{IN})	Pin 7	Pin 8	GND
NC (X_{OUT})	Pin 6	Pin 7	No Connection
$\overline{OE}$	Pin 8	Pin 9	GND
EPM	Pin 9	Pin 10	GND
V_{PP}	Pin 10	Pin 11	GND
CLEAR	Pin 11	Pin 12	GND
CLOCK	Pin 12	Pin 13	GND
$\overline{PGM}$	Pin 13	Pin 14	GND

EPROM Modes

The device offers two modes of operation. Table 6 lists the available mode options.

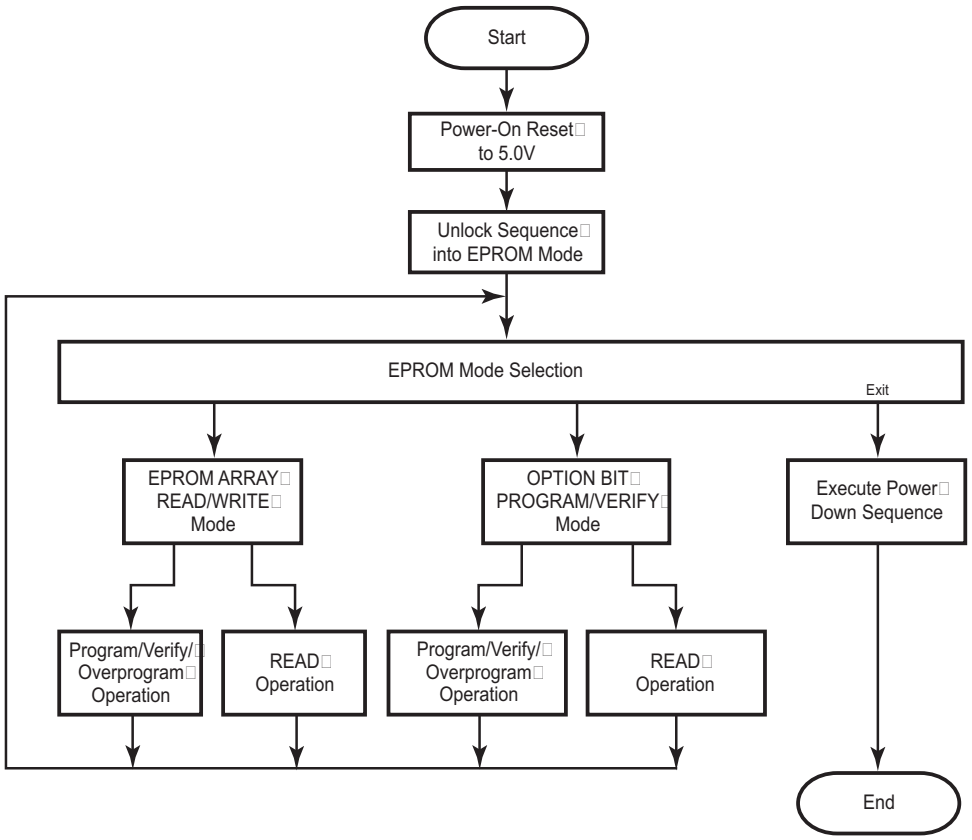
Table 6. Mode Selections

Value	Description
A	EPROM Array Read and Write modes
B	Option Bit Program and Verify modes

Top Level Operations

Figure 7 illustrates the operations available to the user after the device is unlocked and enters EPROM mode.

Figure 7. Top Level Operations Flow



EPROM Array Modes

EPROM ARRAY READ/WRITE Mode Entry

1. To enter EPROM ARRAY READ/WRITE mode, all pins must be set as per Table 7.
2. EPM is lowered to V_{IL}.
3. $\overline{OE}$ is lowered to V_{IL}.
4. The V_{PP} is raised to V_{IH}.
5. The CLEAR is pulsed High to V_{IH} and back down to V_{IL}.
6. The V_{PP} is lowered to V_{IL}.
7. After a delay of at least 1 µsec minimum, the V_{PP} is raised to V_{IH}.
8. $\overline{OE}$ is raised to V_{IH}.
9. EPM is raised to V_{IH}.
10. The device now operates in EPROM ARRAY READ/WRITE mode. See Figure 8.

Note: The delay between edges should be 1 µsec minimum unless specified in the timing specification in Table 14.

Figure 8. EPROM ARRAY READ/WRITE Mode Entry Functional Timing

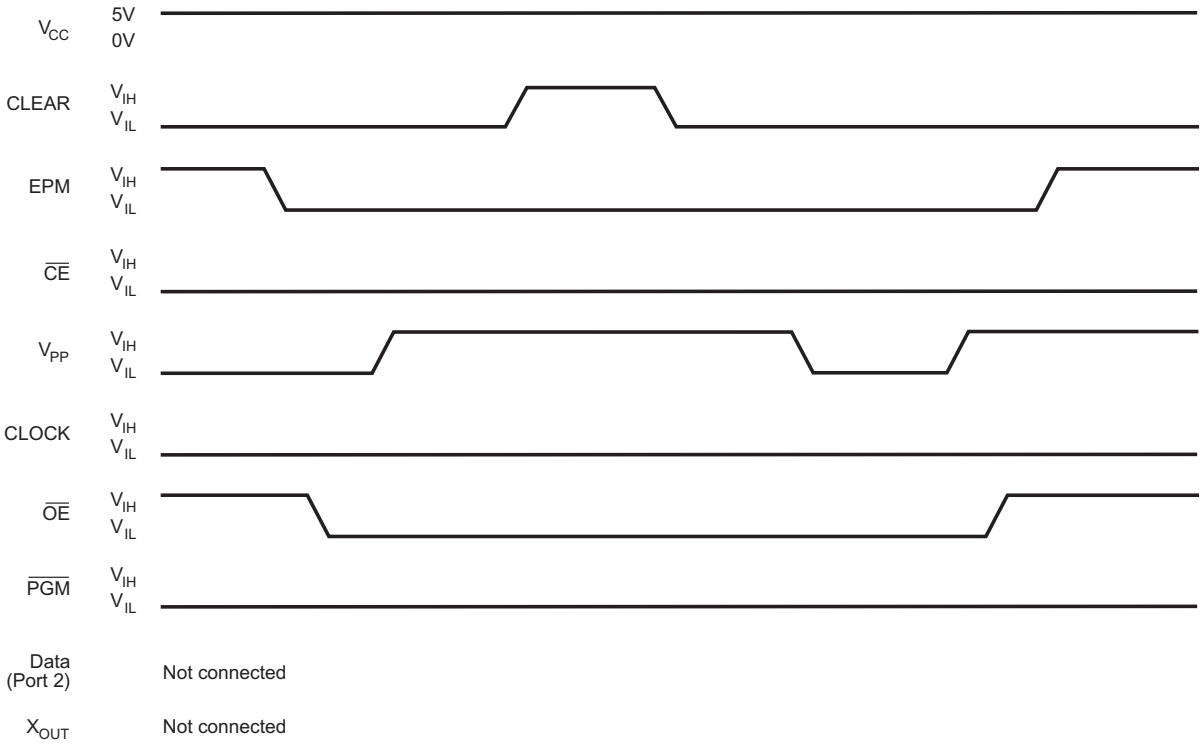


Table 7. EPROM ARRAY READ/WRITE Mode Entry Conditions

EPROM Signal	18-Pin DIP/SOIC	20-Pin SSOP	Forced State
D0–D3	Pins 15, 16, 17, 18	Pins 17, 18, 19, 20	NC
D4–D7	Pins 1, 2, 3, 4	Pins 1, 2, 3, 4	NC
GND	Pin 14	Pins 15, 16	GND
V_{CC}	Pin 5	Pins 5, 6	5V
$\overline{CE}$	Pin 7	Pin 8	V_{IL}
NC	Pin 6	Pin 7	No Connection
$\overline{OE}$	Pin 8	Pin 9	See Figure 8
EPM	Pin 9	Pin 10	See Figure 8
V_{PP}	Pin 10	Pin 11	See Figure 8

Table 7. EPROM ARRAY READ/WRITE Mode Entry Conditions (Continued)

EPROM Signal	18-Pin DIP/SOIC	20-Pin SSOP	Forced State
CLEAR	Pin 11	Pin 12	See Figure 8
CLOCK	Pin 12	Pin 13	V_{IL}
$\overline{PGM}$	Pin 13	Pin 14	V_{IH}

EPROM ARRAY READ Mode Operation

1. Perform Steps 1 through 6 of the EPROM ARRAY READ/WRITE mode entry (see the EPROM ARRAY READ/WRITE Mode Entry operation, previous page) before proceeding to Step 2.
2. Reset the address counter by pulsing the CLEAR pin. See Figure 9 and Table 8. Please refer to Table 14 for minimum and maximum widths of the CLOCK and CLEAR signals.
3. The address counter is incremented on the rising edge of the CLOCK signal.
4. After resetting the address counter using the CLEAR pin, the address counter points to address 0000h.
5. The READ operation is performed by lowering $\overline{OE}$ to V_{IL} and reading the data on Port2. Pins P20 to P27 represent the EPROM data D0 to D7, respectively. See Figure 9 and Table 8.
6. A V_{OH}-level READ on Port2 corresponds to a *1* state, while a V_{OL} level corresponds to a *0* level stored in the EPROM array.

Note: Please refer to Table 14 for the minimum and maximum width of OE during EPROM READ mode and data access time.

7. The next address is read by pulsing the clock pin High, then forcing $\overline{OE}$ to V_{IL} and bringing it back High after the data is read.
8. Repeat Step 7 until the final address is read.
9. Because the address is sequentially accessed, a previously-accessed address can only be read by resetting the address counter to 0000h and clocking the address counter to increment to the appropriate address.

Figure 9. EPROM ARRAY READ Mode Functional Timing

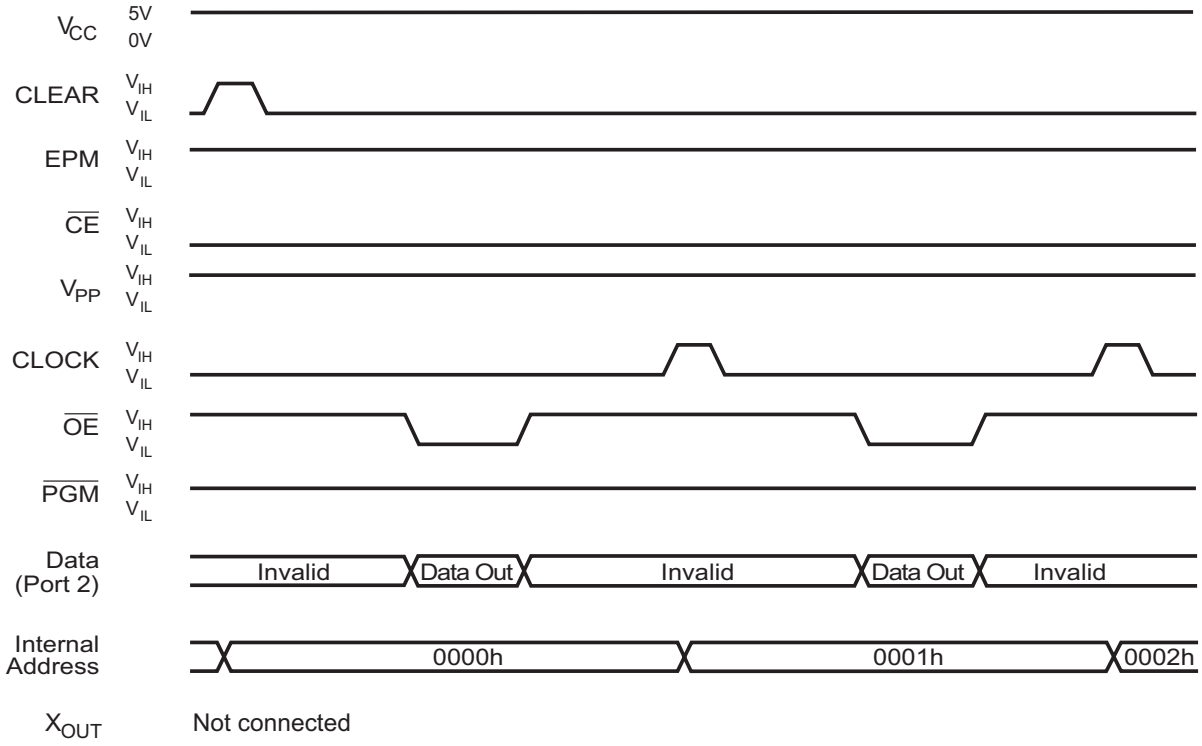


Table 8. EPROM ARRAY READ Mode Conditions

EPROM Signal	18-Pin DIP/SOIC	20-Pin SSOP	Forced State
D0–D3	Pins 15, 16, 17, 18	Pins 17, 18, 19, 20	See Figure 9
D4–D7	Pins 1, 2, 3, 4	Pins 1, 2, 3, 4	See Figure 9
GND	Pin 14	Pins 15, 16	GND
V_{CC}	Pin 5	Pins 5, 6	5V
$\overline{CE}$	Pin 7	Pin 8	V_{IL}
NC	Pin 6	Pin 7	No Connection
$\overline{OE}$	Pin 8	Pin 9	See Figure 9
EPM	Pin 9	Pin 10	V_{IH}
V_{PP}	Pin 10	Pin 11	V_{IH}

Table 8. EPROM ARRAY READ Mode Conditions (Continued)

CLEAR	Pin 11	Pin 12	See Figure 9
CLOCK	Pin 12	Pin 13	See Figure 9
$\overline{PGM}$	Pin 13	Pin 14	V_{IH}

EPROM ARRAY PROGRAM AND VERIFY Mode Operation

1. Perform the EPROM ARRAY READ/WRITE mode entry (see the EPROM ARRAY READ/WRITE Mode Entry operation on page 10) before proceeding to Step 2.
2. Reset the address counter by pulsing the CLEAR pin. See Figure 10 and Table 9. Please refer to Table 14 for minimum and maximum widths of the CLOCK signal.
3. The address counter is incremented on the rising edge of the CLOCK signal.
4. After resetting the address counter using the CLEAR pin, the address counter points to address 0000h.
5. The PROGRAM operation is performed by lowering $\overline{PGM}$ to V_{IL}. See Figure 10. Please refer to Table 14 for minimum and maximum widths of the PGM signal.
6. The PROGRAM operation is complete when $\overline{PGM}$ is raised back to V_{IH}.
7. The VERIFY operation is performed by lowering $\overline{OE}$ to V_{IL} and reading the data on Port2. Pins P20 to P27 represent the EPROM data D0 to D7, respectively.
8. A V_{OH}-level READ on Port2 corresponds to a *1* state, while a V_{OL} level corresponds to a *0* level stored in the EPROM array.
9. Please refer to Table 14 for the minimum and maximum width of $\overline{OE}$ during EPROM Read mode and data access time.
10. If the data read shows that the address location is not yet programmed, then repeat Steps 5 to 7 until the data read shows that the address location is programmed.
11. If the address location is not programmed after the 25th try, then the device is considered failed.
12. If the address location is programmed, then the address location is overprogrammed with three times the total accumulated program time.
13. The next address is accessed by pulsing the CLOCK High to V_{IH}, then Low to V_{IL}.

14. Repeat Steps 5 to 12 until the last address is read.
15. Because the address is sequentially accessed, a previously-accessed address can only be programmed or read by resetting the address counter to 0000h and clocking the address counter to increment to the appropriate address.

Figure 10. EPROM ARRAY PROGRAM AND VERIFY Functional Timing

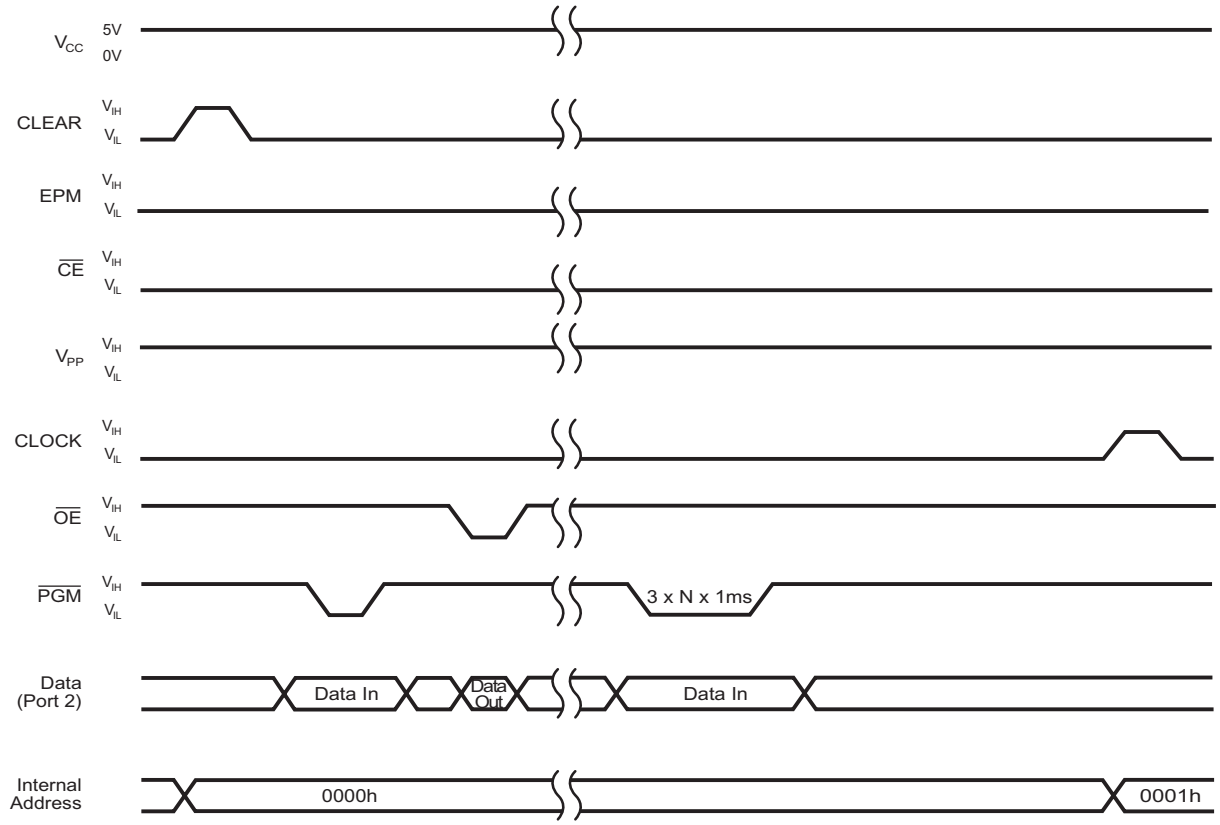


Table 9. EPROM ARRAY PROGRAM AND VERIFY Mode Conditions

EPROM Signal	18-Pin DIP/SOIC	20-Pin SSOP	Forced State
D0–D3	Pins 15, 16, 17, 18	Pins 17, 18, 19, 20	See Figure 10
D4–D7	Pins 1, 2, 3, 4	Pins 1, 2, 3, 4	See Figure 10
GND	Pin 14	Pins 15, 16	GND
V_{CC}	Pin 5	Pins 5, 6	5V
$\overline{CE}$	Pin 7	Pin 8	V_{IL}

Table 9. EPROM ARRAY PROGRAM AND VERIFY Mode Conditions (Continued)

NC	Pin 6	Pin 7	No Connection
$\overline{OE}$	Pin 8	Pin 9	See Figure 10
EPM	Pin 9	Pin 10	V_{IH}
V_{PP}	Pin 10	Pin 11	V_{IH}
CLEAR	Pin 11	Pin 12	See Figure 10
CLOCK	Pin 12	Pin 13	See Figure 10
$\overline{PGM}$	Pin 13	Pin 14	See Figure 10

Option Bit Modes

Table 10 lists the device's available option bits and their default states.

Table 10. Option Bit Values*

Bit	Option	Unprogrammed Default Value
D0	ROM Protect	Disabled
D1	Low-EMI Mode	Disabled
D2	Autolatches	Enabled
D3	Reserved	Must be 1
D4	Permanent WDT	Disabled
D5	Reserved	Must be 1
D6	RC Oscillator	Disabled
D7	32-kHz Oscillator	Disabled

Note: Option bits are 0 when programmed and 1 when unprogrammed.

OPTION BIT PROGRAM AND VERIFY Mode Entry

1. To enter OPTION BIT PROGRAM AND VERIFY mode, all pins must be set as per Table 11. The initial state for V_{PP} and CLEAR is V_{IL} while OE is at V_{IH}.
2. V_{PP} is raised to V_{IH}.
3. CLEAR is pulsed High to V_{IH}, then Low to V_{IL}. See Table 14 for specifications regarding the CLEAR signal.
4. V_{PP} is lowered to V_{IL}.
5. After a delay of at least 1 µs minimum, V_{PP} is raised to V_{IH}.

6. After a delay of at least 1 µs minimum from V_{PP} rising, $\overline{OE}$ is raised to V_{IH}.
7. The CLOCK is raised to V_{IH}.
8. $\overline{OE}$ is pulsed Low to V_{IL}, then High to V_{IH}.
9. The CLOCK is lowered to V_{IL}.
10. Repeat steps 7 to 9 six more times.
11. After a delay of at least 1 µs minimum, EPM is raised to V_{IH}.
12. The device is now in OPTION BIT READ/WRITE mode. See Figure 11.

Figure 11. OPTION BIT PROGRAM AND VERIFY Mode Entry Functional Timing

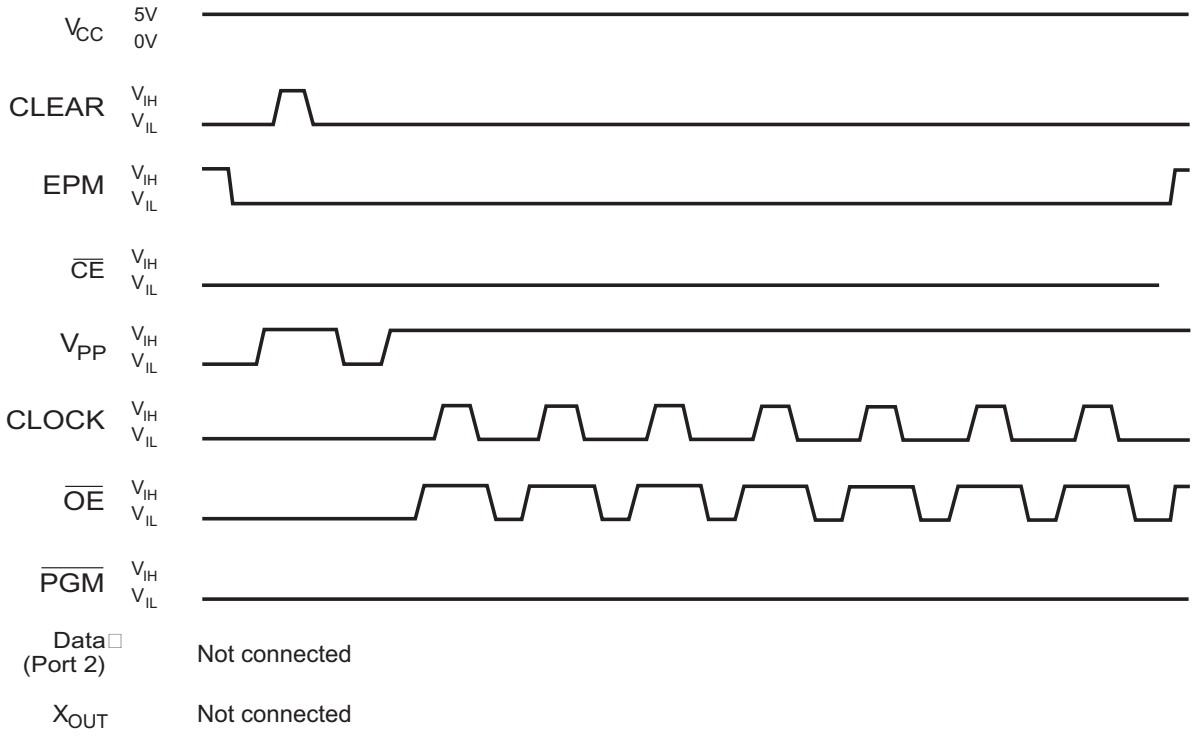


Table 11. OPTION BIT PROGRAM AND VERIFY Mode Entry Conditions

EPROM Signal	18-Pin DIP/SOIC	20-Pin SSOP	Forced State
D0–D3	Pins 15, 16, 17, 18	Pins 17, 18, 19, 20	NC
D4–D7	Pins 1, 2, 3, 4	Pins 1, 2, 3, 4	NC
GND	Pin 14	Pins 15, 16	GND

Table 11. OPTION BIT PROGRAM AND VERIFY Mode Entry Conditions (Continued)

V_{CC}	Pin 5	Pins 5, 6	5V
$\overline{CE}$	Pin 7	Pin 8	V_{IL}
NC	Pin 6	Pin 7	No Connection
$\overline{OE}$	Pin 8	Pin 9	See Figure 11
EPM	Pin 9	Pin 10	See Figure 11
V_{PP}	Pin 10	Pin 11	See Figure 11
CLEAR	Pin 11	Pin 12	See Figure 11
CLOCK	Pin 12	Pin 13	See Figure 11
$\overline{PGM}$	Pin 13	Pin 14	V_{IH}

OPTION BIT PROGRAM AND VERIFY Mode Operation

1. Perform the Option Bit READ/WRITE Mode Entry operation (see OPTION BIT PROGRAM AND VERIFY Mode Entry on page 16) before proceeding to Step 2.
2. The CLOCK is pulsed High to V_{IH}, then Low to V_{IL}. Please refer to Table 14 for minimum and maximum widths of the CLOCK signal. See Figure 12 and Table 12.
3. The 8 option bit values required in Table 10 are forced onto Port2. Option bits D0 to D7 corresponds to Port2 pins P20 to P27. Please refer to Table 14 for setup and hold times.
4. The PROGRAM operation is performed by lowering $\overline{PGM}$ to V_{IL}. Please refer to Table 14 for minimum and maximum widths of the PGM signal. See Figure 12 and Table 12.
5. The PROGRAM operation is complete when the $\overline{PGM}$ is raised back to V_{IH}.
6. The VERIFY operation is performed by lowering $\overline{OE}$ to V_{IL}, then reading the data on Port2. Pins P20 to P27 represent the Option Bit data D0 to D7, respectively.
7. A V_{OH}-level READ on Port2 corresponds to a *1* state (unprogrammed), while a V_{OL} level corresponds to a *0* level stored in the EPROM array.

Note: Please refer to Table 14 for the minimum and maximum width of OE during EPROM READ mode and data access time.

8. If the data read shows that the address location is not yet programmed, then repeat Steps 4 to 7 until the data read shows that the address location is programmed.
9. If the address location is not programmed after the 25th try, then the device is failed.
10. If the address location shows that it is programmed, then the address location is then overprogrammed with three times the total accumulated program time.

Figure 12. OPTION BIT PROGRAM AND VERIFY Functional Timing

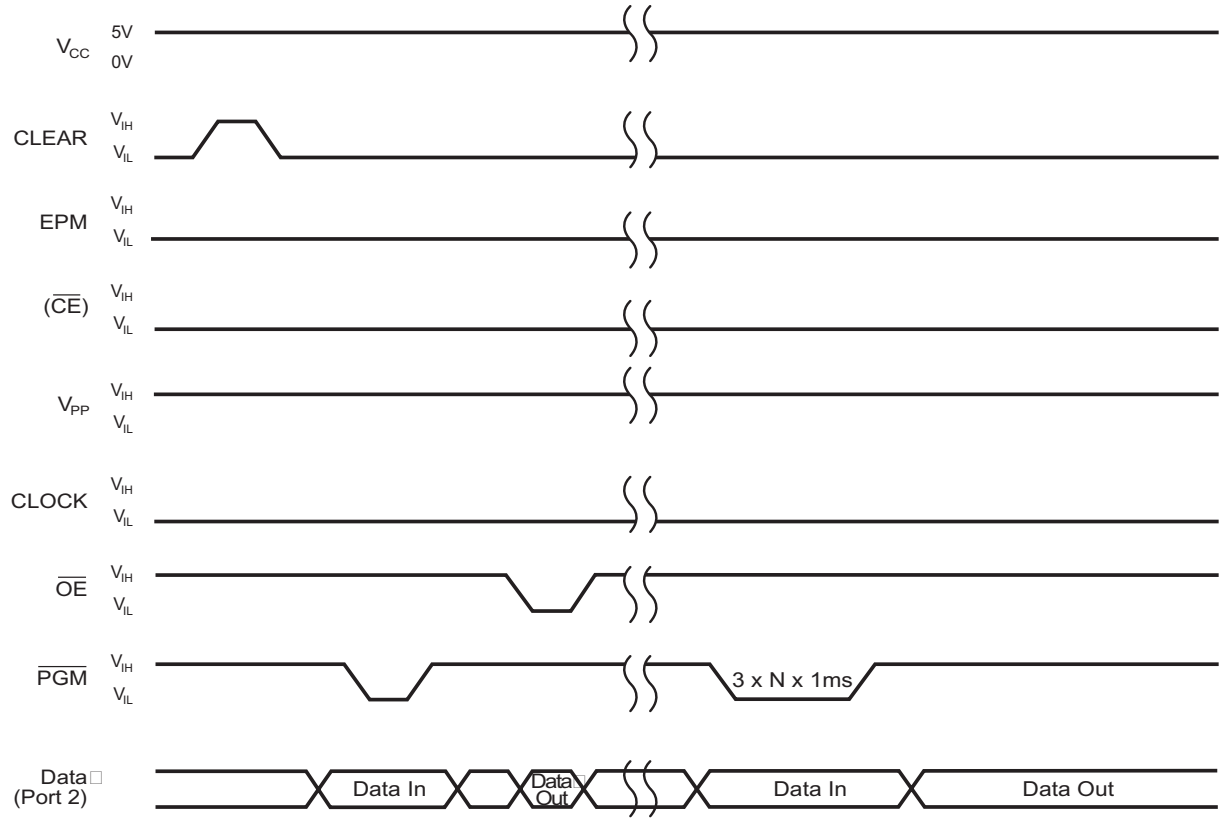


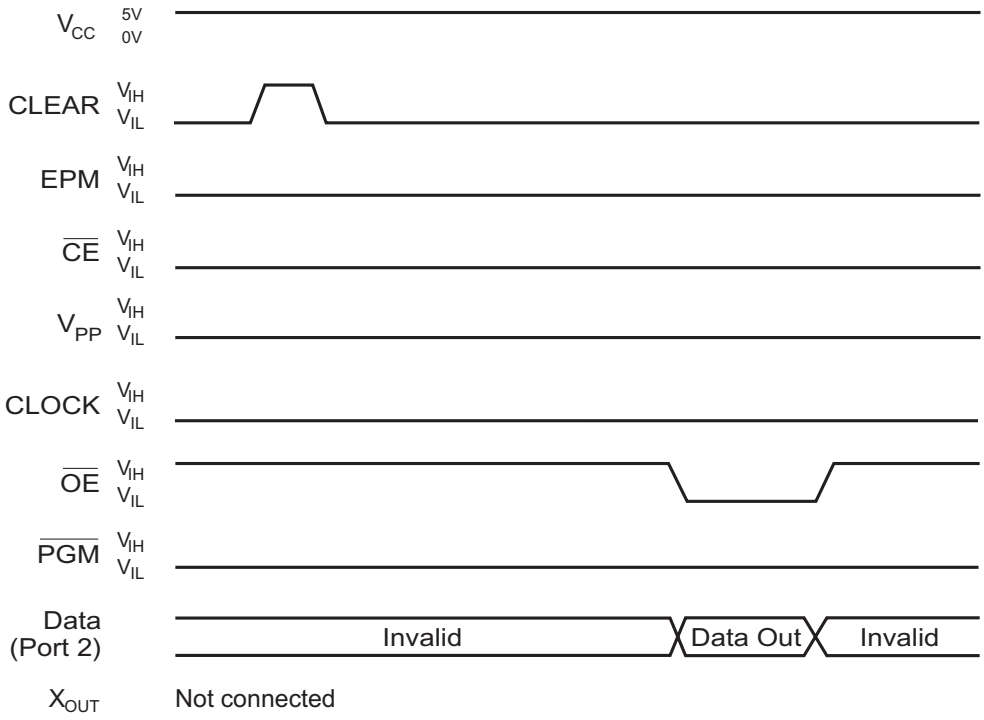
Table 12. OPTION BIT PROGRAM AND VERIFY Mode Conditions

EPROM Signal	18-Pin DIP/SOIC	20-Pin SSOP	Forced State
D0–D3	Pins 15, 16, 17, 18	Pins 17, 18, 19, 20	See Figure 12
D4–D7	Pins 1, 2, 3, 4	Pins 1, 2, 3, 4	See Figure 12
GND	Pin 14	Pins 15, 16	GND
V_{CC}	Pin 5	Pins 5, 6	5V
$\overline{CE}$	Pin 7	Pin 8	V_{IL}
NC	Pin 6	Pin 7	No Connection
$\overline{OE}$	Pin 8	Pin 9	See Figure 12
EPM	Pin 9	Pin 10	V_{IH}
V_{PP}	Pin 10	Pin 11	V_{IH}
CLEAR	Pin 11	Pin 12	See Figure 12
CLOCK	Pin 12	Pin 13	See Figure 12
$\overline{PGM}$	Pin 13	Pin 14	See Figure 12

OPTION BIT READ Mode Operation

1. Perform the Option Bit READ/WRITE Mode Entry operation (see OPTION BIT PROGRAM AND VERIFY Mode Entry on page 16) before proceeding to Step 2.
2. CLOCK is pulsed High to V_{IH}, then Low to V_{IL}. Please refer to Table 14 for the minimum and maximum width values of the CLOCK signal.
3. The 8 option bit values required in Table 10 are read from Port2. Option bits D0 to D7 correspond to Port2 pins P20 to P27. Please refer to Table 14 for setup and hold times.
4. The OPTION BIT READ operation is performed by lowering $\overline{OE}$ to V_{IL} and reading the data on Port2. Pins P20 to P27 represent the option bit data D0 to D7, respectively. See Figure 13.
5. A V_{OH}-level READ on Port2 corresponds to a *1* state, while a V_{OL}-level corresponds to a *0* level stored in the EPROM array.
6. Please refer to Table 14 for the minimum and maximum width of $\overline{OE}$ during EPROM READ mode and data access time.

Figure 13. OPTION BIT READ Mode Functional Timing



Power-Down Procedure

The following steps outline the power-down operation of the Z86E0x device.

1. Set up the I/O pins per Figure 14 and Table 13.
2. $\overline{CE}$ is raised to V_{IH}.
3. EPM is lowered to GND.
4. V_{PP} is lowered to GND.
5. V_{CC} is lowered from 5.0V to 2.0V.
6. $\overline{PGM}$ is lowered to GND.
7. $\overline{OE}$ is lowered to GND.
8. $\overline{CE}$ is lowered to GND.
9. V_{CC} is lowered to GND.

Figure 14. Power-Down Functional Timing

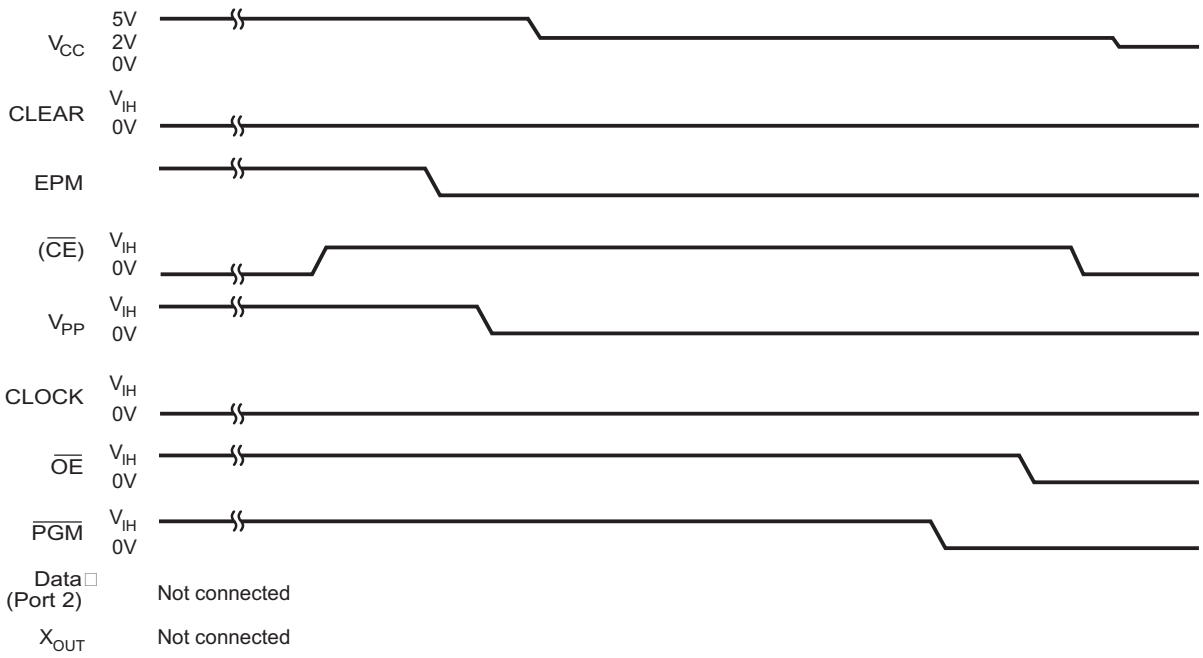


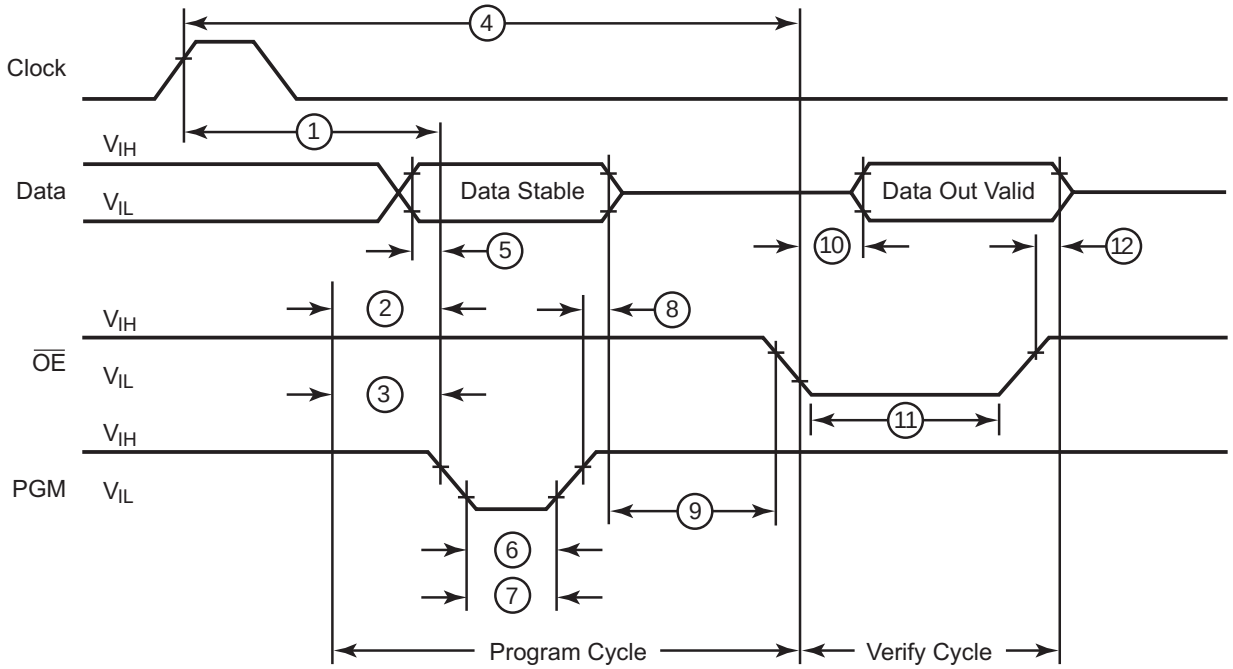
Table 13. Power-Down Conditions

EPROM Signal	18-Pin DIP/SOIC	20-Pin SSOP	Forced State
D0–D3	Pins 15, 16, 17, 18	Pins 17, 18, 19, 20	NC
D4–D7	Pins 1, 2, 3, 4	Pins 1, 2, 3, 4	NC
GND	Pin 14	Pins 15, 16	GND
V_{CC}	Pin 5	Pins 5, 6	See Figure 14
$\overline{CE}$	Pin 7	Pin 8	See Figure 14
NC	Pin 6	Pin 7	No Connection
$\overline{OE}$	Pin 8	Pin 9	See Figure 14
EPM	Pin 9	Pin 10	See Figure 14
V_{PP}	Pin 10	Pin 11	See Figure 14
CLEAR	Pin 11	Pin 12	V_{IL}
CLOCK	Pin 12	Pin 13	V_{IL}
$\overline{PGM}$	Pin 13	Pin 14	See Figure 14

EPROM I/O Timing

The following section details the programming and verification of the OTP. Input and output timing is illustrated in Figure 15. Timing specifications are provided in Table 14. Voltage specifications are provided in Table 15.

Figure 15. Z86E0x EPROM ARRAY and OPTION BIT PROGRAM AND VERIFY Waveform*



Note: *EPROM bits are 0 when programmed, and 1 when unprogrammed.

Table 14. Timing Specifications

Parameters	Name	Min	Max	Units
1	Address setup time	2		µs
2	Chip Enable setup time	2		µs
3	$\overline{\text{PGM}}$ setup time	2		µs
4	Address to $\overline{\text{OE}}$ setup time	2		µs
5	Data setup time	2		µs
6	Program pulse width	0.95		ms
7	Overprogram pulse width	2.85		ms

Table 14. Timing Specifications (Continued)

Parameters	Name	Min	Max	Units
8	Data hold time	2		µs
9	$\overline{OE}$ setup time	2		µs
10	Data access time	188		ns
11	$\overline{OE}$ width	250		ns
12	Data output float time		100	ns

Table 15. Voltage Specifications

		20ºC to 30ºC			
Symbol	**Description**	**Min**	**Max**	**Typical**	**Unit**
V_{PROG}	Programming supply voltage	4.75	5.25	5.0	V
I_{PROG}	Programming supply current		50		mA
V_{IH}	Input High Voltage	0.7 x V_{PROG}	V_{PROG}+0.3	2.6	V
V_{IL}	Input Low Voltage	GND–0.3	0.2 x V_{PROG}	1.6	V
V_{OH}	Output High Voltage	V_{PROG}–0.4		4.8	V
V_{OL}	Output Low Voltage		1.0	0.8	V

Figure 16 illustrates additional timing for the device. Table 16 provides the timing specifications identified in Figure 16.

Figure 16. Z86E0x Additional Timing Waveform

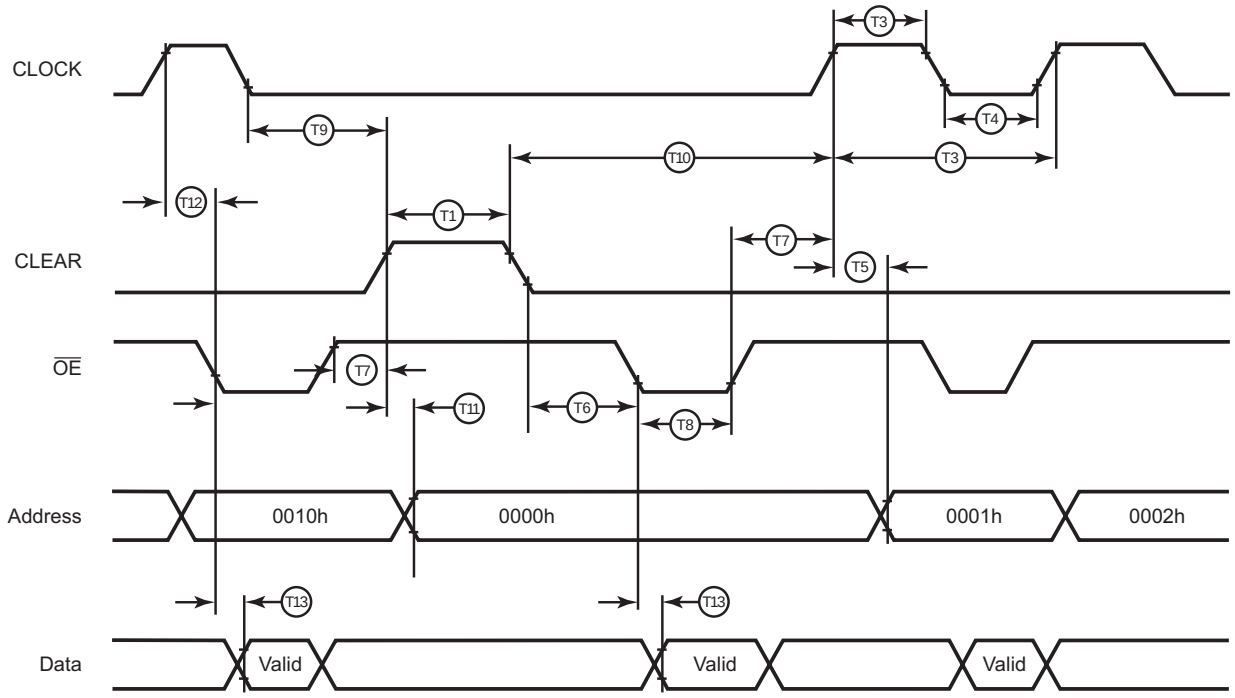


Table 16. Z86E0x Additional Timing Specifications

		Timing	
Parameter	**Name**	**Minimum**	**Maximum**
T1	CLEAR Width	1µs	
T2	Input CLOCK High	1µs	
T3	Input CLOCK Period	2µs	
T4	Input CLOCK Low	1µs	
T5	CLOCK to Address Counter Out Delay		15ns
T6	$\overline{OE}$ Setup Time	1µs	
T7	$\overline{OE}$ Hold Time	1µs	
T8	$\overline{OE}$ Width Low	250ns	
T9	CLOCK Falling to CLEAR Rising	2µs	
T10	CLEAR Falling to CLOCK Rising	2µs	

Table 16. Z86E0x Additional Timing Specifications (Continued)

		Timing	
Parameter	**Name**	**Minimum**	**Maximum**
T11	CLEAR to Address Counter Out Delay		15ns
T12	CLOCK Rising to $\overline{OE}$ Falling	1µs	
T13	Data Access Time	188ns	

Programming Flow

Figures 17 and 18 illustrate the flow of the EPROM ARRAY PROGRAM, VERIFY, and READ operations. Figures 19 and 20 illustrate the flow of the OPTION BIT PROGRAM, VERIFY, and READ operations.

Figure 17. EPROM ARRAY PROGRAM, VERIFY, and READ Algorithm

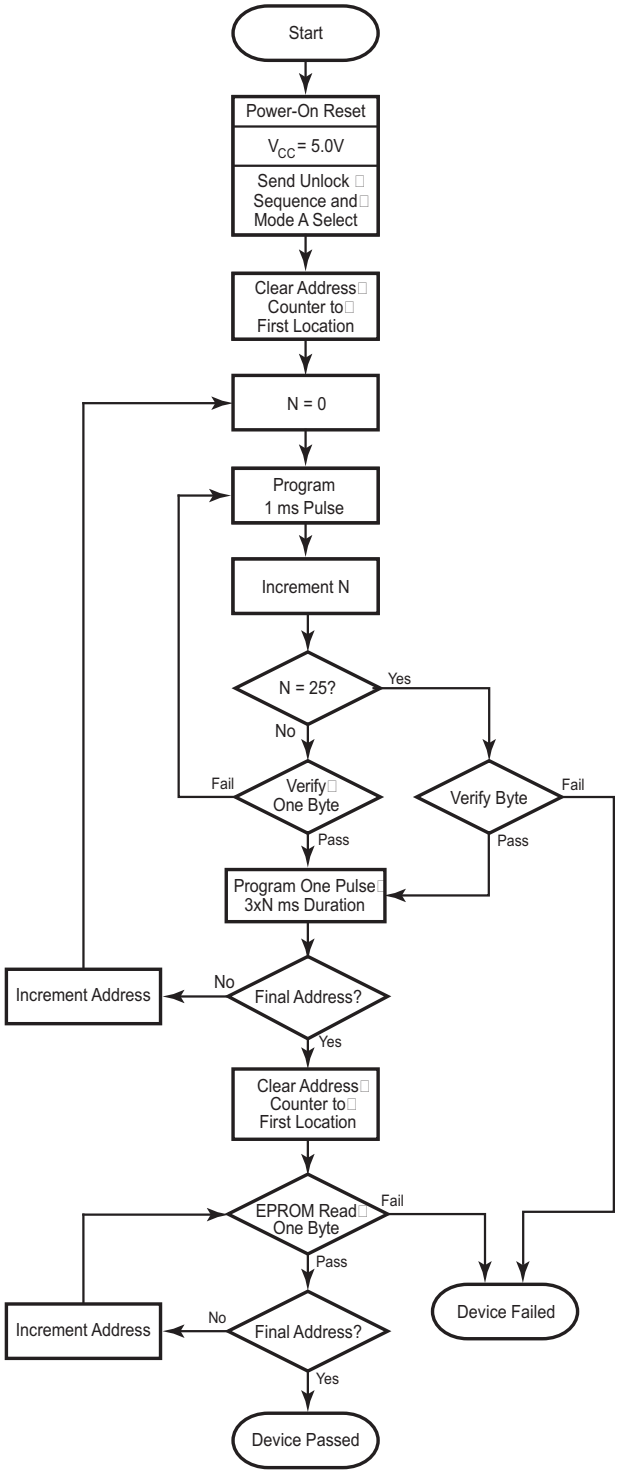


Figure 18. EPROM ARRAY READ Algorithm

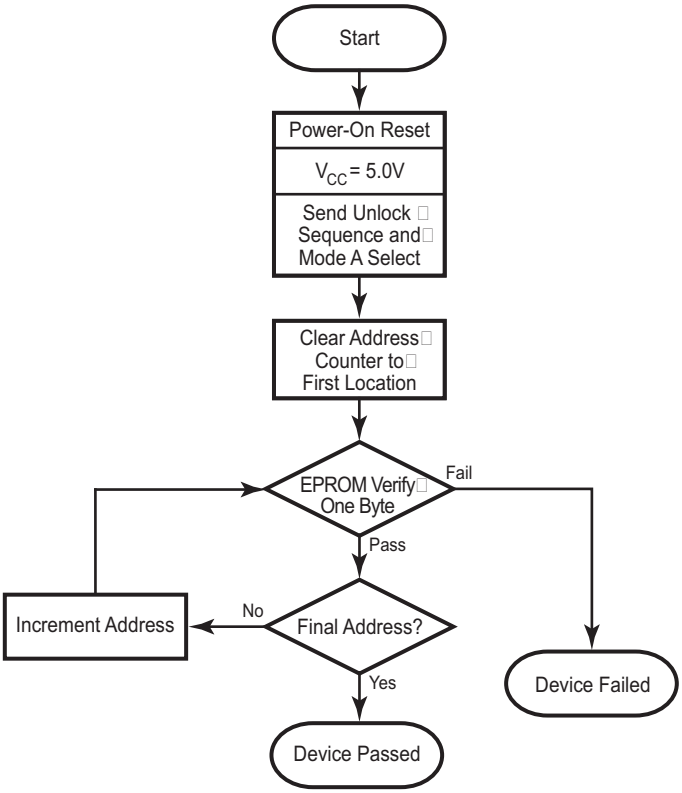
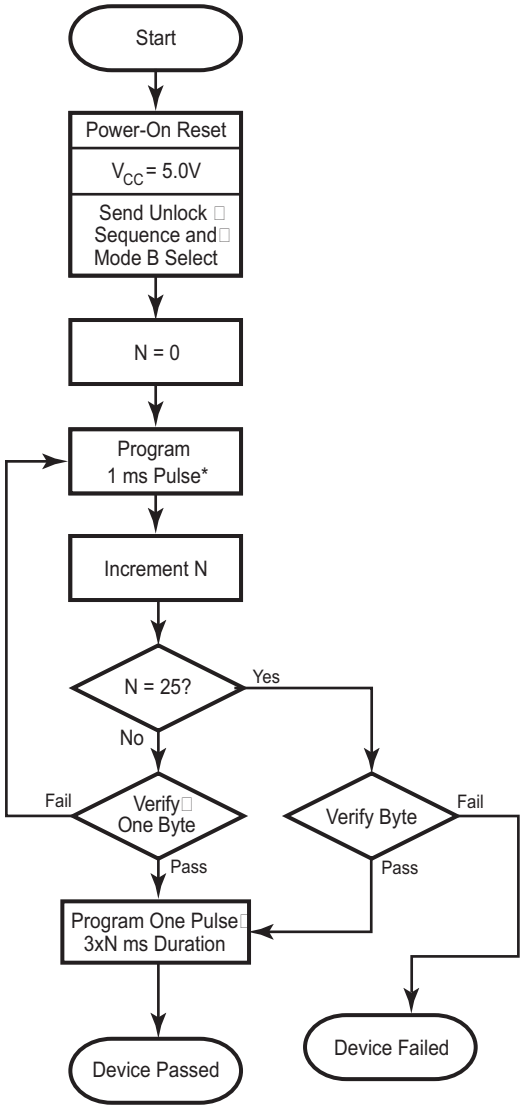
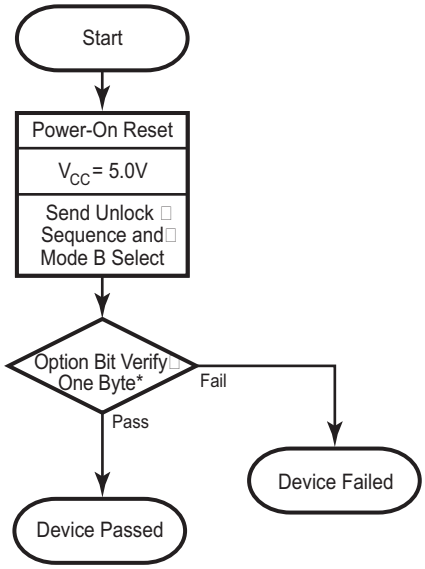


Figure 19. OPTION BIT PROGRAM, VERIFY, and READ Algorithm



Note: *It is assumed that the user has already selected the option bits prior to this step.

Figure 20. OPTION BIT READ Algorithm

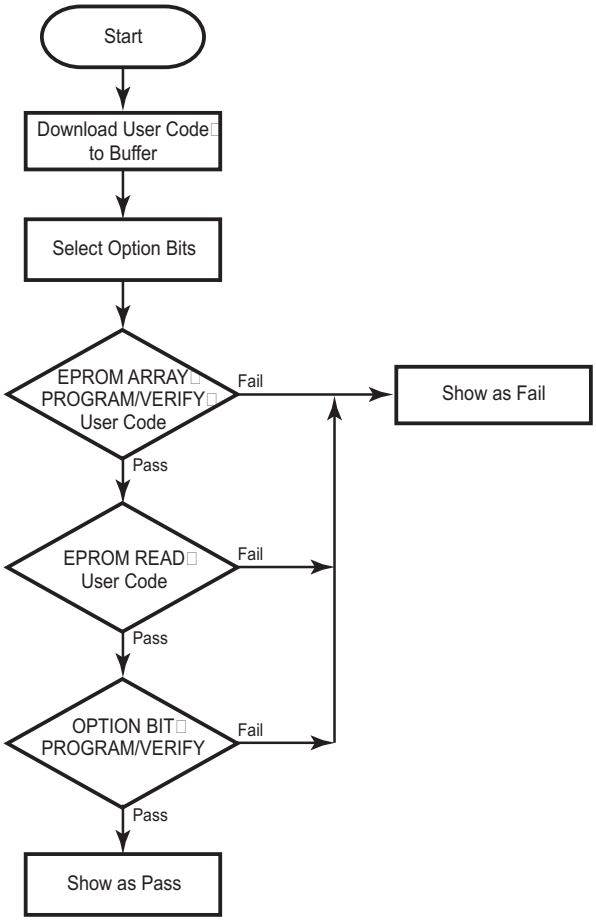


Note: *It is assumed that the user has already selected the option bits prior to this step.

Recommendations to Third-Party Programmers

ZiLOG recommends the top-level flow illustrated in Figure 21 for programming user code and option bits into OTP.

Figure 21. Third-Party Top-Level Algorithm



ZiLOG recommends that third-party programmers offer the following features for OTP operations.

- Blank check
- Examine OTP code
- Program/verify code and option bits
- Verify code
- Checksum of OTP

- Checksum of buffer/RAM
- Program option bits as a sole option
- Read option bits as a sole option

Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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Third Party Developer Feedback Form

The Z86E02/E04/E08/E09 SL1995 Programming Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Third Party Developer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

Third Party Developer Product Information

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
System Test/Customer Support
532 Race Street
San Jose, CA 95126
Phone: (408) 558-8500
Fax: (408) 558-8536
ZiLOG Customer Support

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.