CHAPTER 3 HARDWARE CIRCUITRY AND THEORY OF OPERATION

INTRODUCTION

The Smart Battery Charger Evaluation Board schematic diagram and other related drawings are provided in Appendix B. The discussion below uses the reference designations of the evaluation board schematic when describing circuit function.

The evaluation board is comprised of the following functional blocks, each of which are described in the following sections:

- The Z8-Controlled, Constant Current Power Supply
- RS-232C Serial Data Buffer
- Battery Discharge Circuit
- Linear Ramp Generator
- Regulated V_{CC} Power Supply

Z8-CONTROLLED, CONSTANT CURRENT POWER SUPPLY

Charge Current Control Loop

The charger is configured for constant current output. The Z8 senses battery voltage through the attenuation network comprised of Rs1 and Rs2. (Refer to the evaluation board schematic diagram.) The evaluation board permits a wide range of battery voltages (2.4V to 12VDC) simply by selecting the scaling resistors from a look-up table. R20 and C11 are a low-pass filter for the Z8's battery voltage A/D input at pin 8, and diode D4 clamps the voltage at this pin to V_{CC}.

NOTE: The evaluation board accommodates battery voltages of 9.6V maximum, due to voltage limitations of the included wall transformer; however, 12V is possible with other power supplies.

The power input for the charging circuit is an AC wall transformer; however, a DC input can also be used. The DC supply to the top of Q1 must be at least two to three volts higher than the battery pack's peak voltage. This voltage can be as high as two volts per cell during charging. The supply voltage

must also be high enough to trigger missing battery detection. A missing battery causes the P31 voltage ($V_{BAT'}$) to be: $V_{BAT'} = V_{IN}$ x Rs1 / (Rs1 + Rs2 + R_{PU}) >= 4V.

This voltage must be greater than 4V, but Rpu should be as large as possible to prevent charging the battery through it. Values are given for Rpu in the cell count look-up table that are appropriate for the supplied transformer. A missing battery is detected when the Z8's periodic battery voltage A/D routine senses an out-of-range high battery voltage.

When a battery is connected to the charger and the Z8 enables charging by setting output P20, the constant current control circuit works in the following manner:

- The PNP pass transistor Q1 is switched on/off at a frequency loosely determined by:
  - Input voltage
  - Battery voltage
  - Choke L1 value
  - Component values around the comparator U3 pins 1,2,3

  When Q1 is on, current through L1 increases linearly with a slope, dI/dt = VL / L where VL is approximately equal to V_{IN}- V_{BAT}.
- The charging current through the battery develops a voltage drop across resistor R25, which is sensed by the constant current feedback control circuit. A 0.1V DC drop across sense resistor R25 would correspond to a 0.1V / 0.1 Ohm = 1.0 A DC current.
- A low-pass filter (R27 and C15) attenuates high-frequency switching noise at the comparator's inverting input, pin 2.
- A voltage divider comprised of R26 and Rch sets the DC charging current applied to the battery. Resistors R26 and Rch develop a comparator threshold voltage.
- When the increasing charge current causes the R25 voltage drop to exceed the comparator threshold voltage, the comparator output switches low, which turns off Q3 and subsequently Q1. This causes the current through L1 to now linearly decrease, with a slope, dI / dt = VL / L, where VL is approximately equal to V_{BAT}.
- When the voltage drop across sense resistor R25 drops below the comparator threshold, the comparator output switches high, which turns on both Q3 and Q1, completing the current control cycle.

Notice that the comparator threshold value is modified by the hysteresis introduced by R24, which causes the R24 value to alternately appear in parallel with either R26 or Rch, depending on whether the comparator output is high or low. When the comparator open collector output is off, R24 effectively appears across R26, and the maximum threshold value is:

V_{CC}(Rch / (RX+Rch) where RX = R24 x R26 / (R24+R26)

This maximum threshold value yields a maximum threshold voltage of 0.11V for the values shown. This voltage scales to an I Lmax value of 1.1 A.

When the comparator output is low, the minimum threshold value is:

V_{CC} (RY / (RY+R26)) where RY = R24 x Rch / (R24+Rch)

Since R24 is 100X larger than Rch, its effect on the voltage divider is negligible. So, RY essentially equals Rch, and the equation for the minimum threshold value simplifies to V_{CC}(Rch / (Rch+R26). The minimum threshold voltage for the values shown is 0.08V. This scales to an ILmin value of 0.8A.

The average charging current is approximately equal to 0.5 (ILmin + ILmax). Unequal upslope and downslope values, and Q1 turn-off delay time affect the actual average charging current. The percentage of AC ripple in the charging current is a function of the R24 value. A larger R24 value decreases the AC component, but increases switching frequency by moving the comparator thresholds closer together. Hysteresis around the comparator causes Q1's on/off switching to occur at predictable limits. The result is a DC current component determined primarily by the values of R26, Rch, sense resistor R25, and a sawtooth AC component due to the hysteresis caused by R24. A voltage analogue of the battery charging current is easily observed across R25 when the charger is operating. The values shown produce a voltage equal to 0.1V per Ampere. For a thorough discussion of hysteresis in inverting voltage comparators, see Ref 1.

Design Considerations

The constant current control circuitry is easily tailored to different requirements, but there are several considerations to keep in mind. First, transistor Q1 is selected for both it's current capability and high-speed characteristics. This is a 5A 25V device with an fT of 65 MHz. For compact applications, this device is also available in a surface-mount D Pack. To limit Q1's power dissipation, it is desirable to limit the switching frequency to less than 25 kHz. The range of 15- to 20-kHz is ideal. For most applications, the heatsink on Q1 will not be needed.

Worst-case (maximum) switching frequency occurs with a low-voltage battery pack at a high-input voltage condition. Recall that the current upslope and downslope are VL / L and the slopes control switching frequency. (Steep slopes mean the current is ramping between limits faster, resulting in higher frequency.) Since the power dissipated by Q1 is proportional to the switching frequency, care should be taken when using low-cell-count battery packs. The input supply should be sized down to keep VL reasonably small but still high enough to keep the circuit active. For good performance, ensure that the input-transformer turns ratio is sized to provide adequate inductor voltage under all conditions of AC line and battery voltages. The worst-case condition is maximum battery voltage but low input voltage (or a large input voltage ripple component at C1). With the maximum battery voltage at low AC line voltage, there should be at least 4V across the inductor, even at the low point in ripple at capacitor C1. Some ripple at C1 is acceptable, but an unfiltered input does not work, as VL periodically goes to zero.

When the input voltage is sized to the battery voltage, the operating frequency can be adjusted by varying the choke L1 value. This choke can be one of several types. For lowest cost, a ferrite bobbin style choke is a good choice. Another option is a powdered-iron toroidal choke. Several manufac-

turers offer engineering sample kits at reasonable cost that provide a convenient method for quickly trying different L values.

Another alternative is the design-to-spec route. Micrometals, Inc. makes the powdered-iron cores used by many inductor manufacturers. Their catalog has the necessary design data for DC chokes. They can also provide excellent design software which automates the design process, yielding different options for the parameters you specify.

For applications which must accommodate a wide range of battery voltages and/or input voltages, it may be better to consider a PWM current control method, using an industry standard current mode control device. The UC384x series of devices are made by several manufacturers, and offer predictable performance at somewhat higher cost than the scheme used in this evaluation board.

RS-232C SERIAL DATA BUFFER

The serial data buffer is a simple level-shifting scheme. The buffer transistor Q5 provides output switching from Z8 ground to the V_{IN} supply rail. Components R33, C18, and D8 provide a virtual ground for the connected computer. R34, C17, and D7 provide ESD protection, and D7 also clamps the output signal so the serial data has a +6V to -6V swing about the RS-232C signal ground at connector pin 5.

NOTE: Because the virtual ground is typically connected to earth ground at the PC, the serial port generally does not work if an oscilloscope is connected to the charger.

This serial hardware is generally not included on the production design as the in-line manufacturing test can use the CMOS-level data available directly at the Z8 output. The serial data output is a software debug feature that provides a convenient method for studying charger performance when used in conjunction with the PC monitor software provided with this evaluation board.

BATTERY DISCHARGE CIRCUITRY

The conditioning discharge circuit is included to allow chargers designed for NiCd batteries to remove any remaining charge from the battery before commencing the charge cycle. Since the NiCd chemistry is so prone to the memory effect, this discharge cycle can extend the life of the battery significantly. Since discharging can take several hours if the battery was not near empty, the conditioning cycle is often used as a user-selectable input. This allows the end user to get a battery back quickly or to start a discharge cycle if leaving the battery over night.

The discharge current can be changed with a single resistor value change. Discharge current is controlled by resistor R30. The evaluation board will accommodate discharge rates over 1A with appropriate selection of R30. Keep in mind that R30 dissipation is approximately V_{BAT}**2 / R30. Q4

accommodates significant power dissipation as well, but should be placed on a heatsink if you greatly increase the discharge current.

Discharging the battery too quickly seriously shorten its life. Typically, discharge should not be faster than a C/10 rate. Also be aware that it is detrimental to deeply discharge most batteries. Most NiCd and NiMH batteries should not be discharged below 1V per cell. The Z8 monitors the battery voltage during discharge and terminates at a software-configurable voltage.

Battery discharge is initiated by either a momentary press of push-button SW1 or can be jumped to always discharge before charging or disabled completely. If the discharger will not be used, it can be removed completely (to save money).

LINEAR RAMP GENERATOR

The Analog-to-Digital Conversion (ADC) is done by timing a linear ramp from 0V to the point at which it crosses the unknown voltage. The ramp generator consists of PNP transistor Q2, resistors R7 though R9x and capacitor C10. It works like this, the ramp is initialized to zero by driving P23 low. This causes the capacitor to charge up to the point at which Q2 is cut off. At that point, P23 is tri-stated and the capacitor starts to discharge.

Since the voltage across the capacitor cannot change instantly, this causes the base of Q2 to attempt to rise, further cutting off the transistor. Since P23 and P33 are tri-state inputs, negligible amounts of current flow into the Z8. Assuming the gain of the transistor is reasonably large, the base current is also negligible. Thus, the capacitor can only discharge through the series combination of R7, R8 and R9', where R9' represents the effective resistance of R9 through R9e. As the capacitor discharges, the transistor starts to activate. The current flowing through R7 and R8 causes the capacitor to push the base upwards, again shutting down the transistor. In this way, the voltage output ramps from approximately zero volts to approximately V_{CC} in a nearly-linear fashion. The linearity of the ramp is assured as long as the transistor remains in the linear region. Therefore, the transistor must be a highly-linear amplifier. Ramp time is given by the RC time constant of C10 with R7, R8, and R9'.

The exact ramp time must be known in order for the counter value to accurately reflect the measured ADC voltage. In order to tune this in, R9 has been broken into several parts. There are three options:

1. Use a set of precise components including all the resistors and the capacitor.

   All the components in the system must have a minimum of error because the error becomes directly reflected in the accuracy of the measured voltage. The drawback is that tight-tolerance components, particularly capacitors, are very expensive. However, only R9 is used; R9a through R9e are not used.

2. Use R9D and R9E to provide an adjustment capability.

   A potentiometer provides the trim adjustment. The advantage is the ability to use large resistance values and smaller capacitors. This method saves the cost of the high-value, low-tolerance capacitor but trades off the cost of the potentiometer. This cost is offset somewhat by using a fixed

resistor with a smaller single-turn pot instead of a multiple-turn pot that covers the full resistance of R9'. The major drawbacks of using the potentiometer are the tendency for its settings to drift, and the time required for a human to trim the board into tolerance.

3. Use R9, R9A, R9B and R9C as a trimming tree to tune out the component error.

   This allows the system to be calibrated once, at the factory, in such a way that there will be very little drift over time, and very little additional cost on the Bill of Materials. The drawback to this approach is the time required for a human to tune every board on the assembly line or the cost of having an automated system do the trim. Another problem with this approach is that the resistance value for R9C must be about forty times the maximum requirement for R9'. The use of resistors above 10 Mohms tends to cause problems with humidity and board cleanliness. To keep the value of R9C down, the value desired for R9' needs to be small which requires a large value for C10.

   The demo board uses this method by default, though the other two are available to the user as well. There is a manufacturing calibration mode incorporated into the demo software that aids in the use of methods two and three. The software, when in calibrate mode, lights the yellow LEDs to tell the user which resistor to cut or how far the pot needs to be turned. This greatly simplifies the trimming process, compared to using an oscilloscope, and allows errors not caused by the ramp time (such as interrupt latency, and V_{CC} variations) to be calibrated out.

REGULATED V_{CC} POWER SUPPLY

The V_{CC} for the microprocessor is regulated down from V_{IN} by an LM317 regulator, U2. This three terminal adjustable regulator is a good compromise for this circuit because it does a good job of rejecting power supply ripple. (V_{IN} is quite noisy when the charge current is on.) It is relatively cheap and small in the TO92 package used here but can also be purchased in a TO220 if higher current or power is required and in a surface mount package for extremely small applications. The LM317 is also fully protected against thermal and current overloads.

The LM317, being an adjustable regulator, lends itself nicely to using trimming resistors.

In the evaluation board, R3 and R4x are a trimming tree that works just like the one discussed for the ramp generator. In this case, it is simply a matter of using a DMM to measure the V_{CC} while trimming the resistors to obtain an accurate supply voltage. Again, this can be bypassed by using just R3 and R4 but that provides only a 5% tolerance on V_{CC} using 1% resistors. Resistors R1 and R2 are provided to reduce the power dissipation in the LM317. They are sized appropriately for V_{IN} values between 12 and 24 VDC. If a smaller supply voltage is used, they need to be resized or eliminated. Larger supplies are not supported on this demo board without significant component changes.

In production, components C5, U2, and R4 through R4C can be left out, and R3 replaced with a zener diode from U2 pin 2 to pin 1, pin 2 shorted to pin 3 and pin 1 shorted to ground. A 5.1V, 0.5W zener diode will provide an adequate V_{CC} regulator but with far less input-noise rejection than the LM317 provides and only 5% voltage accuracy. Care should be taken to size R1 and R2 appropriately for the V_{IN} supply and Iz (zener on current minimum) in order to supply 100 mA to the Z8 maximum. Power dissipation in these resistors must be considered.

A third option is to replace the LM317 with a fixed 5V regulator such as the 78L05, leave R3 out and short R4. This will provide a compromise between the solutions above in terms of price, noise immunity and V_{CC} accuracy.

CHARGING CIRCUITRY DESIGN MODIFICATIONS

The charging circuitry on the evaluation board is extremely adaptable. Depending on performance requirements, system complexity can be reduced. Obvious changes include deletion of software debug features, such as the RS-232C serial data buffer, and deletion of the battery discharge circuit.

Appendix B shows several production charger designs based on the evaluation board hardware and software. This charger design can accommodate a wide range of battery voltages (4.8V to 9.6V with the provided wall transformer, and up to 12V with a different wall transformer). Other schematic diagrams show other simplified chargers based on this design. All run with the supplied code, but provide benefits such as cost reduction and decreased size, often at the price of units with reduced features.

The last of the diagrams shows one method for adapting this design to a multiple pocket charger system that duplicates almost nothing by simply switching a relay to connect one pack only if the other pack is not present. This design requires some software modifications to handle the sharing of circuitry.

REFERENCES

1. “A Quad of Independently Functioning Comparators,” *Linear Applications Handbook*, National Semiconductor Corporation, AN-74,1991. (See the article's Figure 7 and its accompanying text.)

Catalog 4, Power Conversion & Line Filter Applications, 1992, Micrometals, Inc., Anaheim, CA, (800) 356-5977. See sections on DC inductor design.

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