APPLICATION NOTE



# THE Z86C08 CONTROLS A SCROLLING LED MESSAGE DISPLAY

DISPLAY TEXT AND GRAPHICS WHILE SCROLLING THE LED MESSAGE WITH A MINIMUM OF HARDWARE. THE CHARACTERS ARE DISPLAYED USING A TIME-DIVISION MULTIPLEX TECHNIQUE WITH MORE THAN SIX CHARACTERS EASILY ADDED BY SOFTWARE.

#### INTRODUCTION

Designed around the Zilog Z86C08, 18-pin microcontroller, this LED display is capable of displaying text as well as graphics, with hardware being kept to a minimum. The present design is configured to display u to six characters, but additional characters are easily added with minimal software changes.

The display uses a TDM (Time-Division Multiplexed) technique to display the characters. That is, each character

segment is turned on for a few hundred microseconds at a time, then is "refreshed" every 18 ms.

For demonstration purposes, the software routine displays the time in hours, minutes, and seconds. Once every sixty seconds, a "secret message" scrolls across the display. Then, after the message is displayed, the program reverts back to displaying the time.

#### THE HARDWARE

The Z86C08 (Figure 1) uses Port 2 for the row data and clocks the column data out of Port 0. PNP transistors are used to drive the rows, since the Z86C08 cannot source the required current directly. The characters are displayed

in a 5x7 format, so only seven lines are needed out of Port 2. A logic Low turns on the transistors, while a logic High turns them off.

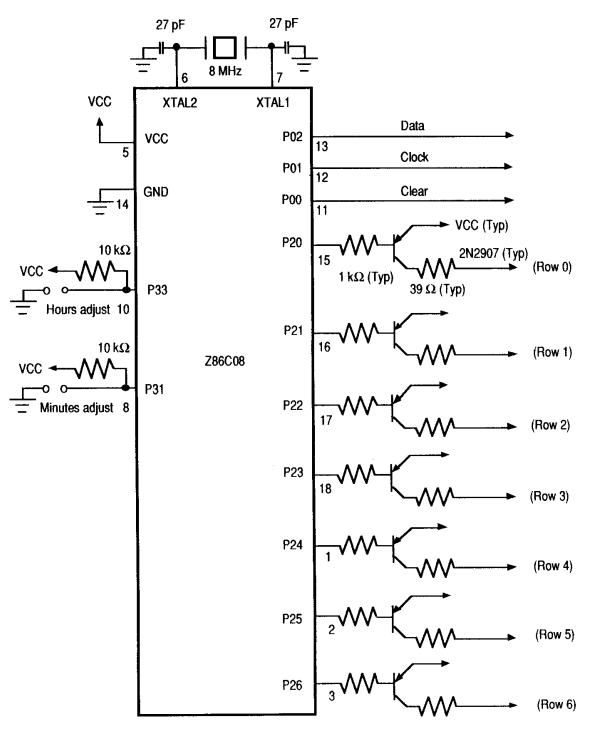


Figure 1. Z86C08 Circuit Functions

The columns are driven by six 74HCT164 shift registers (Figure 2). The 74HCT164s do not have the necessary sink capability to drive the LEDs, so the outputs of the shift registers drive six 75492 high-current buffers. These are capable of sinking 250 mA per pin continuously, with instantaneous current per column approaching 1.5 A.

Each 74HCT164 drives six columns; five character segments, plus one space. The last Q output from the shift register is then fed to the DATA input of the next shift register, while all CLEAR and CLOCK lines are wired in parallel.

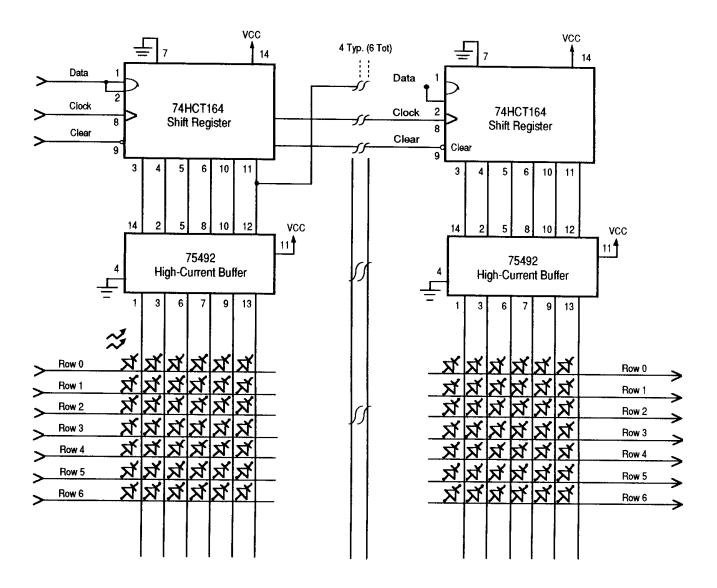


Figure 2. LED Circuitry

### THE HARDWARE (Continued)

To scan the display, a logic 1 is output at P0-2. Next, P0-1 is taken High, then immediately taken Low, along with P0-2. This clocks a logic 1 into the first shift register (column 1). Next a character segment is output at P2. The transistors that are turned on will source current for the LEDs with the column providing a sink path. The columns are left on for about 500  $\mu$ s and then turned off. Now, the column data

is shifted one and a new character segment is output. After the last column has been scanned, the display is "refreshed" starting at the first column again.

To set the time, two push-button switches are connected to Port 3 to adjust the hours and minutes.

#### THE SOFTWARE

The initialization part of the program configures the ports, timers, interrupts, etc. The size of the display buffer (FIFO) is determined by the number of columns in the display. The bottom of the display buffer starts at 20H. The upper limit of the display buffer can extend to 70H. This translates into a sixteen-character display. There is no need to have a display buffer larger than the display itself, since only that many characters can be viewed at a time. A power-up, the display is configured for showing the time.

The flowchart for the display appears in Figures 3a and 3b. To keep time, the internal clock was divided down by T0 to provide an interrupt every 5 ms. The interrupt routine increments a counter, and when 200 counts is reached, the seconds register is incremented by one. Also, when ten seconds is reached, tens-of-seconds is incremented. This counter continues to increment minutes, tens-ofminutes, hours, and tens-of-hours. Upon power-up, the display shows 12:00. When it is around 9:00, the leading hours digit is blanked. Time is adjusted by two push-button switches. When pressed, one increments the minutes register every second, while the other increments the hours register every second. The time data is stored in locations 09H-0EH.

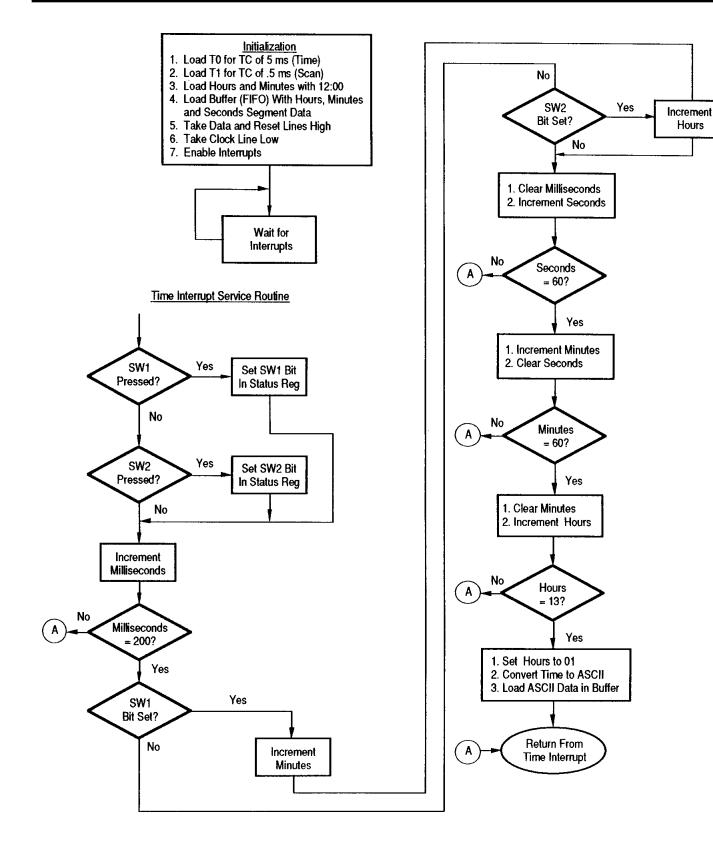


Figure 3a. Display Flowchart

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#### THE SOFTWARE (Continued)

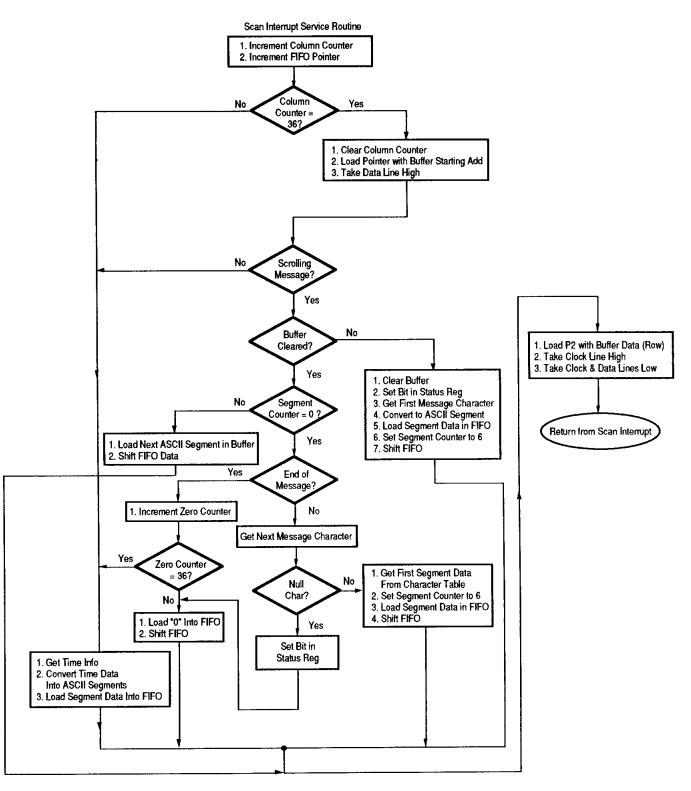


Figure 3b. Display Flowchart

At sixty-second intervals, the time display is blanked, and the internal message is scrolled across the display. The message is stored in an ASCII format. The individual ASCII characters index a look-up table, which converts the characters to a 6x7 format (first segment is a space). The software checks to see if all of the segments have been indexed at the beginning of the scan. If so, it then indexes the next character (Figures 4a and 4b).

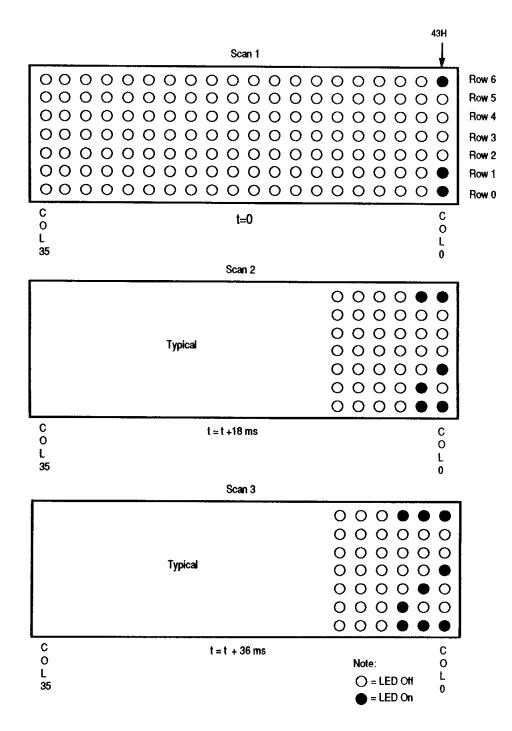
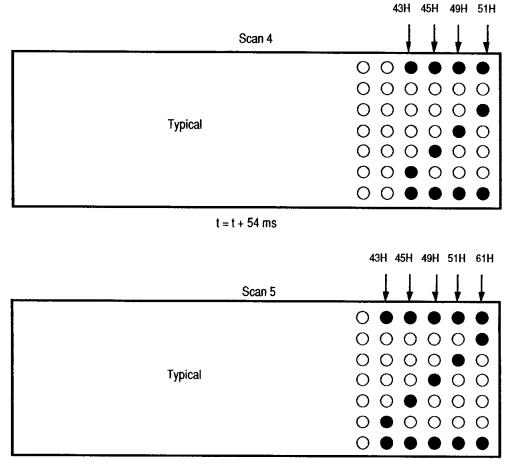


Figure 4a. Scrolling the Letter Z.

#### THE SOFTWARE (Continued)

For scrolling messages, the display buffer acts like a FIFO (First In - First Out). The FIFO is cleared at power-up. When the internal message is being indexed, the character segments are queued up in the FIFO. The FIFO size is determined by the size of the display. At the end of each scan, the next character segment is indexed, and is stored at the bottom of the FIFO. The character segments are then shifted up the FIFO one location. This process continues

until the entire message is displayed. At this time, a 0 is loaded into the FIFO at the beginning of each scan allowing the columns trailing the message to blank out. As the display is being scanned, the byte at each FIFO location is output at P2 as each column is turned on. The scrolling effect is created by shifting the FIFO data at the start of each scan (Figure 5).



t = t + 72 ms

Figure 4b. Scrolling the Letter Z.

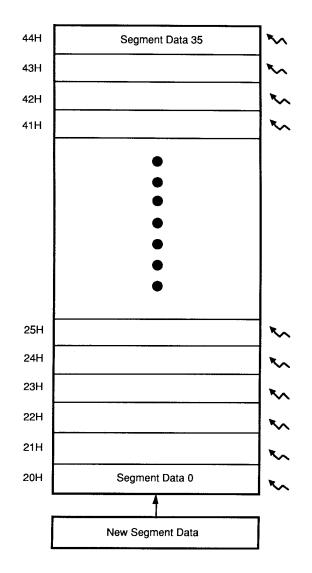


Figure 5. Shifting FIFO Data

### APPENDIX

		SCROLL1								
	LINE	SOURCE	-							
			******	******	***************************************					
	2	;			;					
	3	; This is a	a scrollin	ng LED (	lisplay routine using the Zilog Z86C08, 'C17 ;					
	4	; 18-pin CM	OS process	sor. The	e processor's P2 port outputs the row data, and ;					
	5	; the column	n data is	clocke	d out of PO into cascaded shift registers. It ;					
	6	; has a real	utes, and seconds. At every 60-second interval, it blanks the screen and ;							
	7									
	8				age. The message is stored in ROM, and can be up ;					
	9				th. After scrolling the message, the program re- ;					
	10				til the next 60 seconds.					
	11				s 36-columns long, enough to display six char- ;					
	12				ande longer, but the refresh time may need ad- ;					
	13				xer. Current refresh time is 500 microseconds, ;					
	14				of 8.00 MEz.					
	15				switches that are read to adjust the hours and ;					
	16				display will show 12:00.					
	17				by Don Owen Newquist on 12-1-91.					
					***************************************					
000000000000000000000000000000000000000		WORK REG	.equ	1 <b>0h</b>						
abs 00000000		address hi	.equ	r0						
abs 00000001		address lo	.equ	rl						
abs 00000000		address	.equ	rr0						
abs 00000002		pointer	.equ	r2						
abs 00000004		zero count	.equ	r4						
abs 00000005		temp 1	.equ	r5						
abs 00000006		temp 2	.equ	r6						
abs 00000007		temp 3	.equ	r7						
abs 00000008		col count	.equ	r8						
abs 00000009		seg count	.equ	r9						
000000000000000000000000000000000000000		TIME REG	.equ	00h						
abs 00000005		millisec	.equ	r5						
abs 00000006		seconds	.equ	r6						
abs 00000007		minutes	.equ	<b>r</b> 7						
abs 00000008		bours	.equ	r8						
abs 00000009		seconds lo	.equ	r9						
abs 0000000a		seconds hi	.equ	r10						
abs 0000000b		minutes lo	.equ	r11						
abs 0000000c	• •	minutes hi	.equ	r12						
abs 0000000d		hours lo	.equ	r13						
abs 0000000e		hours hi	.equ	r14						
abs 0000000f		sw count	.equ	r15						
000000000000000000000000000000000000000		STATUS	.equ	\$04						
000000000000000000000000000000000000000		MILLISEC	.equ	\$05						
000000000000000000000		SECONDS	.equ	\$06						
000000000000000000000000000000000000000		MINUTES	.equ	\$07						
000000000000000000000000000000000000000		HOURS	.equ	\$08						
0000000000000000000009		SECONDS LO	.equ	109						
0000000000000000000000000		SECONDS HI	.equ	<b>1</b> 0a						
000000000000000000b		NINUTES LO	.equ	<b>10</b> b						
000000000000000000000000000000000000000		NINUTES HI	.equ	\$0c						
00000000000000000000000		BOURS LO	.equ	\$0d						
0000000000000000000000		HOURS HI	.equ	<b>10e</b>						
000000000000000000000000000000000000000		BUFFER	.equ	\$20						
	54		. 1							
	55	•	STATUS	REG:	d4 d3 d2 d1 d0					
	56				displaying message					
	57	•			buffer cleared					
		-								

	58;		i I I .	
	50 ; 59 ;			and of message
	60;		•	lin sv pressed
	61;		jL	irs sv pressed
00000000	62	.org	00	
00000000 0000	63	.word	00	
0000002 0000	64	.word	00	
0000004 0000	65	.word	00	
00000006 0000	66	.word	00	
0000008 Www	67	.word	time	
0000000a Www	68	.word	shift	
000000c	69	.org	000ch	
	70 ;*********	******	******	*************************
	71 ;	Initi	alization	;
	72 ;*********	********	*****	*******************************
0000000c 3110	73 init:	srp	WORK_REG	
000000e 8f	74	di		; disable int
0000000f e6f464	75	1d	t0, <b>/16</b> 4	; 100 decimal
00000012 e6f5c9	76	ld	pre0,#11001001b	; set t0 for 5 mS period
00000015 e6f27d	77	1d	t1, <b>1</b> 125	;
00000018 e6f313	78	ld	pre1,#00010011b	; set t1 for .5 mS period
0000001b e6f600	79	ld	p2 <b>m</b> , <b>≢</b> 0	; outputs on p2
0000001e e6f701 00000021 e6f800	80	1đ	p3m,#1	; active on p2
0000021 001800	81 82	ld clr	<b>p01m</b> , <b>#</b> 0	; outputs on p0
00000024 b000	83	clr	p0	; p0 low
00000028 e6f908	84	14	sw_count ipr,#00001000b	; sv count = 0
0000002b e6fb30	85	14	imr,#30	<pre>; make irq5 &gt; irq3 ; enable irq4,irq5</pre>
00000028 e6ff80	86	ld	spl,#\$80	; set stack pointer
00000031 e6f10f	87	ld	tmr,#tof	; load and enable counters
00000034 2c04	88	1d	pointer,#104	; point to time regs
00000036 fc0c	89	ĩđ	r15, <b>#</b> 12	; six locations
00000038 ble2	90 clear reg:	clr	épointer	; clear ram
0000003a 2e	91	inc	pointer	;
0000003b fafb	92	djnz	r15,clear reg	; continue until all zero
0000003d d6Www	93	call	clear buffer	; clear buffer
00000040 e60812	94	1d	HOURS, \$12	; start time at 12:00
00000043 d6Www	95	call	load_time	; load starting time
00000046 2c20	96	1d	pointer, <b>/BUFFK</b> R	; start at top of buffer
00000048 e60003	97	1d	p0, <b>#000000</b> 11b	; take data and clear hi
0000004b 9f	98 main_loop:	ei		; enable interrupts
0000004c 8bfd	99	jr	main_loop	;
	100			
	101 ;**********		errupt routine updates the	*****
	102 ;		errupt routine updates the	•
0000004e 70fd	103 ;====================================	push	rp	; save current req pointer
00000050 3100	105	srp	TIME REG	; point to time reg group
00000052 d6Www	106	call	test sv	; look at time-set switches
00000055 5e	107	inc	millisec	; increment millisec req
00000056 a6e5c8	108	ср	millisec, #200	; one second?
00000059 7dWww	109	jp	ult,exit time	; exit if not
0000005c b0e5	110	clr	willisec	; set to zero
0000005e 760408	111	tm	STATUS, #00001000b	; sw 1 pressed?
00000061 6b**	112	jr	z,test_sw2	; no
00000063 060701	113	add	HIJUTES, 1	;
00000066 4007	114	da	HIJUTES	; convert to bcd
00000068 a60760	115	ср	NINUTES, #160	; sirty minutes?
000006b 7b**	116	jr	ult, inc_seconds	;
0000006d b007	117	clr	HINUTES	;

#### **APPENDIX** (Continued)

0000006f 8b**	118	jr	inc_seconds	;
00000071 760410	119 test_sw2:	t∎	STATUS, #00010000b	; sw 2 pressed?
0000007 <u>4</u> 6b**	120	r	z, inc_seconds	; no
00000076 060801	121	add	HOURS, 1	;
0000079 4008	122	da	HOURS	;
000007b a60813	123	ср	HOURS,#113	; 1:00?
0000007e 7b**	124	jr	ult,inc seconds	;
00000080 e60801	125	ld	HOURS, 1	;
00000083 06e601	126 inc seconds:	add	seconds, #1	; increment sec
00000086 40e6	127 -	da	seconds	; convert to bcd
00000088 a6e660	128	ср	seconds, #160	; sixty seconds?
0000008b 7b**	129	jr	ult,erit time	; no
0000008d 460401	130	or	STATUS, #00000001b	; set message flag
00000090 b0e6	131	clr	seconds	; set to zero
00000092 06e701	132	add	minutes,#1	; inc minutes
00000095 40e7	133	da	ninutes	; convert to bed
00000097 a6e760	134	Ср	ninutes,#160	; sixty minutes?
00000097 202700 0000009a 7b**	135	jr	ult, erit time	; not yet
0000009c b0e7	135	clr	ninutes	
				; set to zero
0000009e 06e801	137 set_hrs:	add	hours, 1	; inc hours
000000a1 40e8	138	da	hours	; convert to bod
000000a3 a6e813	139	ср	hours, 113	; 1:00?
000000a6 7b**	140	jr	· _	; exit
000000a8 8c01	141	1d	hours, 1	; set to 1:00
00000aa d6Www	142 exit_time:	call	time_convert	; convert to individual chars
00000ad deiwww	143	call	load_time	; load new values into buffer
000000b0 50fd	144	pop	rp	; return to orig reg pointer
000000b2 bf	145	iret		; return from int
	146			
		*******	******************	******************************
	148 ;		outine converts the second	
	149 ;	data i	nto units and tens-of-unit	ts for displaying ;
	149 ;	data i	nto units and tens-of-unit	
000000b3 e40609	149 ;	data i	nto units and tens-of-unit	ts for displaying ;
000000b3 e40609 000000b6 e4060a	149 ; 150 ;*********	data i:	nto units and tens-of-unit	s for displaying ;
	149 ; 150 ;************************************	data i ******** ld	nto units and tens-of-unit SECONDS_LO,SECONDS	ts for displaying ; ************************************
000000b6 e4060a	149; 150;************************************	data i ********* 1d 1d	nto units and tens-of-unit SECONDS_LO,SECONDS SECONDS_HI,SECONDS	ts for displaying ; ; transfer contents
000000b6 e4060a 000000b9 56090f	149; 150;******************** 151 time_convert: 152 153	data i ******** ld ld and	SECONDS_LO, SECONDS SECONDS_LO, SECONDS SECONDS_HI, SECONDS SECONDS_LO, # 30f SECONDS_HI	ts for displaying ; ; transfer contents ; ; keep only lower bits ; swap nibbles
000000b6 e4060a 000000b9 56090f 000000bc f00a	149; 150;******************* 151 time_convert: 152 153 154	data i d ld ld and swap	SECONDS_LO, SECONDS SECONDS_LO, SECONDS SECONDS_HI, SECONDS SECONDS_LO, # 10f SECONDS_HI SECONDS_HI SECONDS_HI, # 10f	ts for displaying ; ; transfer contents ; ; keep only lower bits
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f	149; 150;****************** 151 time_convert: 152 153 154 155	data i i i i i i i i i i i i i i i i i i i	SECONDS_LO,SECONDS SECONDS_HI,SECONDS SECONDS_HI,SECONDS SECONDS_HI SECONDS_HI SECONDS_HI SECONDS_HI SECONDS_HI,#30f NINUTES_LO,NINUTES	ts for displaying ; transfer contents ; ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b	149; 150;***************** 151 time_convert: 152 153 154 155 156	data i i ld ld and swap and ld	SECONDS_LO,SECONDS SECONDS_HI,SECONDS SECONDS_HI,SECONDS SECONDS_HI SECONDS_HI SECONDS_HI SECONDS_HI HINUTES_LO,MINUTES HINUTES_HI,MINUTES	ts for displaying ; ; ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; keep only lower bits ; transfer contents ;
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c4 e4070c 000000c7 560b0f	149; 150;************************************	data i: ld ld and swap and ld ld and	SECONDS_LO, SECONDS SECONDS_LO, SECONDS SECONDS_HI, SECONDS SECONDS_LO, # 10f SECONDS_HI SECONDS_HI SECONDS_HI HINTES_LO, MINUTES HINTES_HI, MINUTES HINTES_LO, # 10f	ts for displaying ; ; transfer contents ; ; keep only lower bits ; keep only lower bits ; keep only lower bits ; transfer contents ; ; keep only lower bits
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c4 e4070c 000000c7 560b0f 000000ca f00c	149; 150;************************************	data i: ld ld and swap and ld ld and swap	SECONDS_LO, SECONDS SECONDS_LO, SECONDS SECONDS_HI, SECONDS SECONDS_LO, # 10f SECONDS_HI SECONDS_HI SECONDS_HI NINUTES_LO, NINUTES NINUTES_HI, NINUTES NINUTES_HI	ts for displaying ; transfer contents ; ; transfer contents ; ; keep only lower bits ; ; keep only lower bits ; ; transfer contents ; ; keep only lower bits ; ; keep only lower bits ; ; swap nibbles ; ; swap nibbles ;
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c4 e4070c 000000c7 560b0f 000000ca f00c 000000cc 560c0f	149; 150;************************************	data i: data i: d ld and swap and ld ld and swap and	SECONDS_LO, SECONDS SECONDS_LO, SECONDS SECONDS_HI, SECONDS SECONDS_LO, # tof SECONDS_HI SECONDS_HI SECONDS_HI SECONDS_HI HINTES_LO, MINUTES MINUTES_HI, MINUTES HINTES_HI MINUTES_HI HINTES_HI, # tof	ts for displaying ; ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; swap nibbles ; keep only lower bits
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c4 e4070c 000000c7 560b0f 000000ca f00c 000000cc 560c0f 000000cc fe4080d	149; 150;************************************	data i: data i: d ld swap and ld ld swap and swap and ld	SECONDS LO, SECONDS SECONDS LO, SECONDS SECONDS HI, SECONDS SECONDS LO, # 10 SECONDS HI, # 10 SECONDS HI SECONDS HI HINTES LO, MINUTES HINTTES LO, # 20 MINUTES HI HINTES HI HINTES HI HINTES HI HINTES LO, HOURS	<pre>ts for displaying ; ts for displaying ; tt transfer contents ; ; keep only lower bits ; keep only lower bits ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; transfer contents ; </pre>
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c4 e4070c 000000c7 560b0f 000000ca f00c 000000cc 560c0f 000000cc 560c0f 000000cc e4080d 000000c2 e4080e	149; 150;************************************	data i: data i: d ld and swap and ld ld swap and ld ld ld ld ld	NTO UNITS and tens-of-unit SECONDS LO, SECONDS SECONDS HI, SECONDS SECONDS HI, SECONDS SECONDS LO, # TOF SECONDS HI, # TOF HINUTES LO, MINUTES HINUTES HI, MINUTES HINUTES HI HINUTES HI HINUTES HI HINUTES HI, # TOF HOURS LO, HOURS HOURS HI, HOURS	<pre>ts for displaying ; transfer contents ; ; transfer contents ; ; keep only lower bits ; keep only lower bits ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; transfer contents ; ; transfer contents ; ;</pre>
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000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c4 e4070c 000000c7 560b0f 000000c2 560c0f 000000cc 560c0f 000000cf e4080d 000000c2 e4080e 000000d2 e4080e	149; 150; ************************************	data i: data i: d ld and swap and ld ld ld ld ld ld ld and swap and swap and swap and swap	seconds Lo, Seconds SECONDS Lo, SECONDS SECONDS HI, SECONDS SECONDS HI, SECONDS SECONDS HI, SECONDS HI SECONDS HI SECONDS HI, # 10 HINUTES LO, # 10 HINUTES HI, MINUTES HINUTES HI, MINUTES HINUTES HI HINUTES HI HINUTES HI HINUTES HI HOURS LO, # 10 HOURS HI, HOURS HOURS LO, # 10 HOURS HI	<pre>ts for displaying ; transfer contents ; ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; keep</pre>
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c1 e4070c 000000c7 560b0f 000000cc 560c0f 000000cc 560c0f 000000cf e4080d 000000d2 e4080e 000000d5 560d0f 000000d8 f00e 000000da 560e0f	149; 150; ************************************	data i: data i: d ld swap and ld ld ld ld ld ld ld and swap and ld ld and	SECONDS LO, SECONDS SECONDS LO, SECONDS SECONDS HI, SECONDS SECONDS LO, # TOF SECONDS HI, # TOF SECONDS HI, # TOF HINUTES LO, # TOF HINUTES HI, # TOF HINUTES HI, # TOF HINUTES HI HINUTES HI HINUTES HI HINUTES HI, # TOF HOURS LO, # TOF HOURS LO, # TOF	<pre>ts for displaying ; ts for displaying ; t transfer contents ; t keep only lower bits ; keep only lower bits ; transfer contents ; keep only lower bits ; keep only lower bits ; transfer contents ; keep only lower bits ; </pre>
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c4 e4070c 000000c7 560b0f 000000c2 560c0f 000000cc 560c0f 000000cf e4080d 000000c2 e4080e 000000d2 e4080e	149; 150; ************************************	data i: data i: d ld and swap and ld ld ld ld ld ld ld and swap and swap and swap and swap	seconds Lo, Seconds SECONDS Lo, SECONDS SECONDS HI, SECONDS SECONDS HI, SECONDS SECONDS HI, SECONDS HI SECONDS HI SECONDS HI, # 20f HINUTES LO, MINUTES HINUTES HI, MINUTES HINUTES HI HINUTES HI HINUTES HI HINUTES HI HINUTES HI HOURS LO, # 20f HOURS HI, HOURS HOURS LO, # 20f HOURS HI	<pre>ts for displaying ; transfer contents ; ; transfer contents ; ; keep only lower bits ; keep only lower bits ; transfer contents ; ; keep only lower bits ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; keep</pre>
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c1 e4070c 000000c7 560b0f 000000cc 560c0f 000000cc 560c0f 000000cf e4080d 000000d2 e4080e 000000d5 560d0f 000000d8 f00e 000000da 560e0f	149; 150; ************************************	data i: data i: d ld and swap and ld ld ld ld ld and swap and ld ld and swap and ret	SECONDS LO, SECONDS SECONDS LO, SECONDS SECONDS HI, SECONDS SECONDS HI, SECONDS SECONDS HI SECONDS HI SECONDS HI SECONDS HI, # 100 HINUTES LO, MINUTES HINUTES HI, MINUTES HINUTES HI HINUTES HI HINUTES HI HINUTES HI HUNS HI, # 100 HOURS HI HOURS HI HOURS HI HOURS HI HOURS HI HOURS HI, # 10	<pre>ts for displaying ; transfer contents ; ; transfer contents ; ; keep only lower bits ; keep only lower bits ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; return</pre>
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c1 e4070c 000000c7 560b0f 000000cc 560c0f 000000cc 560c0f 000000cf e4080d 000000d2 e4080e 000000d5 560d0f 000000d8 f00e 000000da 560e0f	149; 150; ************************************	data i: data i: d ld and swap and ld ld ld ld and swap and ld ld and swap and control (control (contro) (control (control (control (control (contr	SECONDS LO, SECONDS SECONDS LO, SECONDS SECONDS HI, SECONDS SECONDS HI, SECONDS SECONDS HI SECONDS HI SECONDS HI SECONDS HI, # 10 HINUTES LO, MINUTES HINUTES HI, MINUTES HINUTES HI HINUTES HI HINUTES HI HINUTES HI HOURS LO, # 10 HOURS HI HOURS HI	<pre>s for displaying ; transfer contents ; ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; return</pre>
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c1 e4070c 000000c7 560b0f 000000cc 560c0f 000000cc 560c0f 000000cf e4080d 000000d2 e4080e 000000d5 560d0f 000000d8 f00e 000000da 560e0f	149 ; 150 ;************************************	data i: data i: d ld and swap and ld ld ld ld and swap and ld ld swap and control (control) swap and his subr	seconds LO, SECONDS SECONDS LO, SECONDS SECONDS HI, SECONDS SECONDS HI, SECONDS SECONDS HI SECONDS HI SECONDS HI SECONDS HI, # 10 HINUTES LO, MINUTES MINUTES HI, MINUTES MINUTES HI MINUTES HI MINUTES HI MINUTES HI HOURS LO, # 10 HOURS HI HOURS HI HI HOURS HI HI HOURS HI HI HI HI HI HI HI HI HI HI HI HI HI H	<pre>is for displaying ; is for displaying ; ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; into the RAM buffer ; </pre>
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c1 e4070c 000000c7 560b0f 000000cc 560c0f 000000cc 560c0f 000000cf e4080d 000000d2 e4080e 000000d5 560d0f 000000d8 f00e 000000da 560e0f	149 ; 150 ;************************************	data i: data i: d ld and swap and ld ld ld ld and swap and ld ld swap and control (control) swap and his subr	seconds LO, SECONDS SECONDS LO, SECONDS SECONDS HI, SECONDS SECONDS HI, SECONDS SECONDS HI SECONDS HI SECONDS HI SECONDS HI, # 10 HINUTES LO, MINUTES MINUTES HI, MINUTES MINUTES HI MINUTES HI MINUTES HI MINUTES HI HOURS LO, # 10 HOURS HI HOURS HI HI HOURS HI HI HOURS HI HI HI HI HI HI HI HI HI HI HI HI HI H	<pre>s for displaying ; transfer contents ; ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; return</pre>
000000b6 e4060a 000000b9 56090f 000000be 560a0f 000000c1 e4070b 000000c2 e4070c 000000c2 560b0f 000000cc 560c0f 000000cc 560c0f 000000d2 e4080e 000000d2 e4080e 000000d3 560e0f 000000d3 560e0f 000000da af	149 ; 150 ;************************************	data i: ld ld and swap and ld ld ld and swap and ld ld ld and swap and ta swap and ta swap and swap	SECONDS LO, SECONDS SECONDS LO, SECONDS SECONDS HI, SECONDS SECONDS HI, SECONDS HI, SECONDS HI SECONDS HI SECONDS HI NINUTES LO, NINUTES NINUTES HI, NINUTES NINUTES HI NINUTES HI NINUTES HI NINUTES HI HOURS LO, #30f HOURS HI, HOURS HOURS HI, HOURS HOURS HI, #40f	<pre>s for displaying ; transfer contents ; ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; hinto the RAM buffer ; </pre>
000000b6 e4060a 000000b9 56090f 000000be 560a0f 000000c1 e4070b 000000c2 e4070c 000000c2 560b0f 000000cc 560c0f 000000cc 560c0f 000000d2 e4080e 000000d2 e4080e 000000d3 f00e 000000d3 560e0f 000000da 360e0f 000000dd af	149 ; 150 ;************************************	data i: data i: d ld and swap and ld ld and swap and ld ld and swap and ta swap and ta swap and swap and swap and swap and swap and swap and swap and swap and swap and swap and swap and swap and swap and b swap and b swap and b swap and b swap and b swap and b b swap and b b b swap and b b b swap and b b b swap and b b b swap and b b b swap and b b b swap and b b b swap and b b swap and b b swap and b swap and b swap and b swap and b swap and b swap and b swap and b swap and b swap and b swap and b swap s	rp	<pre>is for displaying ; is for displaying ; it ransfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; return </pre>
000000b6 e4060a 000000b9 56090f 000000bc f00a 000000be 560a0f 000000c1 e4070b 000000c4 e4070c 000000c7 560b0f 000000c2 560c0f 000000cc 560c0f 000000d2 e4080e 000000d2 e4080e 000000d3 f00e 000000d3 f00e 000000da 560e0f 000000dd af	149 ; 150 ;************************************	data i: data i: d ld ld and swap and ld ld ld and swap and ld ld and swap and id ld swap and id swap and swap swap and swap swap and swap sw	rp WORK REG	<pre>is for displaying ; is for displaying ; ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; return ; ; save current reg pointer ; point to working reg</pre>
000000b6 e4060a 000000b9 56090f 000000be 560a0f 000000c1 e4070b 000000c2 e4070c 000000c2 560b0f 000000cc 560c0f 000000cc 560c0f 000000d2 e4080e 000000d2 e4080e 000000d3 f00e 000000d3 f00e 000000d3 560e0f 000000da af	149 ; 150 ;************************************	data i: data i: d ld and swap and ld ld ld and swap and ld ld and swap and ld ld swap and ld ld and swap and ld ld ld and swap and ld ld ld and swap and ld ld ld ld ld ld ld ld ld l	rp WORK REG r10, #409 r10, #409 r10, #409 r10, #407 r10, #407 r10, #407 r10, #407 r10, #407 r10, #407 r10, #407 r10, #407 r10, #409	<pre>s for displaying ; t s for displaying ; t transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; return ************************; ; save current reg pointer ; point to working reg ; load starting time reg</pre>
000000b6 e4060a 000000b9 56090f 000000be 560a0f 000000c1 e4070b 000000c1 e4070c 000000c7 560b0f 000000c2 560c0f 000000c2 560c0f 000000d2 e4080e 000000d2 e4080e 000000d3 500e0 000000d3 f00e 000000d3 560e0f 000000dd af	149; 150; ************************************	data i: data i: d ld ld and swap and ld ld ld and swap and ld ld and swap and ld ld swap and ld ld and swap and ld ld and swap and ld ld and swap and ld ld and swap and ld ld ld and swap and ld ld ld and swap and ld ld ld ld ld ld ld ld ld l	rp WORK REG	<pre>is for displaying ; is for displaying ; ; transfer contents ; ; keep only lower bits ; swap nibbles ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; transfer contents ; ; keep only lower bits ; return ; ; save current reg pointer ; point to working reg</pre>
000000b6 e4060a 000000b9 56090f 000000be 560a0f 000000c1 e4070b 000000c2 e4070c 000000c2 560b0f 000000cc 560c0f 000000cc 560c0f 000000d2 e4080e 000000d2 e4080e 000000d3 f00e 000000d3 f00e 000000d3 560e0f 000000da af	149 ; 150 ;************************************	data i: data i: d ld ld and swap and ld ld ld and swap and ld ld and swap and ld ld ld and swap and ld ld ld and swap and ld ld ld and swap and ld ld ld ld and swap and ld ld ld ld ld ld ld ld ld l	rp WORK REG r12, #10 r12, #10 r12, #10 r12, #10 r12, #10 r12, #10 r12, #10 r14, #00 r12, #10 r14, #00 r11, #00 r11, #00 r11, #00 r11, #00 r10, #10 r10 r10 r10 r10 r10 r10 r10 r	<pre>s for displaying ; t statustic terms for contents ; t transfer contents ; t keep only lower bits ; transfer contents ; t keep only lower bits ; keep only lower bits ; transfer contents ; t keep only lower bits ; transfer contents ; keep only lower bits ; transfer contents ; s keep only lower bits ; transfer contents ; s keep only lower bits ; transfer contents ; s keep only lower bits ; transfer contents ; s keep only lower bits ; transfer contents ; s keep only lower bits ; transfer contents ; s keep only lower bits ; transfer contents ; s keep only lower bits ; transfer contents ; s keep only lower bits ; transfer contents ; s keep only lower bits ; transfer contents ; i hout be RAM buffer ; i hout be RAM buffer ; i lower bits ; lower current reg pointer ; point to vorking reg ; lower starting buffer reg ; lower contents ; </pre>
000000b6 e4060a 000000b9 56090f 000000be 560a0f 000000c1 e4070b 000000c1 e4070c 000000c7 560b0f 000000c2 560c0f 000000c2 560c0f 000000d2 e4080e 000000d2 e4080e 000000d3 500e0 000000d3 f00e 000000d3 560e0f 000000dd af	149; 150; ************************************	data i: data i: d ld ld and swap and ld ld ld and swap and ld ld and swap and ld ld swap and ld ld and swap and ld ld and swap and ld ld and swap and ld ld and swap and ld ld ld and swap and ld ld ld and swap and ld ld ld ld ld ld ld ld ld l	rp WORK REG r12, #10 r12, #10 r12, #10 r12, #10 r12, #10 r12, #10 r12, #10 r14, #00 r12, #10 r14, #00 r11, #00 r11, #00 r11, #00 r11, #00 r10, #10 r10 r10 r10 r10 r10 r10 r10 r	<pre>s for displaying ; t s for displaying ; t transfer contents ; t transfer contents ; t keep only lower bits ; transfer contents ; t keep only lower bits ; keep only lower bits ; transfer contents ; t keep only lower bits ; transfer contents ; t keep only lower bits ; transfer contents ; t keep only lower bits ; transfer contents ; t keep only lower bits ; transfer contents ; s keep only lower bits ; transfer contents ; transfer contents ; keep only lower bits ; transfer contents ; transfer contents ; transfer contents ; transfer contents ; transfer co</pre>

000000ea 1c**	178	ld	address lo, / ^ lb number	table; load lo address of table
000000ec a6ec00	179	ср	r12, <b>1</b> 0	; is it zero?
000000ef 6b**	180	jr	eq, no index	; if yes, don't step thru table
000000f1 a0e0	181 index num:	incv	address	; step thru table
000000f3 a0e0	1 <b>82</b> –	incv	address	
000000f5 a0e0	183	incw	address	;
000000f7 a0e0	184	incw	address	;
000000f9 a0e0	185	incv	address	;
000000fb a0e0	186	incv	address	;
000000fd caf2	187	djnz	r12, index num	; index if not zero
000000ff cc06	188 no index:	lá	r12, <b>#</b> 6	; load no of segments
00000101 c3b0	189 load time reg	: ldci	er11, eaddress	; load into req
00000103 cafc	190	djnz	r12,load time req	; keep going if not zero
00000105 ae	191	inc	r10	; inc reg location
00000106 a6ea0f	1 <b>92</b>	ср	r10, <b>#10</b> f	; at ending reg?
00000109 7bdb	193	jr	ult, load table	; go again
0000010b e62b3a	194	ĺd	\$2b, <b>#</b> \$3a	; put colon here
0000010e e6373a	195	ld	\$37, <b>#</b> \$3a	; and here too
00000111 a60e00	196	ср	HOURS HI, 10	; tero?
00000114 eb**	197	jr	ne, load time ret	i
00000116 ac00	198	ĺd	r10,#0	; load zeros on last 5 columns
00000118 bc3e	199	1d	r11, <b>#</b> 3e	; starting here
0000011a cc05	200	1d	r12, <b>#</b> 5	; blank out leading zero
0000011c f3ba	201 leading loop:	ld	@r11,r10	;
0000011e be	202	inc	r11	; blank last five columns (hrs)
0000011f cafb	203	djnz	r12, leading loop	; step thru ram
00000121 50fd	204 load time ret	-	rp	; return to time reqs
00000123 af	205	ret	•	; return to caller
	206			
	207			
	208 ;*********	*******	*******	******
	209 ; This s	******* 1broutin	e checks to see if the t	ime-set switches are pressed. ;
	209 ; This s	******** 1broutin *******	e checks to see if the t	,
00000124 a803	209 ; This s	******* 1broutin ******* 1d	e checks to see if the t	ime-set switches are pressed. ;
00000124 a803 00000126 60ea	209 ; This su 210 ;**********	*******	e checks to see if the t	<pre>ime-set switches are pressed. ; ' ***********************************</pre>
	209 ; This su 210 ;*********** 211 test_sv:	******** 1d	e checks to see if the t. r10,p3	<pre>ime-set switches are pressed. ; ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;</pre>
00000126 60ea	209; This so 210;************ 211 test_sv: 212	1d com	<pre>checks to see if the t. r10,p3 r10</pre>	<pre>ime-set switches are pressed. ; ; load sw data ; 1's complement</pre>
00000126 60ea 00000128 56ea03	209; This so 210;************************************	ld com and	<pre>checks to see if the t. r10,p3 r10 r10,f03</pre>	<pre>ime-set switches are pressed. ; ; load sw data ; l's complement ; mask off upper bits</pre>
00000126 60ea 00000128 56ea03 0000012b 760301	209; This su 210;************ 211 test_sw: 212 213 214	ld com and tm	r10,p3 r10 r10,#03 p3,#1	<pre>ime-set switches are pressed. ; ************************************</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b**	209 ; This su 210 ;*********** 211 test_sw: 212 213 214 215	tn jr	r10,p3 r10 r10,#03 p3,#1 z,test_hrs	<pre>ime-set switches are pressed. ; ************************************</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000130 fe	209 ; This su 210 ;*********** 211 test_sw: 212 213 214 215 216	ld com and tm jr inc	r10,p3 r10 r10,#03 p3,#1 z,test_hrs sw_count	<pre>ime-set switches are pressed. ;  ; load sw data ; 1's complement ; mask off upper bits ; min pressed? ; no ; inc counter</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000130 fe 00000131 a6ef02	209 ; This su 210 ;*********** 211 test_sv: 212 213 214 215 216 217	ld com and tm jr inc cp	r10,p3 r10 r10,f03 p3,f1 r,test_hrs sw_count sw_count,f2	<pre>ime-set switches are pressed. ; ************************************</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000130 fe 00000131 a6ef02 00000134 7b**	209 ; This su 210 ;********** 211 test_sw: 212 213 214 215 216 217 218	ld com and tm jr inc cp jr	<pre>checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw</pre>	<pre>ime-set switches are pressed. ;  ***********************************</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000130 fe 00000131 a6ef02 00000134 7b** 00000136 460408	209 ; This su 210 ;*********** 211 test_sv: 212 213 214 215 216 217 218 219	ld com and tm jr inc cp jr or	<pre>checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b</pre>	<pre>ime-set switches are pressed. ;  ; load sw data ; l's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000130 fe 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b**	209 ; This so 210 ;********** 211 test_sv: 212 213 214 215 216 217 218 219 220	<pre>inc inc inc inc inc inc inc inc inc inc</pre>	e checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw	<pre>ime-set switches are pressed. ; ************************************</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000130 fe 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 0000013b 760304	209 ; This so 210 ;*********** 211 test_sv: 212 213 214 215 216 217 218 219 220 221 test_hrs:	transformed and the commendation of the commen	<pre>checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4</pre>	<pre>ime-set switches are pressed. ; ; ; load sw data ; l's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed?</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000130 fe 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 0000013b 760304 0000013e 6b**	209 ; This so 210 ;********** 211 test_sv: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222	********* ld com and tm jr inc cp jr or jr tm jr	<pre>e checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw</pre>	<pre>ime-set switches are pressed. ; ; ; load sw data ; l's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed? ; no</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 760304 0000013e 6b** 00000140 fe	209 ; This so 210 ;************ 211 test_sv: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223	******** ld com and tm jr inc cp jr or jr tm jr tm jr tm	<pre>e checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count</pre>	<pre>ime-set switches are pressed. ; ; ; load sw data ; l's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed? ; no ; inc debounce counter</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 760304 0000013e 6b** 00000140 fe 00000141 a6ef02	209 ; This so 210 ;********** 211 test_sv: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223 224	********* ld com and tm jr inc cp jr or jr tm jr tm jr cp	<pre>e checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count sw_count,f2</pre>	<pre>ime-set switches are pressed. ; ; ; load sw data ; l's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed? ; no ; inc debounce counter ; debounced?</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000136 6b** 00000141 a6ef02 00000144 7b**	209 ; This so 210 ;*********** 211 test_sv: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223 224 225	********* ld com and tm jr inc cp jr or jr tm jr tm jr cp jr cp jr	e checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count sw_count,f2 ult,exit_sw	<pre>ime-set switches are pressed. ; ; ; load sw data ; l's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit ; return to caller</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000140 fe 00000141 a6ef02 00000144 7b** 00000146 460410	209 ; This so 210 ;*********** 211 test_sv: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223 224 225 226	********* ld com and tm jr inc cp jr or jr tm jr tm jr cp jr or jr or	e checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count sw_count,f2 ult,exit_sw	<pre>ime-set switches are pressed. ; ; ; load sw data ; l's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000141 a6ef02 00000141 a6ef02 00000144 7b** 00000146 460410 00000149 af	209 ; This su 210 ;*********** 211 test_sw: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223 224 225 226 227 exit_sw:	********* ld com and tm jr inc cp jr or jr tm jr cp jr cp jr or ret	rl0,p3 rl0 rl0,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count,f2 ult,exit_sw sw_count sw_count,f2 ult,exit_sw STATUS,f00010000b	<pre>ime-set switches are pressed. ; ; ; load sw data ; l's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit ; return to caller</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000141 a6ef02 00000141 a6ef02 00000144 7b** 00000144 7b**	209 ; This su 210 ;*********** 211 test_sw: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223 224 225 226 227 exit_sw: 228 clear_sw:	********* ld com and tm jr inc cp jr or jr tm jr cp jr cp jr or tm and	<pre>checks to see if the t. r10,p3 r10 r10,#03 p3,#1 z,test_hrs sw_count sw_count,#2 ult,exit_sw STATUS,#00001000b exit_sw p3,#4 z,clear_sw sw_count sw_count,#2 ult,exit_sw STATUS,#00010000b STATUS,#11100111b</pre>	<pre>ime-set switches are pressed. ; ; ; load sw data ; 1's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit ; return to caller ; reset sw status bits</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000141 a6ef02 00000141 a6ef02 00000144 7b** 00000146 460410 00000149 af 00000149 af 00000144 5604e7 00000144 b0ef	209 ; This su 210 ;*********** 211 test_sw: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223 224 225 226 227 exit_sw: 228 clear_sw: 229 230 231	********* ld com and tm jr inc cp jr or jr tm jr cp jr or ret and clr ret	r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count sw_count,f2 ult,exit_sw STATUS,f00010000b STATUS,f11100111b sw_count	<pre>ime-set switches are pressed. ; ; ; load sw data ; l's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit ; return to caller ; reset sw status bits ; reset debounce counter ; return</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000141 a6ef02 00000141 a6ef02 00000144 7b** 00000146 460410 00000149 af 00000149 af 00000144 5604e7 00000144 b0ef	209 ; This ss 210 ;*********** 211 test_sv: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223 224 225 226 227 exit_sv: 228 clear_sv: 229 230 231 232 ;********	<pre>*********     ld     com     and     tm     jr     inc     cp     jr     or     jr     tm     jr     inc     cp     jr     or     ret     and     clr     ret ************************************</pre>	e checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count sw_count,f2 ult,exit_sw STATUS,f00010000b STATUS,f11100111b sw_count	<pre>ime-set switches are pressed. ; ; ; load sw data ; 1's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit ; return to caller ; reset sw status bits ; reset debounce counter ; return</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000141 a6ef02 00000141 a6ef02 00000144 7b** 00000146 460410 00000149 af 00000149 af 00000144 5604e7 00000144 b0ef	209 ; This ss 210 ;*********** 211 test_sv: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223 224 225 226 227 exit_sv: 228 clear_sv: 229 230 231 232 ;********	<pre>*********     ld     com     and     tm     jr     inc     cp     jr     or     jr     tm     jr     inc     cp     jr     or     ret     and     clr     ret ************************************</pre>	e checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count sw_count,f2 ult,exit_sw STATUS,f00010000b STATUS,f11100111b sw_count	<pre>ime-set switches are pressed. ; ; ; load sw data ; l's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; exit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit ; return to caller ; reset sw status bits ; reset debounce counter ; return</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000141 a6ef02 00000141 a6ef02 00000144 7b** 00000146 460410 00000149 af 00000149 af 00000144 5604e7 00000144 b0ef	209 ; This su 210 ;************************************	<pre>********     ld     com     and     tm     jr     inc     cp     jr     or     jr     tn     jr     inc     cp     jr     or     ret     and     clr     ret     s the tim     one.</pre>	rl0,p3 rl0 rl0,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count sw_count,f2 ult,exit_sw STATUS,f00010000b STATUS,f11100111b sw_count	<pre>ime-set switches are pressed. ; ; ; load sw data ; 1's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; erit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit ; return to caller ; reset sw status bits ; reset debounce counter ; return ************************************</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000141 a6ef02 00000141 a6ef02 00000144 7b** 00000146 460410 00000149 af 00000149 af 00000144 5604e7 00000144 b0ef	209 ; This su 210 ;********** 211 test_sv: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223 224 225 226 227 exit_sv: 228 clear_sv: 229 230 231 232 ;***********************************	<pre>********     ld     com     and     tm     jr     inc     cp     jr     or     jr     tn     jr     inc     cp     jr     or     ret     and     clr     ret     s the tim     one.</pre>	rl0,p3 rl0 rl0,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count sw_count,f2 ult,exit_sw STATUS,f00010000b STATUS,f11100111b sw_count	<pre>ime-set switches are pressed. ; ; load sw data ; 1's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; erit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit ; return to caller ; reset sw status bits ; reset debounce counter ; return  When T1 hits TC, column data is ; ; **********************************</pre>
00000126 60ea 00000128 56ea03 0000012b 760301 0000012e 6b** 00000131 a6ef02 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000141 a6ef02 00000141 a6ef02 00000144 7b** 00000146 460410 00000149 af 00000149 af 00000144 5604e7 00000144 b0ef	209 ; This su 210 ;************************************	<pre>********     ld     com     and     tm     jr     inc     cp     jr     or     jr     tn     jr     inc     cp     jr     or     ret     and     clr     ret     s the tim     one.</pre>	<pre>checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count sw_count,f2 ult,exit_sw STATUS,f00010000b STATUS,f11100111b sw_count er interrupt routine. rp</pre>	<pre>ime-set switches are pressed. ; ; load sw data ; 1's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; erit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit ; return to caller ; reset sw status bits ; reset debounce counter ; return ************************************</pre>
00000126 60ea 00000128 56ea03 00000128 760301 0000012e 6b** 00000130 fe 00000131 a6ef02 00000134 7b** 00000136 460408 00000139 8b** 00000139 8b** 00000139 6b** 00000141 a6ef02 00000141 a6ef02 00000144 7b** 00000144 7b** 00000144 5604e7 00000144 b0ef 0000014f af	209 ; This su 210 ;********** 211 test_sv: 212 213 214 215 216 217 218 219 220 221 test_hrs: 222 223 224 225 226 227 exit_sv: 228 clear_sv: 229 230 231 232 ;***********************************	<pre>********     ld     com     and     tm     jr     inc     cp     jr     or     jr     inc     cp     jr     or     jr     inc     cp     jr     or     inc     cp     jr     or     ret     and     clr     ret ************************************</pre>	e checks to see if the t. r10,p3 r10 r10,f03 p3,f1 z,test_hrs sw_count sw_count,f2 ult,exit_sw STATUS,f00001000b exit_sw p3,f4 z,clear_sw sw_count sw_count,f2 ult,exit_sw STATUS,f00010000b STATUS,f11100111b sw_count er interrupt routine.	<pre>ime-set switches are pressed. ; ; load sw data ; 1's complement ; mask off upper bits ; min pressed? ; no ; inc counter ; debouncd? ; not yet ; set bit ; erit ; hrs pressed? ; no ; inc debounce counter ; debounced? ; not yet ; set bit ; return to caller ; reset sw status bits ; reset debounce counter ; return  When T1 hits TC, column data is ; ; **********************************</pre>

### **APPENDIX** (Continued)

00000154 2e	238	inc		point to next location in ram
00000155 8e	239	inc	col_count	7
00000156 a6e824	240	ср		thirty-six columns?
00000159 7b**	241	jr	· · · ·	; end of screen?
0000015b b0e8	242	clr		reset col number
0000015d 2c20	243	1d	pointer, BUFFER	; start at beginning of buffer
0000015f 460002	244	or		; take data line high
00000162 760401	245 test_flag:	t∎		; time to scroll message?
00000165 6b**	246	jr		; no, display ti <b>n</b> e
00000167 d6Www	247	call		; load message data
0000016a 8b**	248	jr		load row data
0000016c d6R000+00de,	249 continue:	call	-	; get time data
0000016f e352	250 load_row:	1d	······································	load contents
0000017 <u>1</u> 60e5	251	CON	temp_1	;
00000173 5902	252	1d	p2,temp_1	out to port
00000175 460004	253 clock_it:	or	p0,#00000100b	; take clock hi
00000178 560001	254	and	p0,#0000001b ;	take clock and data low
0000017b 50fd	255	рор	rp	; restore reg pointer
0000017d bf	256	iret	;	*
	257 ;**********	*******	*****************	************
	258 ;		outine loads the message in	
	259 ;*********	*******	******************	**********
0000017e 760402	260 load_message:	tz		; clear buffer?
00000181 eb**	261	jr	nz,reg_scroll	;
00000183 d6Www	262	call	clear_buffer	clear contents of buffer
00000186 460402	263	or		; set bit
00000189 0c**	2 <b>64</b>	1d	address_hi, #^hb mess_beg	;
0000018b 1c**	265	ld	address_lo, / ^1b mess_beg	;
0000018d d6Wwww	266	call	get_ascii	; get first character
00000190 9c06	267	1d	seg_count,#6	; start out with six segs
00000192 8b**	268	jr	load_next_seg	;
00000194 a6e900	269 reg_scroll:	ср	<pre>seg_count,#0</pre>	; six segments loaded?
00000197 eb**	270	jr	ne,load_next_seg	; во
00000199 760404	271	tz		; end of message?
0000019c 6b**	272	jr	z,load_next_char	; load nert ascii char
0000019e 6c00	273	ld	temp_2,#0	;
000001a0 d6Wwww	274	call	load_fifo	; load data
000001a3 4e	275	inc	zero_count	; inc no of locations cleared
000001a4 a6e424	276	ср	zero_count, #36	; 36 locations yet?
000001a7 7b**	277	jr		; load segment data
000001a9 b004	278	clr	STATUS	; display time now
000001ab b0e4	279	clr	zero_count	; clear counter
000001ad 8b**	280	jr	scroll_return	; return
000001af 9006	281 load_next_char	:: 1d	<pre>seg_count,#6</pre>	; load 6 segments/character
000001b1 a0e0	282	incv		; point to nert ascii char
000001b3 d6Www	283	call		; get next character
000001b6 c26c	284 load_next_seg:	ldc	temp_2,@rr12	; load seg from ascii table
00001b8 d6Www	285	call		; shift the data
000001bb a0ec	286	incv	rr12	; point to next seg in table
000001bd 00e9	287	dec	seg_count	; decrement segment count
000001bf af	288 scroll_return:	ret		;
	289			
	/			**************
			ine loads and shifts the RA	
				***********************************
000001c0 fc24	293 load_fifo:	ld		; load number of columns
000001c2 2c20	294	ld		; load starting buffer reg
000001c4 e372	295 shift_fifo:	ld		; get data
000001c6 f326				
	296	1d	<pre>@pointer,temp_2</pre>	; load new data
000001c8 68e7	296 297	1d 1d	• • •	; load new data ; transfer bytes

000001ca 2e	298	inc	pointer	; next buffer address
000001cb faf7	299	djnz	r15,shift_fifo	; load all columns
000001cd af	300	ret	*****	; return to caller
				*****
	303 ;*******		tttttttttttttttttttttttttttttttttttttt	e and fetches the segment data. ;
000001ce cc**	304 get ascii:	1d	r12, * hb char table	; load starting add of table
000001d0 dc**	305	1d	r13, f^lb char table	:
000001d2 c2ea	306	ldc	r14,@rr10	; load ascii data
000001d4 a6ee00	307	ср	r14,#0	; end of message?
000001d7 eb**	308	jr	ne,load_nert	; no
000001d9 460404	309	or	STATUS, 100000100b	; set bit to mark mess end
000001dc 8b**	310	jr	mess_return	; return
000001de 26ee20	311 load_next:	sub	r14, <b>#</b> 20	; subtract 20h
000001e1 a6ee00	312	ср	r14, <b>#</b> 0	; is it a space?
000001e4 6b**	313	jr	eg,mess_return	; if yes, don't index table
000001e6 a0ec	314 inder_table:		rr12	; index table
000001e8 a0ec	315	INCW	rr12	;
000001ea a0ec	316	incv	rr12	;
000001ec a0ec	317	incv	rr12	
000001ee a0ec 000001f0 a0ec	318 319	incw	rr12 rr12	
00000110 adec	320	djnz	rl4, index table	; ; keep going if not zero
00000112 ear2	321 mess return:		TIA'INGET CODIC	, keep going it not zero
	322	100		1
		********	*****	******
	324 ;	This subro	outine clears the RAM but	ffer.
	325 ;*********			**********
000001f5 fc24	326 clear_buffer	:: 1ð	r15, <b>#</b> 36	; get no of columns
000001f7 2c20	327	1d	pointer, #BUFFER	; starting point of buffer
000001f9 ble2	328 clear_loop:	clr	<b>e</b> pointer	; clear contents
000001fb 2e	329	inc	pointer	; next location
000001fc fafb	330	djnz	r15,clear_loop	; till out of columns
000001fe af	331	ret		; return to caller
	332			******
	333 ;********** 334 ;			up to 80 ASCII characters ;
	335 :*******	10000490 Ua	ta area. Hessaye can be i	**************************************
00000200	336	.org	200h	,
00000200	337 mess beq:	··,		
00000200 5448495320444953	338	.asciz	THIS DISPLAY IS POWER	ED BY IILOG!'
00000208 504c415920495320				
00000210 504f574552454420				
00000218 4259205a494c4f47				
00000220 2100				
	339			
	· · · ·			****
			CII character look-up ta	1D10. ; ************************************
00000280	343	.orq	280h	***************************************
00000280	344 char table:	.019	2001	
00000280 000000000000	345	.byte	0,0,0,0,0,0	; space
00000286 0000007d00	346	.byte		; !
0000028b 000070007000	347	.byte	0,0,70H,0,70H,0	- H - H
00000291 00147f147f14	348	.byte	0,14H,7FH,14H,7FH,14H	; #
00000297 00122a7f2a24	349	.byte	0,12H,2AH,7FH,2AH,24H	
0000029d 006264081323	350	.byte	0,62H,64H,08H,13H,23H	
000002a3 003649350205	351	.byte	0,368,498,358,028,058	. ; &
000002a9 000000700000	352	.byte	0,00,00,70H,00,00	; /
000002af 001c22410000	353	.byte	0,1CH,22H,41H,0,0	;(

#### **APPENDIX** (Continued)

000002b5 00000041221c	354	.byte	0,0,0,41H,22H,1CH	;)
000002bb 0022147f1422	355	.byte	0,22H,14H,7FH,14H,22H	; *
000002c1 0008083e0808	356	.byte	0,08H,08H,3KH,08H,08H	;+
000002c7 000001060000	357	.byte	0,0,1,6,0,0	;,
000002cd 000808080808	358	.byte	0,8,8,8,8,8	; -
000002d3 00000010000	359	.byte	0,0,0,1,0,0	;.
000002d9 000204081020	360	.byte	0,2,4,8,10H,20H	;/
	361 ;numbers	•		• •
000002df 003e4549513e	362 number table:	.byte	0,3EH,45H,49H,51H,3EH	; 0
000002e5 0000217f0100	363 -	.byte	0,0,21H,7FH,01,0	; 1
000002eb 002345494931	364	.byte	0,23H,45H,49H,49H,31H	; 2
000002f1 004241495966	365	.byte	0,428,418,498,598,668	; 3
000002f7 000c14247f04	366	.byte	0,0CE,14E,24E,7FE,04E	; 4
000002fd 00725151514e	367	.byte	0,72H,51H,51H,51H,4KH	; 5
00000303 001e29494946	368	.byte	0,1KH,29H,49H,49H,46H	; 6
00000309 004047485060	369	.byte	0,40E,47E,48E,50E,60E	; 7
0000030f 003649494936	370	.byte	0,36H,49H,49H,49H,36H	; 8
00000315 003149494a3c	371	.byte	0,31H,49H,49H,4AH,3CH	;9
	372 ; NORE SPEC			, ,
0000031b 000000140000	373 HOLE SEL			
00000321 000001160000	374	.byte	0,0,0,14H,0,0	;:
00000327 000814224100	375	.byte	0,0,1,16H,0,0	;;
		.byte	0,8,14H,22H,41H,0	; <
0000032d 001414141414	376	.byte	0,14E,14E,14E,14E,14E	; =
00000333 000041221408	377	.byte	0,0,41E,22E,14E,08E	;>
00000339 0020404d5020	378	.byte	0,20H,40H,4DH,50H,20H	;?
	•		CASE LETTERS	;
0000033f 003e415d4d39	380	.byte	0,3KH,41H,5DH,4DH,39H	;@
00000345 001f2444241f	381	.byte	0,1FE,24E,44E,24E,1FE	; 1
0000034b 007f49494936	382	.byte	0,7 <b>FH,49H,49H,49H,36</b> H	; B
00000351 003e41414122	383	.byte	0,3KH,41H,41H,41H,22H	; C
00000357 007f4141413e	384	.byte	0,7FE,41E,41E,41E,3EE	; D
0000035d 007f49494941	385	.byte	0,7FH,49H,49H,49H,41H	; E
00000363 007f48484840	386	.byte	0,7FH,48H,48H,48H,40H	; F
00000369 003e41414547	387	.byte	0,3EH,41H,41H,45H,47H	; G
0000036f 007f0808087f	388	.byte	0,7FE,08E,08E,08E,7FE	; H
00000375 0000417f4100	389	.byte	0,00H,41H,7FH,41H,00H	; I
0000037b 00020101017e	390	.byte	0,02H,01H,01H,01H,7EH	; J
00000381 007f08142241	391	.byte	0,7FH,08H,14H,22H,41H	; K
00000387 007f01010101	392	.byte	0,7FH,01H,01H,01H,01H	; L
0000038d 007f2018207f	393	.byte		. N
00000393 007f1008047f	394	.byte	0,7FH,10H,08H,04H,7FH	
00000399 003e4141413e	395	.byte	0,3EH,41H,41H,41H,3EH	
0000039f 007f48484830	396	.byte	0,7FH,48H,48H,48H,30H	
000003a5 003e4145423d	397	.byte	0,3EH,41H,45H,42H,3DH	; 0
000003ab 007f484c4a31	398	.byte		; R
000003b1 003249494926	399	.byte	0,328,498,498,498,268	; 5
000003b7 0040407f4040	400	.byte		; T
000003bd 007e0101017e	401	.byte	0,7KH,01H,01H,01H,7KH	; 0
000003c3 007c0201027c	402	.byte		; V
000003c9 007f020c027f	403	.byte		; W
000003cf 006314081463	404	.byte		
000003d5 0060100f1060	405	.byte		; X
000003db 004345495161	405	.byte	0,43H,45H,49H,51H,61H	; Y
000003e1 007f7f414141	407	.byte	0,7FE,7FE,41E,41E,41E	
000003e7 002010080402	407	.byte		
000003ed 004141417f7f			0,20H,10H,08H,04H,02H	
000003f3 000408100804	409	.byte		;]
	410	.byte	0,04E,08E,10E,08E,04E	
000003f9 000101010101	411	.byte	0,01H,01H,01H,01H,01H	• -
			-,,,,,	1 -
	412 413	.end		, -

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