zilog

CUSTOMER PROCUREMENT SPECIFICATION

Z86C91

CMOS Z8® ROMLESS MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C91 microcontroller (MCU) introduces a new level of sophistication to single-chip architecture. The Z86C91 is a ROMless Z8 single-chip microcontroller family with 236 bytes of RAM.

The MCU is packaged in a 40-pin DIP, 44-pin PLCC, or a 44-pin LOFP and is manufactured in CMOS technology. The Z86C91 is a ROMless part and offers the use of external memory which enables this Z8 microcontroller to be used where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C91 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C91 offers 24 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provided timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory, and 236 general-purpose registers.

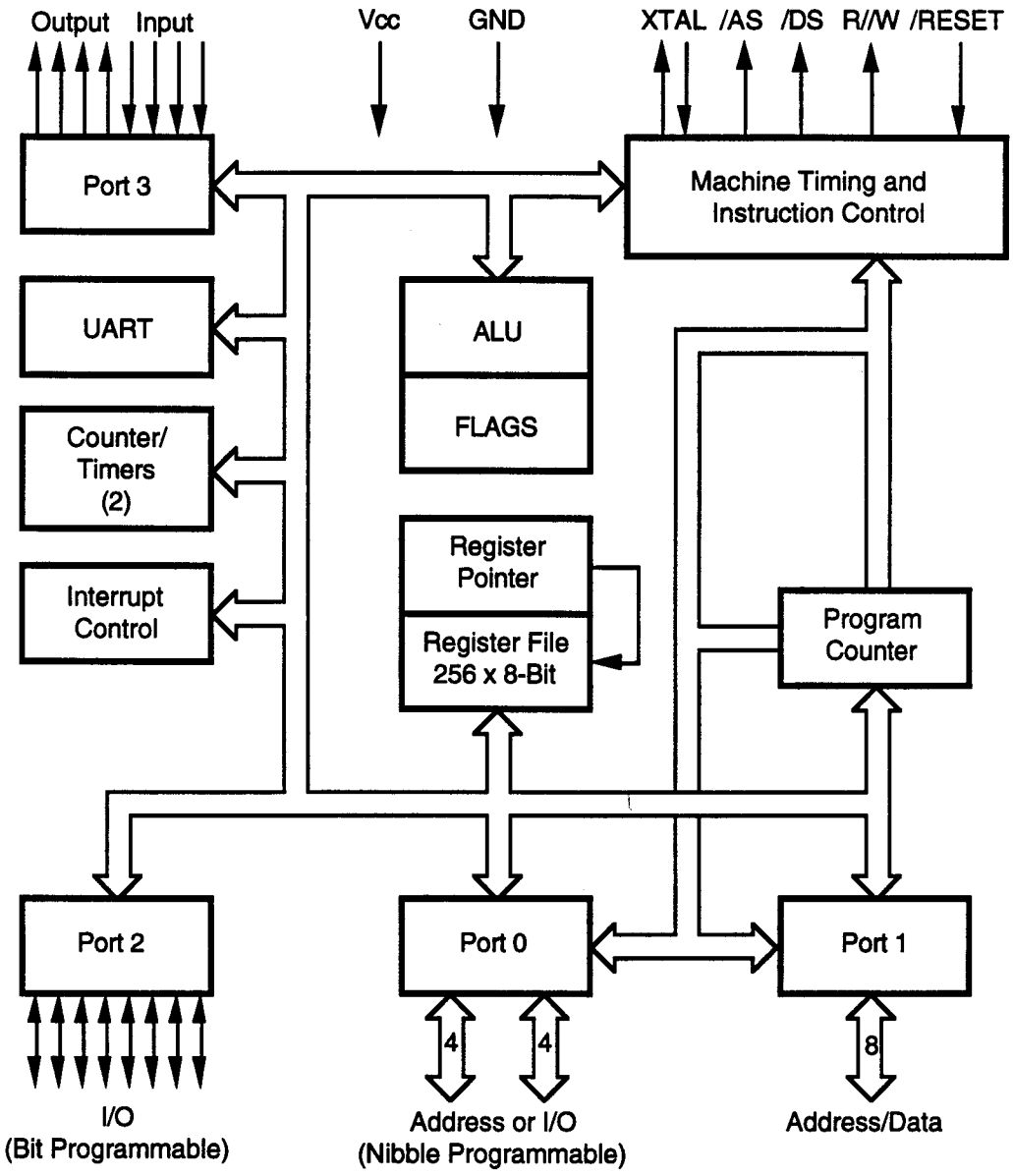
To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C91 offers two on-chip counter/timers with a large number of user selectable modes, and a universal asynchronous receiver/transmitter (Functional Block).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

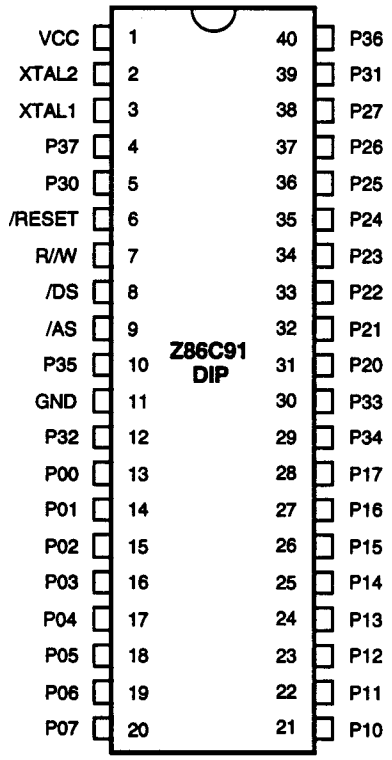
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

BLOCK DIAGRAM

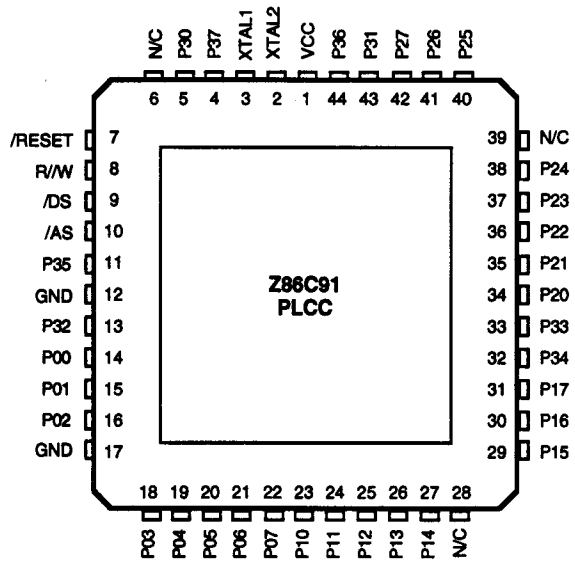


Functional Block Diagram

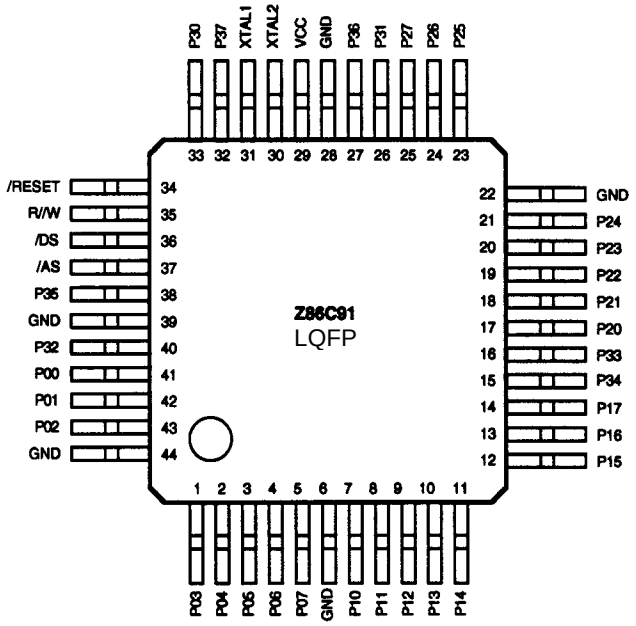
PIN DESCRIPTION



40-Pin DIP Pin Assignments



44-Pin PLCC Pin Assignments



44-Pin LQFP pin Assignments

ABSOLUTE MAXIMUM RATINGS

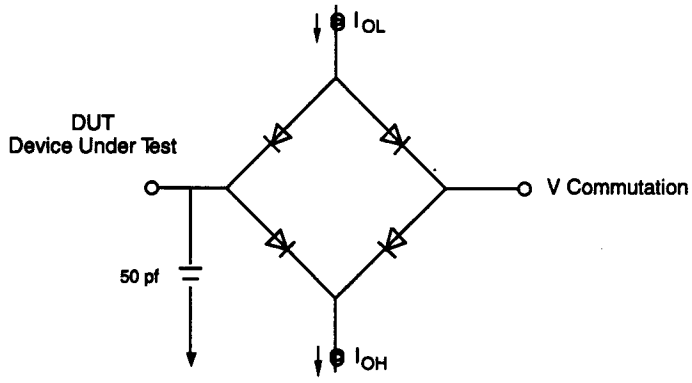
Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp		†	°C

Notes:
* Voltages on all pins with respect to GND.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 18).



Test Load Diagram

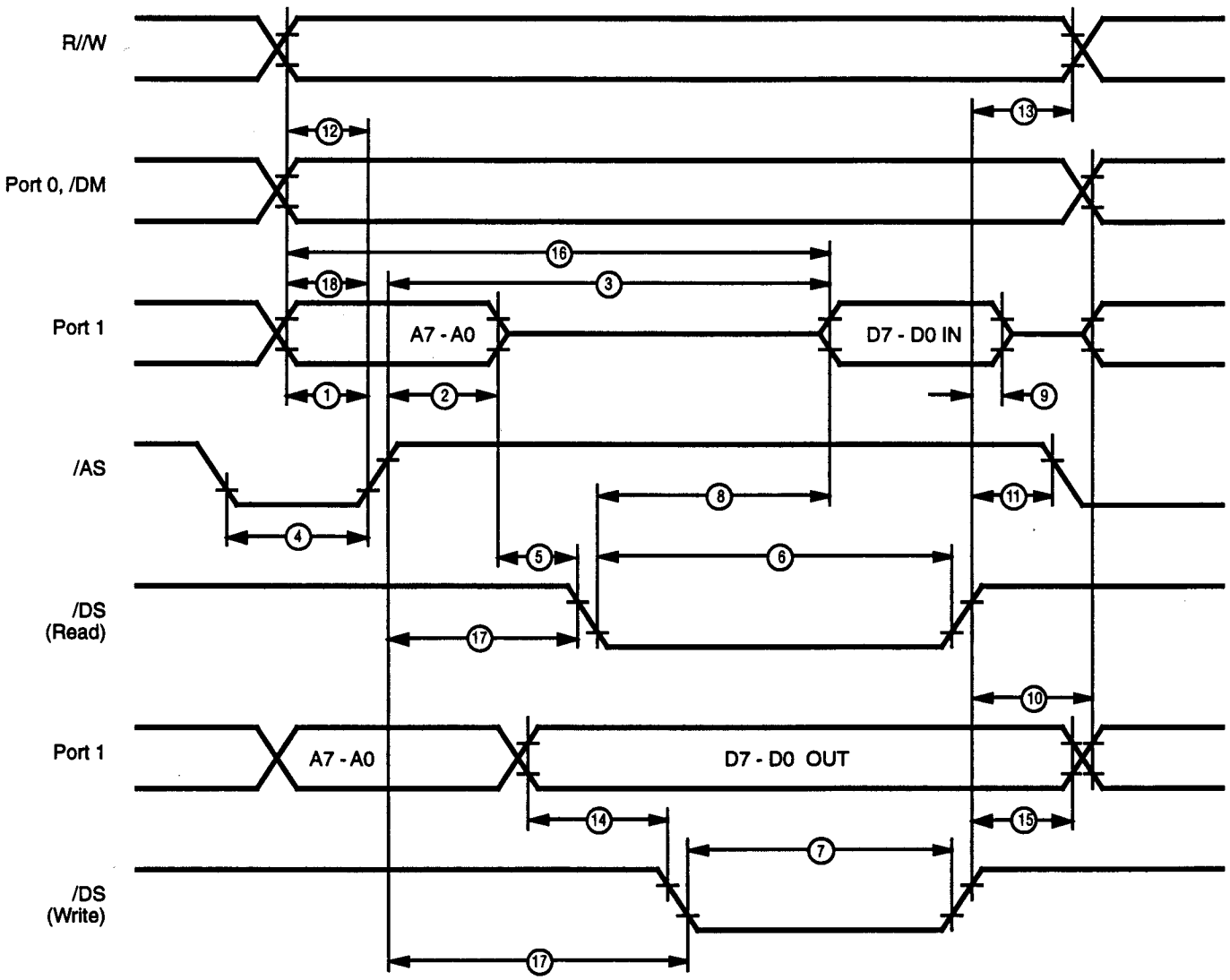
DC CHARACTERISTICS

Sym	Parameter	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		7		V	I_{IN} < 250 µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	−0.3	0.8	−0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	V_{CC}	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	−0.3	0.8	−0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = −2.0 mA
V_{OH}	Output High Voltage	V_{CC} −100 mV		V_{CC} −100 mV			V	I_{OH} = −100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	
V_{RL}	Reset Input Low Voltage	−0.3	0.8	−0.3	0.8		V	
I_{IL}	Input Leakage	−2	2	−2	2		µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	−2	2	−2	2		µA	V_{IN} = 0V, V_{CC}
I_{IR}	Reset Input Current		−180		−180		µA	V_{RL} = 0V
I_{CC}	Supply Current		30		30	20	mA	@ 12 MHz [1]
			40		40	24	mA	@ 16 MHz [1]
			50		50		mA	@ 20 MHz [1]
I_{CC1}	Standby Current		6.5		6.5	4	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz [1]
			7		7	4.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 16 MHz [1]
			8.5		8.5		mA	HALT mode V_{IN} = 0V, V_{CC} @ 20 MHz [1]
I_{CC2}	Standby Current		10		20	1	µA	STOP mode V_{IN} = 0V, V_{CC} [1]
I_{ALL}	Auto Latch Low Current	−16	16	−16	16	5	µA	

Note:
[1] All inputs driven to either 0V or V_{CC}, outputs floating.

AC CHARACTERISTICS

External I/O or Memory Read/Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Table

			T_A = 0°C to +70°C						T_A = −40°C to +105°C							
			12 MHz		16 MHz		20 MHz		12 MHz		16 MHz		20 MHz			
No	Sym	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	35		25		20		35		25		20		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		35		25		45		35		25		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		250		180		150		250		180		150	ns	[1,2,3]
4	TwAS	/AS Low Width	55		40		30		55		40		30		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		105		185		135		105		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		65		110		80		65		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75		55		130		75		55	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		0		0		0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	65		50		40		65		50		40		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	45		35		25		45		35		25		ns	[2,3]
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	30		25		20		33		25		20		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	50		35		25		50		35		25		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		20		35		25		20		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	55		35		25		55		35		25		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		310		230		180		310		230		180	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	65		45		35		65		45		35		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS Rise Delay	50		30		20		50		30		20		ns	[2,3]

Notes:

[1] When using extended memory timing add 2TpC.

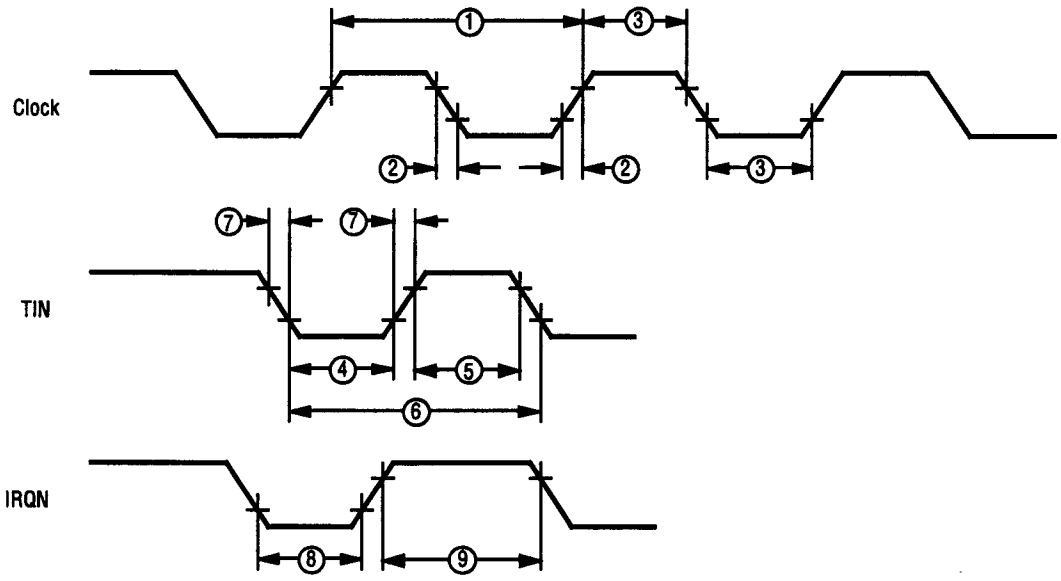
[2] Timing numbers given are for minimum TpC.

[3] See clock cycle dependent characteristics table.

Standard Test Load

All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

AC CHARACTERISTICS
Additional Timing Diagram



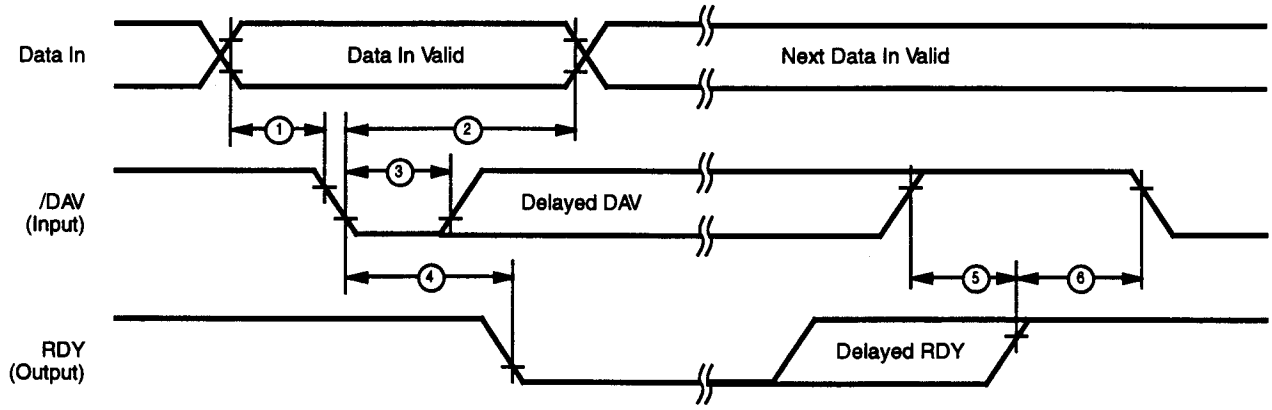
Additional Timing

AC CHARACTERISTICS
Additional Timing Table

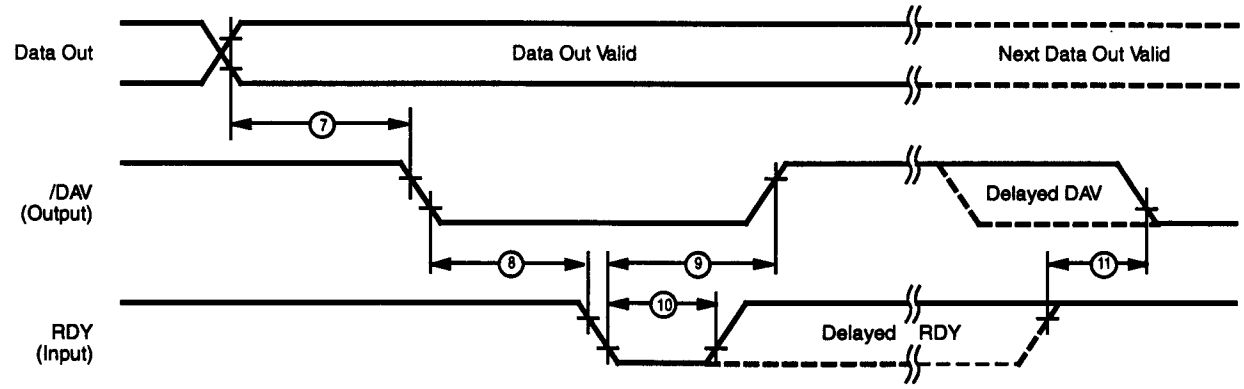
			T_A = 0°C to +70°C						T_A = −40°C to +105°C							
			12 MHz		16 MHz		20 MHz		12 MHz		16 MHz		20 MHz			
No	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	83	1000	62.5	1000	50	1000	83	1000	62.5	1000	50	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		15		10		10		15		10		10	ns	[1]
3	TwC	Input Clock Width	35		25		15		35		25		15		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		75		75		75		75		ns	[2]
5	TwTinH	Timer Input High Width	3TpC		3TpC		3TpC		3TpC		3TpC		3TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC		8TpC		8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		70		70		70		70		70		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC		5TpC		5TpC		5TpC		5TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC		3TpC		3TpC		3TpC		3TpC		3TpC			[2,3]

Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

No	Sym	Parameter	T_A = 0°C to +70°C 12, 16, and 20 MHz Min	Max	T_A = −40°C to +105°C 12, 16, and 20 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV fall to RDY fall Delay		115		115	IN
5	TdDAVId(RDY)	DAV rise to RDY rise Delay		115		115	IN
6	TdRDYO(DAV)	RDY rise to DAV fall Delay	0		0		IN
7	TdDO(DAV)	Data Out to DAV fall Delay		TpC		TpC	OUT
8	TdDAVO(RDY)	DAV fall to RDY fall Delay	0		0		OUT
9	TdRDYO(DAV)	RDY fall to DAV rise Delay		115		115	OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDYOd(DAV)	RDY rise to DAV fall Delay		115		115	OUT

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.