Z80182/Z8L182

Intelligent Peripheral Controller

Reference Manual

RM000201-0901

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Z80182/Z8L182
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Overview

FEATURES

Table 1. Device Features

Device	CPU	UART	USART I/O	Speed (MHz)
Z80182	S180	16550 ESCC	24	16,18,33
Z8L182	S180	16550 ESCC	24	20

- Enhanced Z8S180 MPU
  - Code Compatible with Zilog Z80™/Z180™ CPU
  - Extended Instructions
  - On-Chip 1 MB MMU
  - Two Enhanced UART Channels (Up to 512 Kbps)
  - Two Chain-Linked DMA Channels
  - X2 Clock Multiplier
  - Low-Power Consumption Modes
  - Two 16-Bit Timer/Counters
  - Clocked Serial I/O
  - On-Chip Wait-State Generators
  - On-Chip Interrupt Controller
  - On-Chip Oscillator/Generator
- 16550 Compatible MIMIC Interface
  - 16 mA MIMIC Output Drive Capability
- Two Z85230 Enhanced Serial Communications Controllers (ESCC) Channels

- 100-pin QFP and VQFP Packages
- Three 8-Bit Parallel I/O Ports
- 5.0V and 3.3V Operating Range

GENERAL DESCRIPTION

The Z80182/Z8L182 SL1932/1933 is an Intelligent peripheral controller chip used for modems, faxes, voice messaging and other data communications applications. This version is backward-compatible with all previous Z80182 versions. The Z80182 supports 5.0V operation up to 33 MHz, while the low-voltage 3.3V Z8L182 supports operating frequencies up to 20 MHz.

The enhanced Z80182/Z8L182 consists of an enhanced Z8S180 microprocessor linked with a dual channel of the industry-standard ESCC, 24 bits of parallel I/O, and a 16550 MIMIC for direct connection to the IBM PC, XT, AT bus. Current PC modem software compatibility can be maintained with the Z80182's ability to mimic the 16550 UART Chip. In modem applications, the Z8S180 core is the intelligent controller between the ESCC and 16550 MIMIC interface when used in internal PC applications and between the two ESCC channels in external PC applications. The Z182 intelligent controller can be used to perform the data compression and error correction on outgoing and incoming data.

The enhancements that were implemented into the S180 design were made to the ASCIs, DMAs, and ICC Standby Mode power consumption. With the addition of "ESCC-like" Baud Rate Generator (BRG), the two ASCIs now have the flexibility and capability to transfer data asynchronously at rates up to 512 Kbps. In addition, the ASCI channels FIFO size have been deepened to decrease the number of interrupts; the receive FIFO have been upgraded to 4 bytes and the transmit FIFO have been upgraded to 2 bytes.

The DMA allows for a "chain-linking" of the two DMA channels when set to take their DMA requests from the same peripheral device. This

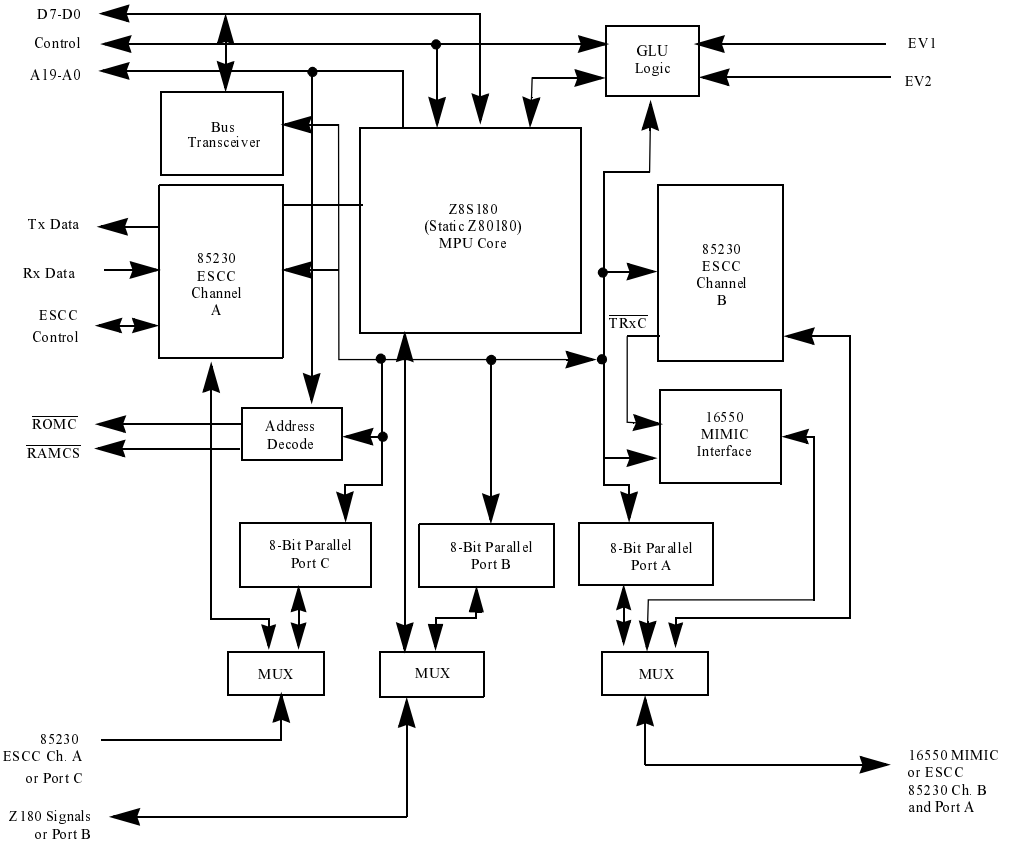
feature provides for higher DMA transfer rates, while reducing the amount of CPU intervention. Finally, the ICS power consumption during Standby Mode (or any of the Power-Down Modes, which involves the stopping of the CPU core) was improved to reduce current to a minimum, in the range of 50A.

A new clock doubler feature has been implemented in the new S180 device that allows the programmer to double the internal clock from that of the external clock.

The SL1933 includes an upgraded 180 CPU core. This backward compatible core contains A revision I.D. register (0xDA, value 9F for Rev K) is also included to allow for software differentiation (if needed) between Z80182 revisions and older devices.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}



Note: Conventional use of the term "MPU side" refers to all interface through the Z180 MPU cor and "PC side" refers to all interface through the 16550 MIMIC interface.

Figure 1. Z80182/Z8L182 Functional Block Diagram

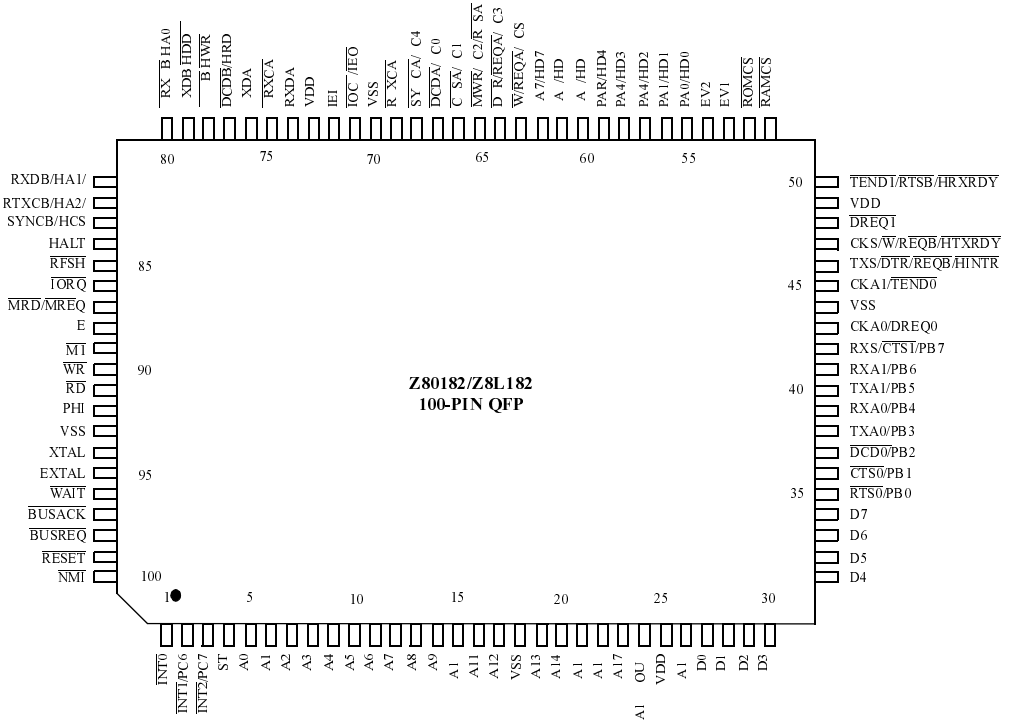


Figure 2. Z80182/Z8L182 100-Pin QFP Pin Configuration

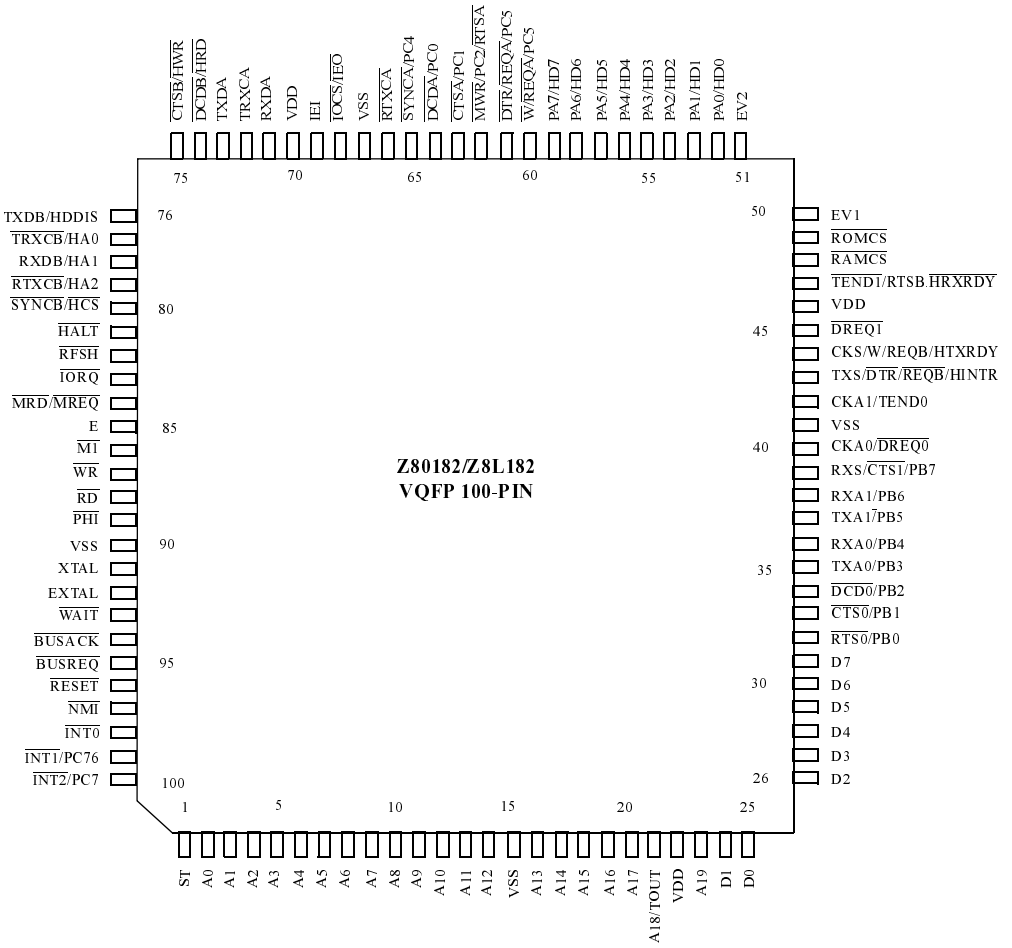


Figure 3. Z80182/Z8L182 100-Pin VQFP Pin Configuration

Signal and Pin Descriptions

Z180™ CPU SIGNALS

A19-A0. *Address Bus (input/output, active High, tristate)*. A19-A0 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges up to 1Mbyte, and I/O data bus exchanges up to 64K. The address bus enters a high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states. This bus is an input when the external bus master is accessing the on-chip peripherals. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset).

D7-D0. *Data Bus (bi-directional, active High, tristate)*. D7-D0 constitute an 8-bit bi-directional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states.

$\overline{\text{RD}}$. *Read (input/output, active Low, tristate)*. $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device uses this signal to gate data onto the CPU data bus.

$\overline{\text{WR}}$. *Write (input/output, active Low, tristate)*. MR indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

$\overline{\text{IORQ}}$. *I/O Request (input/output, active Low, tristate)*. $\overline{\text{IORQ}}$ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. $\overline{\text{IORQ}}$ is also generated, along with $\overline{\text{M1}}$, during the acknowledgment of the $\overline{\text{INTO}}$ input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the IOE signal of the Z64180.

$\overline{\text{M1}}$. *Machine Cycle 1 (input/output, active Low)*. Together with $\overline{\text{MREQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is the Op Code fetch cycle of an instruction execution; unless $\overline{\text{M1}}$E bit in the OMCR is cleared to 0. Together with $\overline{\text{IORQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is for an interrupt acknowledge. It is also used with the $\overline{\text{HALT}}$ and ST signals to decode status of the CPU machine cycle. This signal is analogous to the $\overline{\text{LIR}}$ signal of the Z64180.

$\overline{\text{MREQ}}$. *Memory Request (input/output, active Low, tristate)*. $\overline{\text{MREQ}}$ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the $\overline{\text{LIR}}$ signal of the Z64180. $\overline{\text{MREQ}}$ is multiplexed with $\overline{\text{MRD}}$ on the $\overline{\text{MRD}}$/$\overline{\text{MREQ}}$ pin. The $\overline{\text{MRD}}$/$\overline{\text{MREQ}}$ pin is an input during adapter modes; is tristate during bus acknowledge if the $\overline{\text{MREQ}}$ function is selected; and is inactive High if $\overline{\text{MRD}}$ function is selected.

$\overline{\text{MRD}}$. *Memory Read (input/output, active Low, tristate)*. $\overline{\text{MRD}}$ is active when both the internal $\overline{\text{MREQ}}$ and $\overline{\text{RD}}$ are active. $\overline{\text{MRD}}$ is multiplexed with $\overline{\text{MREQ}}$ on the $\overline{\text{MRD}}$/$\overline{\text{MREQ}}$ pin. The $\overline{\text{MRD}}$/$\overline{\text{MREQ}}$ pin is an input during adapter modes; is tristate during bus acknowledge if $\overline{\text{MREQ}}$ function is selected; and is inactive High if $\overline{\text{MRD}}$ function is selected. The default function on power up is $\overline{\text{MRD}}$ and may be changed by programming bit 3 of the Interrupt Edge/Pin MUX Register (xxDFH).

$\overline{\text{MWR}}$. *Memory Write (input/output, active Low, tristate)*. $\overline{\text{MWR}}$ is active when both the internal $\overline{\text{MREQ}}$ and MR are active. This $\overline{\text{RTSA}}$ or PC2 combination is pin multiplexed with $\overline{\text{MWR}}$ on the $\overline{\text{MWR}}$/PC2/$\overline{\text{RTSA}}$ pin. The default function of this pin on power up is $\overline{\text{MWR}}$, which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

$\overline{\text{WAIT}}$. *(input/output active Low)*. $\overline{\text{WAIT}}$ indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The $\overline{\text{WAIT}}$ input is sampled on the failing edge of T2 (and subsequent wait states). If the input is sampled Low, then additional wait

states are inserted until the $\overline{\text{WAIT}}$ input is sampled High, at which time execution continues.

$\overline{\text{HALT}}$. *Halt/Sleep Status (input/output, active Low)*. This output is asserted after the CPU has executed either the HALT or SLEEP instruction, and is waiting for either nonmaskable or maskable interrupts before operation can resume. It is also used with the $\overline{\text{M1}}$ and ST signals to decode status of the CPU machine cycle. On exit of HALT/SLEEP mode, the first instruction fetch can be delayed by 16 clock cycles after the $\overline{\text{HALT}}$ pin goes High, if HALT 16 feature is selected.

$\overline{\text{BUSACK}}$. *Bus Acknowledge (input/output, active Low)*. $\overline{\text{BUSACK}}$ indicates to the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

$\overline{\text{BUSREQ}}$. *Bus Request (input, active Low)*. This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions and places the address/data buses and other control signals, into the high impedance state.

$\overline{\text{NMI}}$. *Non-maskable interrupt (input, negative edge triggered)*. /NM1 has a higher priority than $\overline{\text{INT}}$ and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location `0066H`.

$\overline{\text{INT0}}$. *Maskable Interrupt Request 0 (input/output active Low)*. This signal is generated by external I/O devices. The CPU honors this request at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$ and $\overline{\text{BUSREQ}}$ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ signals become active. The internal Z180 MPU's $\overline{\text{INTO}}$ source is: $\overline{\text{INTO}}$ or ESCC or the MIMIC. This input is level triggered. $\overline{\text{INTO}}$ is an open-drain output, so you can connect other open-drain interrupts onto the circuit in addition to having a pull-up to V_{CC}.

$\overline{\text{INT}}$, $\overline{\text{INT2}}$. *Maskable Interrupt Requests 1 and 2 (inputs, active Low)*. This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$, $\overline{\text{BUSREQ}}$, and $\overline{\text{INTO}}$ signals are inactive. The CPU acknowledges these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgment for $\overline{\text{INTO}}$, during this cycle neither the $\overline{\text{M1}}$ or $\overline{\text{IORQ}}$ signals become active. These pins may be programmed to provide an active Low level on rising or falling edge interrupts. The level of the external $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ pins may be read through bits PC6 and PC7 of parallel Port C. Pin $\overline{\text{INT1}}$/PC6 multiplexes $\overline{\text{INT1}}$ and PC6. Pin $\overline{\text{INT2}}$/PC7 multiplexes $\overline{\text{INT2}}$ and PC7.

$\overline{\text{RFSH}}$. *Refresh (input/output, active Low, tristate)*. Together with $\overline{\text{MREQ}}$, $\overline{\text{RFSH}}$ indicates that the current CPU machine cycle and the contents of the address bus are used for refresh of dynamic memories. The low order 8 bits of the address bus (A7-A0) contain the refresh address. This signal is analogous to the $\overline{\text{REF}}$ signal of the Z64180.

Z180™ MPU UART and SIO Signals

CKA0, CKA1. *Asynchronous Clocks 0 and 1 (bi-directional, active High)*. These pins are the transmit and receive clocks for the synchronous channels. CKA0 is multiplexed with $\overline{\text{DREQ0}}$ on the CKA0/$\overline{\text{DREQ0}}$ pin. CKA1 is multiplexed with $\overline{\text{TEND0}}$ on the CKA1/$\overline{\text{TEND0}}$ pin.

CKS. *Serial Clock (bi-directional, active High)*. This line is clock for the CSIO channel and is multiplexed with the ESCC signal ($\overline{\text{W}}$/$\overline{\text{REQB}}$) and the 16550 MIMIC interface signal $\overline{\text{HTxRDY}}$ on the CKS/$\overline{\text{W}}$/$\overline{\text{REQB}}$/ $\overline{\text{HTxRDY}}$ pin.

$\overline{\text{DCD0}}$. *Data Carrier Detect 0 (input, active Low)*. This is a programmable modem control signal for ASCI channel 0. $\overline{\text{DCD0}}$ is multiplexed with the PB2 (parallel Port B, bit 2) on the $\overline{\text{DCD0}}$/PB2 pin.

$\overline{\text{RTS0}}$. *Request to Send 0 (output, active Low)*. This is a programmable modem control signal for ASCI channel 0. This pin is multiplexed with PB0 (parallel Port B, bit 0) on the $\overline{\text{RTS0}}$/PB0 pin.

$\overline{\text{CTS0}}$. *Clear to Send 0 (input, active Low)*. This line is a modem control signal for the ASCI channel 0. This pin is multiplexed with PB1 (parallel Port B, bit 1) on the /CTS0/PB1 pin.

TxA0. *Transmit Data 0 (output, active High)*. This signal is the transmitted data from the ASCI channel 0. This pin is multiplexed with PB3 (parallel Port B, bit 3) on the TxA0/ PB3 pin.

TxS. *Clocked Serial Transmit Data (output, active High)*. This line is the transmitted data from the CSIO channel. TxS is multiplexed with the ESCC signal ($\overline{\text{DTRREQB}}$) and the 16550 MIMIC interface signal HINTR on the TxS/$\overline{\text{DTR}}$/$\overline{\text{REQB}}$/$\overline{\text{HINTR}}$ pin.

RxA0. *Receive Data 0 (input, active High)*. This signal is the receive data to ASCI channel 0. This pin is multiplexed with PB4 (parallel Port B, bit 4) on the RxA0/PB4.

RxS. *Clocked Serial Receive Data (input, active High)*. This line is the receive data for the CSIO channel. RxS is multiplexed with the $\overline{\text{CTS1}}$ signal for ASCI channel 1 and with PB7 (parallel Port B, bit 7) on the RxS/$\overline{\text{CTS1}}$/PB7 pin.

RxA1. *Received Data ASCI channel 1 (input, active High)*. This pin is multiplexed with PB6 (parallel Port B, bit 6) on the RxA1/PB6 pin.

TxA1. *Transmitted Data ASCI Channel 1 (output, active High)*. This pin is multiplexed with PB5 (parallel Port B, bit 5) on the TxA1/PB5 pin.

Z180 MPU DMA Signals

$\overline{\text{TEND0}}$. *Transfer End 0 (output, active Low)*. This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{\text{TEND0}}$ is multiplexed with CKA1 on the CKA1/$\overline{\text{TEND0}}$ pin.

$\overline{\text{TEND1}}$. *Transfer End 1 (output, active Low)*. This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{\text{TEND1}}$ is multiplexed with the ESCC signal $\overline{\text{RTSB}}$ and the 16550 MIMIC interface signal $\overline{\text{HRxRDY}}$ on the $\overline{\text{TEND1}}$/$\overline{\text{RTSB}}$/$\overline{\text{HRxRDY}}$ pin.

$\overline{\text{DREQ0}}$. *DMA request 0 (input, active Low)*. $\overline{\text{DREQ0}}$ is used to request a DMA transfer from DMA channel 0. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed. $\overline{\text{DREQ0}}$ is multiplexed with CKA0 on the CKA0/$\overline{\text{DREQ0}}$ pin.

$\overline{\text{DREQ1}}$. *DMA request 1 (input, active Low)*. $\overline{\text{DREQ1}}$ is used to request a DMA transfer from DMA channel 1. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed.

Z180™ MPU Timer Signals

T_{OUT}. *Timer Out (output, active High)*. T_{OUT} is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus on the A18/T_{OUT} pin.

Z85230 ESCC™ Signals

TxDA. *Transmit Data (output, active High)*. This output signal transmits channel A's serial data at standard TTL levels. This output can be tristated during power down modes.

TxDB. *Transmit Data (output, active High)*. This output signal transmits channel B's serial data at standard TTL levels. In Z80182/ZSL182 mode 1, TxDB is multiplexed with the 16550 MIMIC interface $\overline{\text{HDDIS}}$ signal on the TxDB/$\overline{\text{HDDIS}}$ pin.

RxDA. *Receive Data (inputs, active High)*. These inputs receive channel A's serial data at standard TTL levels.

RxDB. *Receive Data (input, active High)*. These inputs receive channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1 RxDB is multiplexed with the 16550 MIMIC HA1 input on the RxDB/HA1 pin.

$\overline{\text{TRxCA}}$. *Transmit/Receive Clock (input or output, active Low)*. The functions of this pin are under channel A program control. $\overline{\text{TRxCA}}$ may supply the receive clock or the transmit clock in the Input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

$\overline{\text{TRxCB}}$. Transmit/Receive Clock (input or output, active Low). The functions of this pin are under channel B program control. $\overline{\text{TRxCB}}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop (DPLL), the crystal oscillator, the baud rate generator, or the transmit clock in output mode. In Z80182/Z8L182 mode 1 $\overline{\text{TRxCB}}$ is multiplexed with the 16550 MIMIC interface HA0 input on the $\overline{\text{TRxCB}}$/HA0 pin.

$\overline{\text{RTxCA}}$. *ReceivelTransmit Clock (input, active Low)*. The functions of this pin are under channel A program control. In channel A, $\overline{\text{RTxCA}}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the $\overline{\text{SYNCA}}$ pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode.

$\overline{\text{RTxCB}}$. *ReceivelTransmit Clock (input, active Low)*. The functions of this pin are under channel B program control. In channel B, $\overline{\text{RTxCB}}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the $\overline{\text{SYNCB}}$ pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode. In Z80182/Z8L182 mode 1 the $\overline{\text{RTxCB}}$ signal is multiplexed with 16550 MIMIC interface HA2 input on the $\overline{\text{RTxCB}}$/HA2 pin.

$\overline{\text{SYNCA}}$, **$\overline{\text{SYNCB}}$**. *Synchronization (inputs/outputs, active Low)*. These pins can act as either inputs, outputs, or as part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$. In this mode, transitions on these lines affect the state of the Sync /Hunt status bits in Read Register 0, but have no other function. $\overline{\text{SYNCA}}$ is also multiplexed with PC4 (parallel Port C, bit 4) on the $\overline{\text{SYNCA}}$/PC4 pin.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode $\overline{\text{SYNC}}$ must be driven Low two receive clock cycles after the last bit in the sync character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{\text{SYNC}}$.

In the Internal Synchronization mode, (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync character is recognized (regardless of the character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag. In Z80182/Z8L182 mode 1 the $\overline{\text{SYNCB}}$ signal is multiplexed with the 16550 MIMIC interface $\overline{\text{HCS}}$ input on the $\overline{\text{SYNCB}}$/$\overline{\text{HCS}}$ pin.

$\overline{\text{CTSA}}$. *Clear To Send (input, active Low)*. If this pin is programmed as auto enable, a Low on this input enables the channel A transmitter. If not programmed as auto enable, it may be used as a general-purpose input. The input is Schmitt-trigger buffered to accommodate slow rise-time input. The ESCC detects transitions on this input and can interrupt the Z180' MPU on either logic level transitions. $\overline{\text{CTSA}}$ is multiplexed with PC1 (parallel Port C, bit 1) on the $\overline{\text{CTSA}}$/PC1 pin.

$\overline{\text{CTSB}}$. *Clear To Send (input, active Low)*. This pin is similar to $\overline{\text{CTSA}}$'s functionality but is applicable to the channel B transmitter. In Z80182/Z8L182 mode, the $\overline{\text{CTSB}}$ signal is multiplexed with the 16550 MIMIC interface $\overline{\text{HWR}}$ input on the $\overline{\text{CTSB}}$/$\overline{\text{HWR}}$ pin.

$\overline{\text{DCDA}}$. *Data Carrier Detect (input, active Low)*. This pin functions as receiver enables if it is programmed as an auto enable bit; otherwise, it may be used as a general-purpose input pin. The pin is Schmitt-trigger buffered to accommodate slow rise-time signals. The ESCC detects transitions on this pin and can interrupt the Z180 MPU on either logic level transitions. $\overline{\text{DCDA}}$ is also multiplexed with PC0 (parallel Port C, bit 0) on the $\overline{\text{DCDA}}$/PC0 pin.

$\overline{\text{DCDB}}$. *Data Carrier Detect (input, active Low)*. This pin's functionality is similar to $\overline{\text{DCDA}}$ but applicable to the channel B receiver. In Z80182/Z8L182 mode 1, $\overline{\text{DCDB}}$ is multiplexed with the 16550 MIMIC interface $\overline{\text{HRD}}$ input on the $\overline{\text{DCDB}}$/$\overline{\text{HRD}}$ pin.

$\overline{\text{RTSA}}$. *Request to Send (output, active Low)*. When the Request to Send (RTS) bit in Write Register 5 channel A is set, the $\overline{\text{RTSA}}$ signal goes Low. When the RTS bit is reset in the Asynchronous mode and auto enables is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with auto enables off, the $\overline{\text{RTSA}}$ pin strictly follows the state of the RTS bit. The pin can be used as general-purpose output. ($\overline{\text{RTSA}}$ is multiplexed with PC2 (parallel Port C bit 2). This $\overline{\text{RTSA}}$ or PC2 combination is pin multiplexed with $\overline{\text{MWR}}$ (active when both the internal $\overline{\text{MREQ}}$ and $\overline{\text{WR}}$ are active) on the $\overline{\text{MWR}}$/PC2/$\overline{\text{RTSA}}$ pin. The default function of this pin on power-up is $\overline{\text{MWR}}$ which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

$\overline{\text{RTSB}}$. *Request to Send (output, active Low)*. This pin is similar in functionality as $\overline{\text{RTSA}}$ but is applicable on channel B. The $\overline{\text{RTSB}}$ signal is multiplexed with the Z180 MPU $\overline{\text{TEND1}}$ signal and the 16550 MIMIC interface $\overline{\text{HRxRDY}}$ signal on the $\overline{\text{TEND1}}$/$\overline{\text{RTSB}}$/$\overline{\text{HRxRDY}}$ pin.

$\overline{\text{DTR}}$/$\overline{\text{REQA}}$. *Data Terminal Ready (output, active Low)*. This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. $\overline{\text{DTR}}$/$\overline{\text{REQA}}$ is

also multiplexed with PC3 (parallel Port C, bit 3) on the $\overline{\text{DTR}}/\overline{\text{REQA}}$/PC3 pin.

$\overline{\text{DTR}}/\overline{\text{REQB}}$. *Data Terminal Ready (output, active Low)*. This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. The $\overline{\text{DTR}}/\overline{\text{REQB}}$ signal is multiplexed with the Z180 MPU TxS signal and the 16550 MIMIC interface HINTR signal on the $\overline{\text{TxS}}/\overline{\text{DTR}}/\overline{\text{REQB}}/\overline{\text{HINTR}}$ pin.

$\overline{\text{W}}/\overline{\text{REQA}}$. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function)*. This dual-purpose output can be programmed as Request (receive) lines for a DMA controller or as Wait lines to synchronize the Z180 MPU to the ESCC data rate. The reset state is Wait. The ESCC allows full duplex DMA transfers. $\overline{\text{W}}/\overline{\text{REQA}}$ is also multiplexed with PC5 (parallel Port C, bit 5) on the $\overline{\text{W}}/\overline{\text{REQA}}$/PC5 pin.

$\overline{\text{W}}/\overline{\text{REQB}}$. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function)*. This pin is similar in functionality to $\overline{\text{W}}/\overline{\text{REQA}}$ but is applicable on channel B. The $\overline{\text{W}}/\overline{\text{REQB}}$ signal is multiplexed with the Z180 MPU CKS signal and the 16550 MIMIC interface $\overline{\text{HTxRDY}}$ signal on the CKS/$\overline{\text{W}}/\overline{\text{REQB}}/\overline{\text{HTxRDY}}$ pin.

16550 MIMIC Interface Signals

HD7-HD0. *Host Data Bus (input/output, tristate)*. In Z80182/Z8L182 mode 1, the host data bus is used to communicate between the 16550 MIMIC interface and the PC/XT/AT. It is multiplexed with the PA7-PA0 of parallel Port A when the Z80182/Z8L182 is in mode 0.

$\overline{\text{HDDIS}}$. *Host Driver Disable (output, active Low)*. In Z80182/Z8L182 mode 1, this signal goes Low whenever the PC/XT/AT is reading data from the 16550 MIMIC interface. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC™ TxDB signal on the TxDB/$\overline{\text{HDDIS}}$ pin.

HA2-HA0. *Host Address (input)*. In Z80182/Z8L182 mode 1, these pins are the address inputs to the 16550 MIMIC interface. This address determines which register the PC/XT/AT accesses. HA0 is multiplexed with $\overline{\text{TRxCB}}$ on the $\overline{\text{TRxCB}}$/HA0 pin; HA1 is multiplexed with RxDB on the RxDB/HA1 pin; HA2 is multiplexed with $\overline{\text{RTxCB}}$ on the $\overline{\text{RTxCB}}$/HA2 pin.

$\overline{\text{HCS}}$. *Host Chip Select (input, active Low)*. In Z80182/ Z8L182 mode 1, this input is used by the PC/XT/AT to select the 16550 MIMIC interface for an access. In Z80182/ Z8L182 mode 0, it is multiplexed with the ESCC $\overline{\text{SYNCB}}$ signal on the SYNCB/$\overline{\text{HCS}}$ pin.

$\overline{\text{HWR}}$. *Host Write (Input, active Low)*. In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a write operation is taking place. In Z80182/Z8L182 mode 0, this input is multiplexed with the ESCC $\overline{\text{CTSB}}$ signal on the $\overline{\text{CTSB}}$/$\overline{\text{HWR}}$ pin.

$\overline{\text{HRD}}$. *Host Read (input, active Low)*. In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a read operation is taking place. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC $\overline{\text{DCDB}}$ signal on the $\overline{\text{DCDB}}$/$\overline{\text{HRD}}$ pin.

HINTR. *Host Interrupt (output, active High)*. In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface to signal the PC/XT/AT that an interrupt is pending. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC ($\overline{\text{DTR}}$/$\overline{\text{REQB}}$) signal and the Z180 MPU TxS signal on the TxS/$\overline{\text{DTR}}$/$\overline{\text{REQB}}$/$\overline{\text{HINTR}}$ pin.

$\overline{\text{HTxRDY}}$. *Host Transmit Ready (output, active Low)*. In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. In Z80182/ Z8L182 mode 0, this pin is multiplexed with the ESCC ($\overline{\text{W}}$/$\overline{\text{REQB}}$) signal and the Z180 MPU CKS signal on the CKS/$\overline{\text{W}}$/$\overline{\text{REQB}}$/$\overline{\text{HTxRDY}}$ pin.

$\overline{\text{HRxRDY}}$. *Host Receive Ready (output, active Low)*. In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface in DMA mode to signal the PC/XT/AT that a data byte is ready in the Receive Buffer. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC $\overline{\text{RTSB}}$

signal and the Z180 MPU $\overline{\text{TEND1}}$ signal on the $\overline{\text{TEND1}}$/$\overline{\text{RTSB}}$ $\overline{\text{HRxRDY}}$ pin.

Parallel Ports

PA7-PA0. *Parallel Port A (input/output)*. These lines can be configured as inputs or outputs on a bit-by-bit basis when the Z80182/Z8L182 is operated in mode 0. These pins are multiplexed with the HD7-HD0 when the Z80182/ Z8L182 is in mode 1.

PB7-PB0. *Parallel Port B (input/output)*. These lines can be configured as inputs or outputs on a bit-by-bit basis when the Port function is selected in the System Configuration register. The pins are multiplexed with the following 2180 peripheral functions: $\overline{\text{RTS0}}$, $\overline{\text{CTS0}}$, $\overline{\text{DCD0}}$, TXA0, RxA0, TxA1, RxA1, (RxS/$\overline{\text{CTS1}}$).

PC7-PC0. *Parallel Port C (input/output)*. These lines can be configured as inputs or outputs on a bit-by-bit basis for bits PC5-PC0. Bits PC7 and PC6 are input only and read the level of the external $\overline{\text{INT2}}$ and $\overline{\text{INT1}}$ pins. When $\overline{\text{INT2}}$ and/or $\overline{\text{INT1}}$ are in edge capture mode, writing a 1 to the respective PC7, PC6 bit clears the interrupt capture latch; writing a 0 has no effect. Bits PC5-PC0 are multiplexed with the following pins from ESCC channel A: ($\overline{\text{W}}$/$\overline{\text{REQA}}$), $\overline{\text{SYNCA}}$, ($\overline{\text{DTR}}$/$\overline{\text{REQA}}$), $\overline{\text{RTSA}}$, $\overline{\text{MWR}}$, $\overline{\text{CTSA}}$, $\overline{\text{DCDA}}$. The Port function is selected through a bit in the System Configuration Register.

EMULATION SIGNALS

EV1, EV2: Emulation Select (input). These two pins determine the emulation mode of the Z180 MPU (Table 2).

Table 2. Evaluation Modes

Mode	EV2	EV1	Description
0	0	0	Normal mode, on-chip Z180 bus master
1	0	1	Emulation Adapter Mode
2	1	0	Emulator Probe Mode
3	1	1	Reserved for Test

System Control Signals

ST. *Status (output, active High)*. This signal is used with the $\overline{M1}$ and $\overline{HALT}$ output to decode the status of the CPU machine cycle. If unused, this pin is pulled to V_{DD}.

$\overline{RESET}$. *Reset Signal (input, active Low)*. $\overline{RESET}$ signal is used for initializing the MPU and other devices in the system. It must be kept in the active state for a period of at least three system clock cycles.

IEI. *Interrupt Enable Signal (input, active High)*. IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.

IEO. *Interrupt Enable Output Signal (output, active High)*. In the daisy-chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is 1 and the CPU is not servicing an interrupt from the on-chip peripherals. This pin is multiplexed with $\overline{IOCS}$ on the $\overline{IOCS}$/IEO pin. The $\overline{IOCS}$ function is the default on Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

$\overline{IOCS}$. *Auxiliary Chip Select Output Signal (output, active Low)*. This pin is multiplexed with /IEO on the $\overline{IOCS}$/IEO pin. $\overline{IOCS}$ is an auxiliary chip select that decodes A7, A6, $\overline{IORQ}$, $\overline{M1}$ and effectively decodes the address space xx80H to xxBFH for I/O transactions. A15 through A8 are

not decoded so that the chip select is active in all pages of I/O address space. The $\overline{\text{IOCS}}$ function is the default on the $\overline{\text{IOCS}}$/IEO pin after Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

$\overline{\text{RAMCS}}$. *RAM Chip Select (output, active Low)*. Signal used to access RAM based upon the Address and the RAMLBR and RAMUBR registers and $\overline{\text{MREQ}}$.

$\overline{\text{ROMCS}}$. *ROM Chip Select (output, active Low)*. Signal used to access ROM based upon the address and the ROMBR register and $\overline{\text{MREQ}}$.

E. *Enable Clock (output, active High)*. Synchronous machine cycle clock output during bus transactions.

XTAL. *Crystal (input, active High)*. Crystal oscillator connection. This pin must be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics).

EXTAL. *External Clock/Crystal (input, active High)*. Crystal oscillator connections to an external clock can be input to the Z80180 on this pin when a crystal is not used. This input is Schmitt triggered.

PHI. *System Clock (output, active High)*. The output is used as a reference clock for the MPU and the external system. The frequency of this output is reflective of the functional speed of the processor. In clock divide-by-two mode, the pHI frequency is half that of the crystal or input clock. If divide-by-one mode is enabled, the PHI frequency is equivalent to that of crystal or input frequency. The PHI frequency is also fed to the ESCC core. If running over 20 MHz (5V) or 10 MHz (3V) the PHI-ESCC frequency divider must be enabled to divide the PHI clock by two prior to feeding into the ESCC core.

Multiplexed Pin Descriptions

A18/TOUT. During Reset, this pin is initialized as an A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, the

T_{OUT} function is selected. If TOC1 and TOC0 bits are cleared to 0, the A18 function is selected.

In normal user mode (on-chip bus master), the A18 signal for the chip select logic is obtained from the CPU before the external pin is muxed as A18/T_{OUT}. Therefore, the selection of T_{OUT} does not affect the operation of the 182 chip select logic. However, in adapter mode (off-chip bus master), the A18 signal MUST be provided by the external bus master.

CKA0/$\overline{\text{DREQ0}}$. During Reset, this pin is initialized as CKA0 pin. If either DM1 or SM1 in the DMA Mode Register (DMODE) is set to 1, $\overline{\text{DREQ0}}$ function is always selected.

CKA1/$\overline{\text{TEND0}}$. During Reset, this pin is initialized as CKA1 pin. If CKA1 D bit in the ASCI control register Ch1(CNTLA1) is set to 1, $\overline{\text{TEND0}}$ function is selected. If CKA1 D bit is set to 0, CKA1 function is selected.

RxS/$\overline{\text{CTS1}}$. During Reset, this pin is initialized as the RxS pin. If CTS1E bit in the ASCI status register Ch1 (STAT1) is set to 1, $\overline{\text{CTS1}}$ function is selected. If CTS1E bit is set to 0, RxS function is selected. This pin is also multiplexed with PB7 based on bit 6 in the System Configuration Register.

The pins below in Table 3 are triple-multiplexed based upon the values of bit 1 and bit 2 of the System Configuration Register. The pins are configured as Table 3 specifies. On Reset, both bits 1 and 2 are 0, so $\overline{\text{TEND1}}$,TxS, CKS are selected.

Table 3. Triple Multiplexed Pins

Bit 1	Bit 2	Master Configuration Register
0	0	$\overline{\text{TEND1}}$,TxS,CKS
0	1	$\overline{\text{RTSB}}$,$\overline{\text{DTR}}$/$\overline{\text{REQB}}$,$\overline{\text{W}}$/$\overline{\text{REQB}}$
1	0	$\overline{\text{TEND1}}$,TxS,CKS
1	1	$\overline{\text{HRxRDY}}$,$\overline{\text{HTxRDY}}$,HINTR

The pins below are multiplexed based upon the value of bit 1 of the System Configuration register. If bit 1 is 0, then the Z80182/Z8L182 Mode 0 (non-16550 MIMIC mode) signals are selected; if bit 1 is 1, then Z80182/Z8L182 Mode 1 (16550 MIMIC mode) signals are selected. On Reset, Z80182/Z8L182 Mode 0 is always selected as shown in Table 4.

Table 4. Mode 0 and Mode 1 Multiplexed Pins

Z80182/Z8L182 Mode 0	Z80182/Z8L182 Mode 1
TxDB	HDDIS
RxDB	HA1
TRxCB	HA0
RTxCB	HA2
SYNCB	HCS
CTSB	HWR
DCDB	HRD
PA7-PA0	HD7-HD0

Ports B and C Multiplexed Pin Descriptions

Ports B and C are pin multiplexed with the Z180 ASCI functions and part of ESCC channel A. The MUX function is controlled by bits 7-5 in the System Configuration Register. The MUX is organized as shown in Table 5.

Table 5. Multiplexed Port Pins

Port Mode Function	ASCI/ESCC Mode Function
PB7	RxS,$\overline{CTS1}$
PB6 Select with bit 6 = 1	RxA1
PB5 System Config Reg.	TxA1
PB4	RxA0
PB3	TxA0
PB2 Select with bit 5 = 1	DCD0
PB1 System Config Reg.	$\overline{CTS0}$[1]
PB0	RTS0
PC7	Always Reads $\overline{INT2}$ Ext. Status
PC6	Always Reads $\overline{INT1}$ Ext. Status
PC5	$\overline{W}/\overline{REQA}$
PC4	SYNCA
PC3 Select with bit 7 = 1	$\overline{DTR}/\overline{REQA}$
PC2 System Config Reg.	$\overline{RTSA}$[2]
PC1	CTSA
PC0	DCDA

NOTES:
1. When the Port function (PB1) is selected, the internal Z180$\overline{CTS0}$ is always driven Low. This ensures that the ASCI channel 0 of the Z180™ MPU is enabled to transmit data.
2. Interrupt Edge/Pin MUX register, bit 3 chooses between the $\overline{MWR}$ or PC2/$\overline{RTSA}$ combination; the System Configuration Register bit 7 chooses between PC2 and $\overline{RTSA}$.

Refer to Table 6 for the 1st, 2nd and 3rd pin functions.

Table 6. Primary, Secondary and Tertiary Pin Functions

Pin Number					
VQFP	QFP	1st Function	2nd Function	3rd Function	MUX Control
1	4	ST			
2	5	A0			
3	6	A1			
4	7	A2			
5	8	A3			
6	9	A4			
7	10	A5			
8	11	A6			
9	12	A7			
10	13	A8			
11	14	A9			
12	15	A10			
13	16	All			
14	17	A12			
15	18	V_{SS}			
16	19	A13			
17	20	A14			
18	21	A15			
19	22	A16			
20	23	A17			
21	24	A18/T_{OUT}			
22	25	V_{DD}			
23	26	A19			
24	27	D0			
25	28	D1			
26	29	D2			
27	30	D3			

Table 6. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number					
VQFP	QFP	1st Function	2nd Function	3rd Function	MUX Control
28	31	D4			
29	32	D5			
30	33	D6			
31	34	D7			
32	35	RTS0	PB0		SYS CONF REG Bit 5
33	36	CTS0	PB1		SYS CONF REG Bit 5
34	37	DCD0	PB2		SYS CONF REG Bit 5
35	38	TxA0	PB3		SYS CONF REG Bit 5
36	39	RxA0	PB4		SYS CONF REG Bit 5
37	40	TxA1	PB5		SYS CONF REG Bit 6
38	41	RxA1	PB6		SYS CONF REG Bit 6
39	42	Rx/$\overline{\text{CTS1}}$	PB7		SYS CONF REG Bit 6
40	43	CKA0/ $\overline{\text{DREQ0}}$			
41	44	V_{SS}			
42	45	CKA1/ $\overline{\text{TEND0}}$			
43	46	TXS	$\overline{\text{DTR}}$/$\overline{\text{REQB}}$	HINTR	SYS CONF REG Bit 1,2
44	47	CKS	$\overline{\text{W}}$/$\overline{\text{REQB}}$	HTxRDY	SYS CONF REG Bit 1,2
45	48	DREQ1			
46	49	V_{DD}			
47	50	TEND1	RTSB	HRxRDY	SYS CONF REG Bit 1,2
48	51	RAMCS			
49	52	ROMCS			
50	53	EV1			
51	54	EV2			

Table 6. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number					
VQFP	QFP	1st Function	2nd Function	3rd Function	MUX Control
52	55	PA0	HD0		SYS CONF REG Bit 1
53	56	PA1	HD1		SYS CONE REG Bit 1
54	57	PA2	HD2		SYS CONF REG Bit 1
55	58	PA3	HD3		SYS CONF REG Bit 1
56	59	PA4	HD4		SYS CONF REG Bit 1
57	60	PA5	HD5		SYS CONF REG Bit 1
58	61	PA6	HD6		SYS CONF REG Bit 1
59	62	PA7	HD7		SYS CONF REG Bit 1
60	63	$\overline{W}/\overline{REQA}$	PC5		SYS CONF REG Bit 7
61	64	$\overline{DTR}/\overline{REQA}$	PC3		SYS CONF REG Bit 7
62	65	MWR	PC2	RTSA	SYS CONF REG Bit 7[2]
63	66	CTSA	PC1		SYS CONF REG Bit 7
64	67	DCDA	PC0		SYS CONF REG Bit 7
65	68	SYNCA	PC4		SYS CONF REG Bit 7
66	69	RTxCA			
67	70	V_{SS}			
68	71	IOCS	IEO		INT EDG/PIN REG Bit 2
69	72	IEI			
70	73	V_{DD}			
71	74	RxDA			
72	75	TRxCA			
73	76	TxDA			
74	77	DCDB	HRD		SYS CONF REG Bit 1
75	78	CTSB	HWR		SYS CONF REG Bit 1
76	79	TxDB	HDDIS		SYS CONF REG Bit 1
77	80	TRxCB	HA0		SYS CONF REG Bit 1
78	81	RxDB	HA1		SYS CONF REG Bit 1

Table 6. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number					
VQFP	QFP	1st Function	2nd Function	3rd Function	MUX Control
79	82	RTxCB	HA2		SYS CONF REG Bit 1
80	83	SYNCB	HCS		SYS CONF REG Bit 1
81	84	HALT			
82	85	RFSH			
83	86	IORQ			
84	87	MRD	MREQ		INT EDG/PIN REG Bit 3
85	88	E			
86	89	M1			
87	90	WR			
88	91	RD			
89	92	PHI			
90	93	V_{SS}			
91	94	XTAL			
92	95	EXTAL			
93	96	WAIT			
94	97	BUSACK			
95	98	BUSREQ			
96	99	RESET			
97	100	NMI			
98	1	INT0			
99	2	INT1	PC6[1]		
100	3	$\overline{INT2}$	PC7[1]		

NOTES:
1. PC7 and PC6 are inputs only and can read values of $\overline{INT1}$ and $\overline{INT2}$.
2. Also controlled by Interrupt Edge/Pin MUX Register.

Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

- Voltage on V_{CC} with respect to V_{SS}
  - -0.3V to +7.0V
- Voltages on all inputs with respect to V_{SS}
  - -0.3V to V_{CC} +0.3V
- Operating Ambient Temperature
  - 0°C to +70°C
- Storage Temperature
  - -55°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0 V). Positive current flows into the referenced pin (Figure 4).

- Available operating temperature range is:
  - S = 0°C to +70°C
- Voltage Supply Range:
  - +4.50V V_{CC} + 5.50V Z80182
  - +3.0 V V_{CC} + 3.60 V 28L182

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for ad- dress and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pF.

Note: The ESCC™ Core is only guaranteed to operate at 20 MHz 5.0V or 10 MHz 3.3V. At reset, the Z182 system clock is "divided by one" before clocking the ESCC. When Z182 operates above 20 MHz 5.0V or 10 MHz 3.3V, program the ESCC to "divide-by-two" mode.

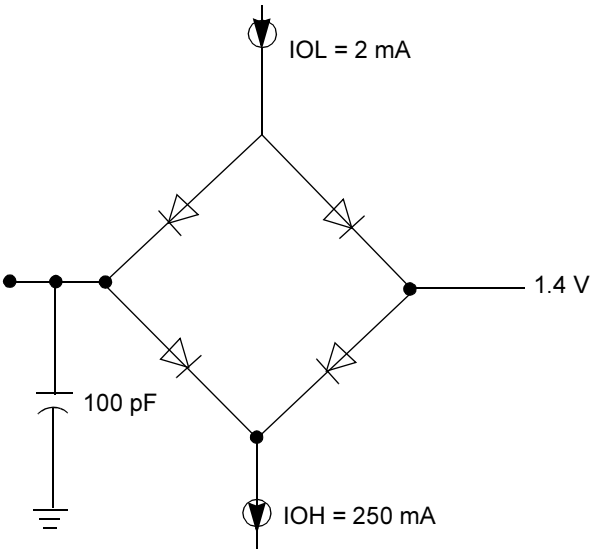


Figure 4. Test Load Diagram

DC Characteristics

Table 7. Z80182/Z8L182 DC Characteristics

(V_{CC} = 5V 10%, V_{SS} = 0V, over specified temperature range unless otherwise noted.)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
VIH1	Input H Voltage	V_{CC} -0.6		V_{CC} +0.3	V	
	$\overline{RESET}$, EXTAL, NMI					
VIH2	Input H Voltage	2.0		V_{CC} +0.3	V	
	Except $\overline{RESET}$, EXTAL, NMI					
VIL1	Input L Voltage	-0.3		0.6	V	
	$\overline{RESET}$, EXTAL, NMI					
VIL2	Input L Voltage	-0.3		0.8	V	
	Except $\overline{RESET}$, EXTAL, NMI					
V0H1	Output H Voltage	2.4			V	I_{OH} = -200 A
	All outputs	V_{CC} -1.2				I_{OH} = -200 A
V0H2	Output H PHI	V_{CC}-0.6			V	I_{OH}= -200 A
VOL1	Output L Voltage	0.40			V	I_{OL} = 2.2 MA
	All outputs					
VOL2	Output L PHI	0.40			V	I_{OL}= 2.2 MA
I_{IL}	Input Leakage	1.0			A	VIN = 0.5 - V_{CC} -0.5
	Current All Inputs					
	Except XTAL, EXTAL					
I_{TL}	tristate Leakage Current			1.0	A	VIN = 0.5 - V_{CC} -0.5
ICC[1]	Power Dissipation[1]	60		120	mA	f = 20 MHz
	(Normal Operation)	100		200	mA	f = 33 MHz
	Power Dissipation[1]	TBD		TBD	mA	f= 20 MHz
	(SLEEP)	TBD		TBD	mA	f= 33 MHz
	Power Dissipation[1]	TBD		TBD	mA	f= 20 MHz
	IDLE Mode	TBD		TBD	mA	f = 20 MHz
		TBD		TBD	mA	f = 33 MHz
	STANDBY Mode	50			A	f = 0 MHz[2]
CP	Pin Capacitance			12	pF	VIN = 0 V, f = 1 MHz
						TA =25 °C

NOTES:

1. These I_{CC} values are preliminary and subject to change without notice.
   V_{IH} Min = V_{CC} -1.0 V, VIL Max = 0.8V (all output terminals are at no load)
   V_{CC} = 5.0 V; (I_{OH} Low EMI) = -50 A, I_{OL} (Low EMI) = 500 A
2. Device may take up to two seconds before stabilizing to steady state standby current.

TIMING DIAGRAMS

Z180 MPU Timing

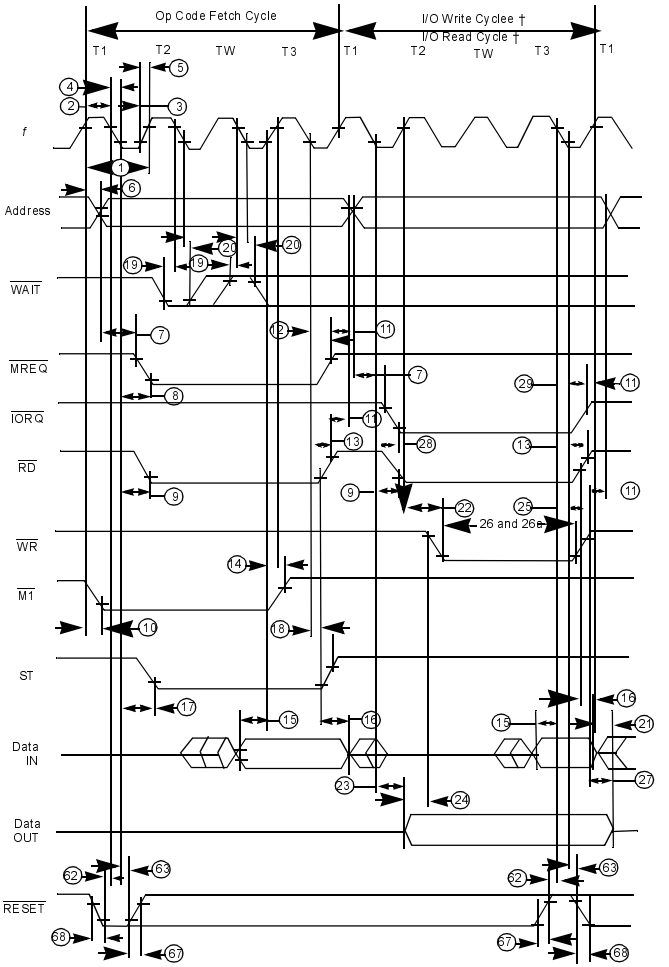


Figure 5. CPU Timing Op Code Fetch Cycle, Memory Read/Write Cycle I/O Read/Write Cycle)

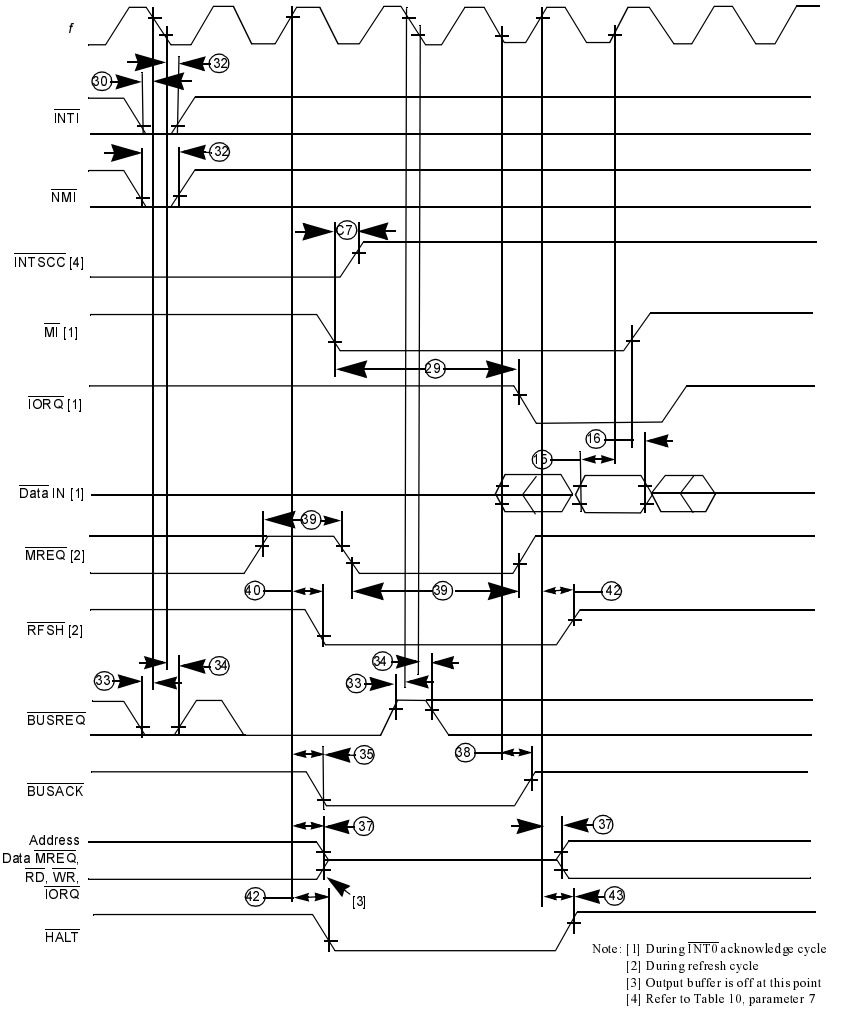


Figure 6. CPU Timing ($\overline{\text{INTO}}$ Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

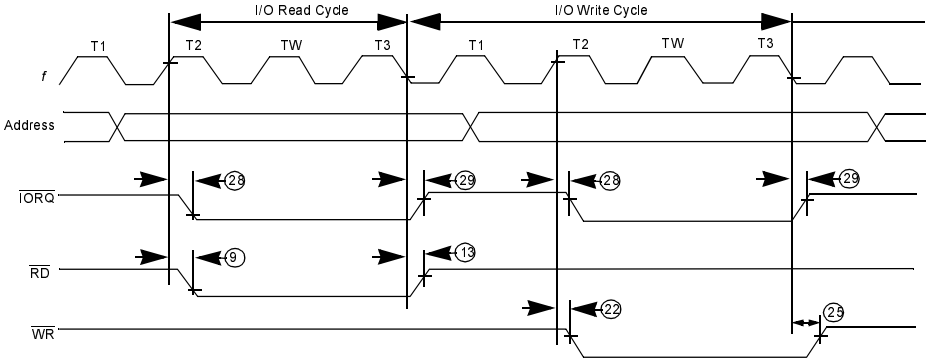
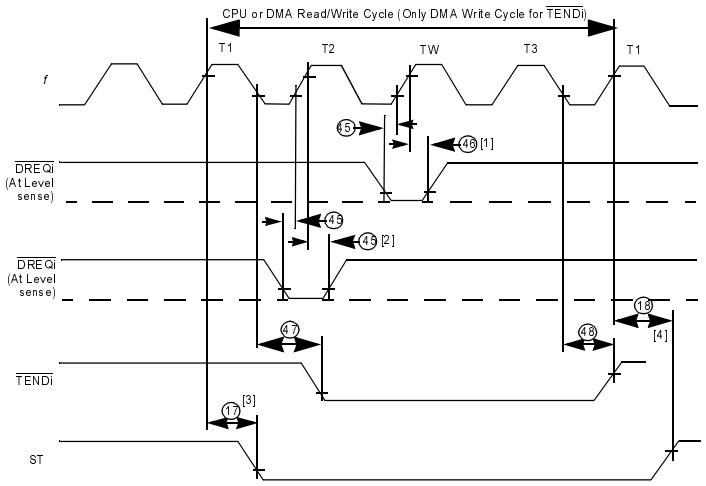


Figure 7. CPU Timing



DMA Control Signals
[1] tDRQS and tDRQH are specified for the rising edge of clock followed by T3.
[2] tDRQS and tDRQH are specified for the rising edge of clock.
[3] DMA cycle starts.
[4] CPU cycle starts.

Figure 8. DMA Control Signals

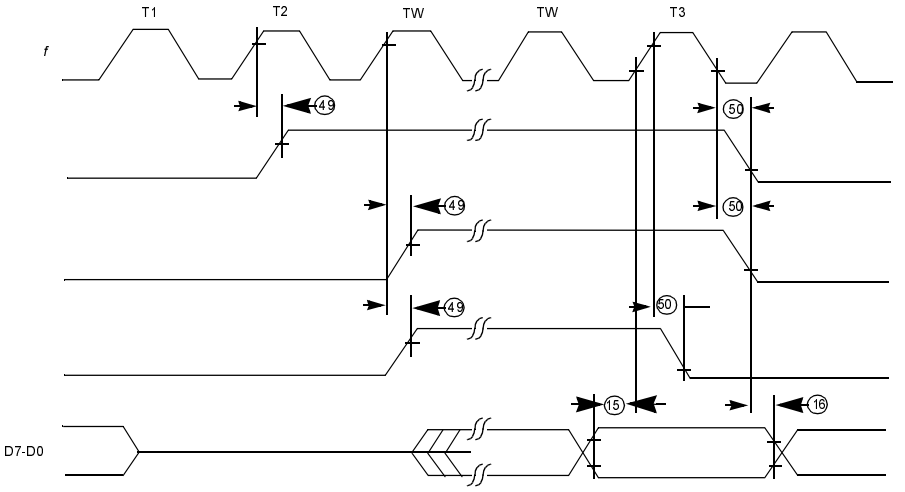


Figure 9. E Clock Timing (Memory Read/Write Cycle I/O Read/Write Cycle)

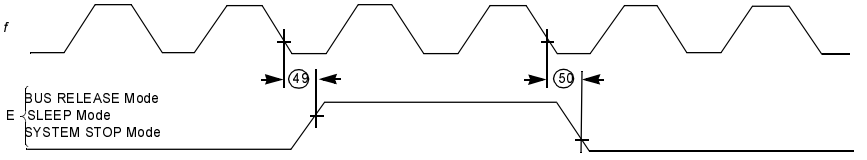


Figure 10. E Clock Timing

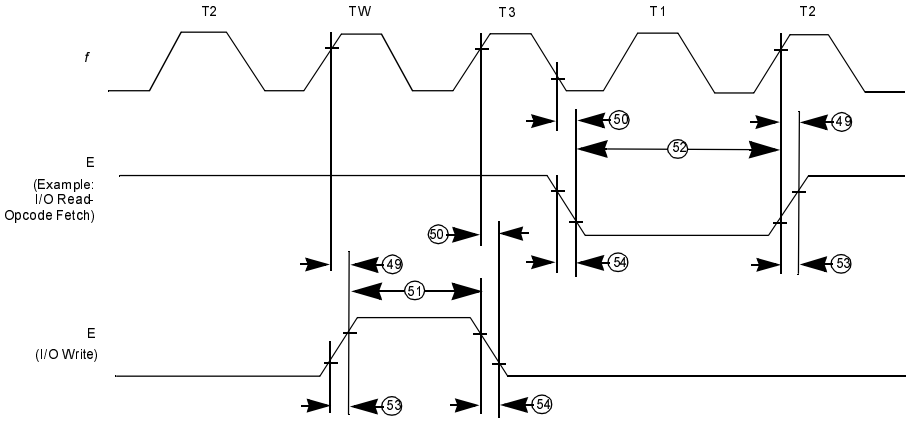


Figure 11. E Clock Timing (Minimum Timing Example of PWEL and PWEH)

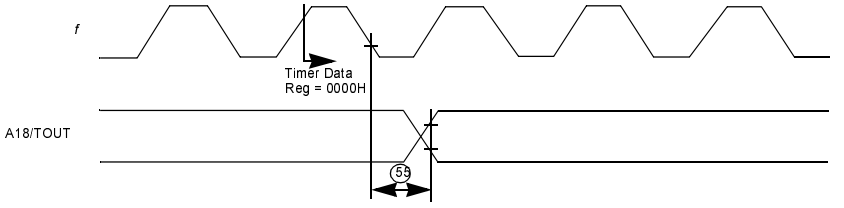


Figure 12. Timer Output Timing

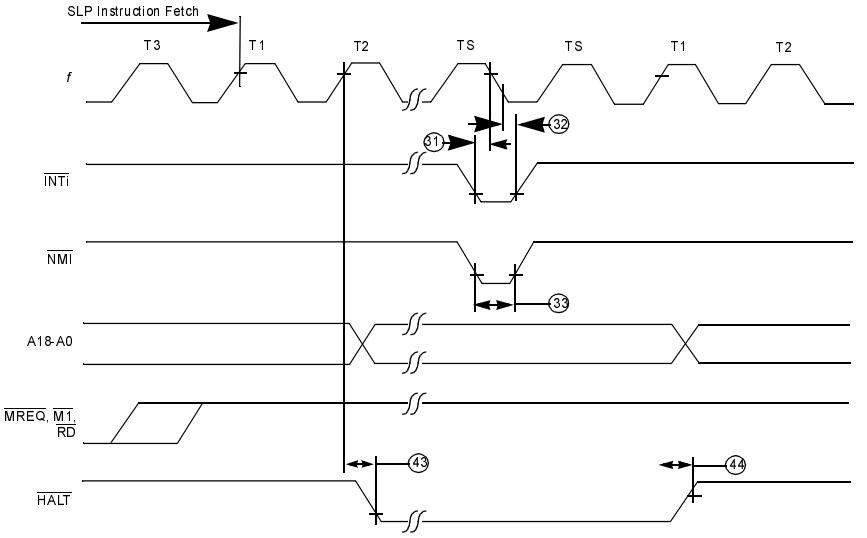


Figure 13. SLEEP Execution Cycle

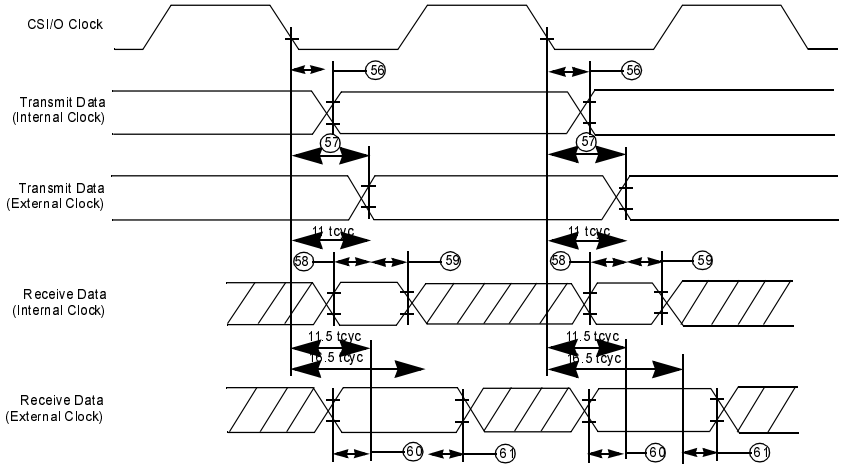


Figure 14. CSI/O Receive/Transmit Timing

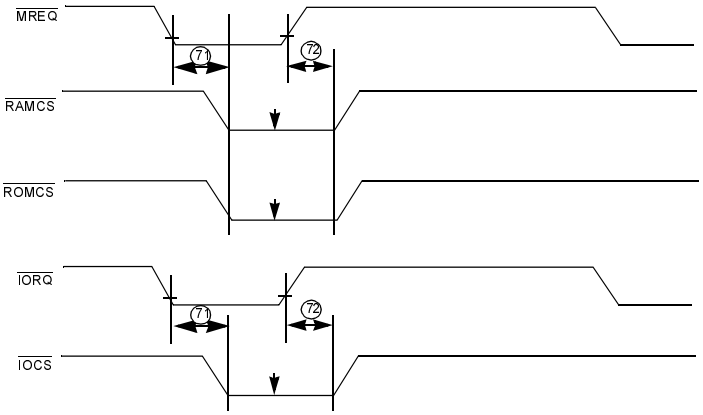


Figure 15. $\overline{\text{ROMCS}}$ and $\overline{\text{RAMCS}}$ Timing

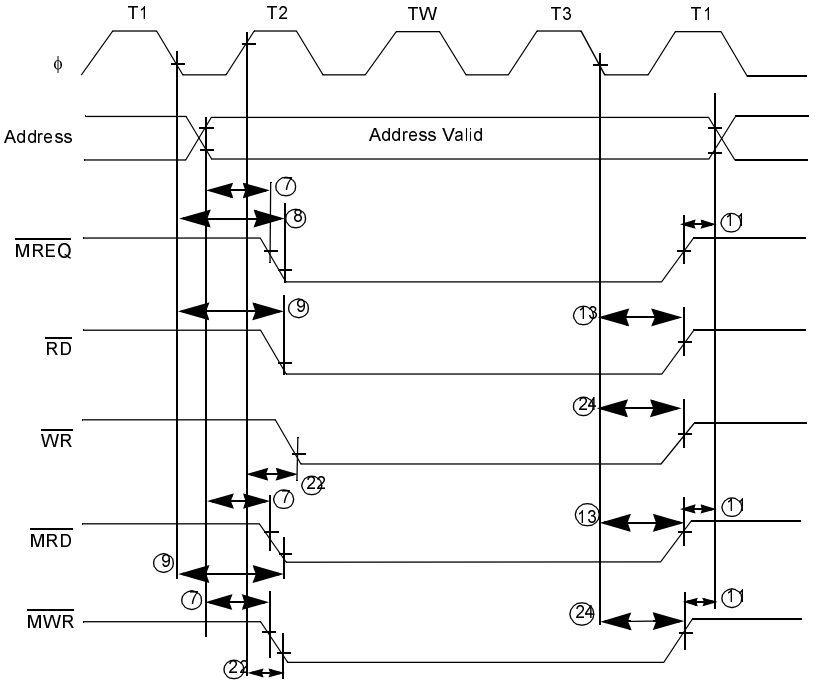


Figure 16. $\overline{\text{MWR}}$ and $\overline{\text{MRD}}$ Timing

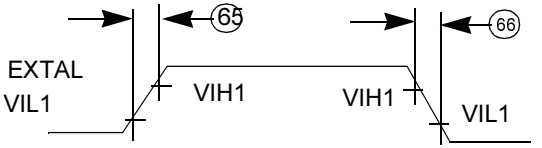


Figure 17. External Clock Rise Time and Fall Time

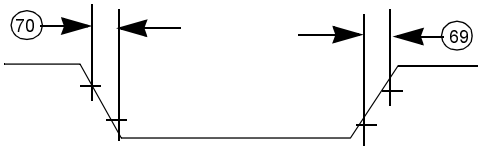


Figure 18. Input Rise and Fail Time (Except EXTAL, RESET

ZSS180 AC CHARACTERISTICS

Table 8. Z8L180 and Z8S180 Timings

			Z8L180 20 MHz		Z80180 33 MHz			
No.	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
1	tcyc	Clock Cycle Time	50	2000	30	2000	ns	Note[1]
2	tCHW	Clock Pulse Width (High)	15		10		ns	Note[1]
3	tCLW	Clock Pulse Width (Low)	15		10		ns	Note[1]
4	tcf	Clock Fall Time		10		5	ns	Note[1]
5	tcr	Clock Rise Time		10		5	ns	Note[1]
6	tAD	Address Valid from Clock Rise		15		15	ns	
7	tAS	Address Valid to $\overline{MREQ}$, $\overline{IORQ}$, $\overline{MRD}$ Fall	5				ns	
8	tMED1	Clock Fall to $\overline{MREQ}$ Fall Delay		15		10	ns	
9	tRDD1	Clock Fall to $\overline{RD}$, $\overline{MRD}$ ($\overline{IOC}$ = 1)		25		15	ns	
		Clock Rise to $\overline{RD}$, $\overline{MRD}$ Fall ($\overline{IOC}$ = 0)		35		15	ns	
10	tMlD1	Clock Rise to $\overline{M1}$ Fall delay		35		15	ns	
11	tAH	Address Hold time ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$,	5		5		ns	
		$\overline{WR}$/$\overline{MRD}$)					ns	
12	tMED2	Clock Fall to $\overline{MREQ}$ Rise Delay		25		15	ns	
13	tRDD2	Clock Fall to $\overline{RD}$, $\overline{MRD}$ Rise Delay		25		15	ns	
14	tM1	D2 Clock Rise to $\overline{M1}$ Rise Delay		40		15	ns	
15	tDRS	Data Read Setup Time	15		15		ns	
16	tDRH	Data Read Hold Time	0		0		ns	
17	tSTD1	Clock Edge to ST Fall		30		15	ns	
18	tSTD2	Clock Edge to ST Rise		30		15	ns	
19	tWS	$\overline{WAIT}$ Setup Time to Clock Fall	15		10		ns	Note[2]
20	tWH	$\overline{WAIT}$ Hold Time from Clock Fall	10		5		ns	
21	tWDZ	Clock Rise to Data Float Delay		35		20	ns	
22	tWRD1	Clock Rise to $\overline{WR}$,$\overline{MWR}$ Fall Delay		25		15	ns	
23	tWDD	Clock Fall to Write Data Delay		25		15	ns	
24	tWDS	Write Data Setup Time to $\overline{WR}$,$\overline{MWR}$ Fall	10		10		ns	
25	tWRD2	Clock Fall to $\overline{WR}$ Rise		25		15	ns	

Table 8. Z8L180 and Z8S180 Timings (Continued)

			Z8L180 20 MHz		Z80180 33 MHz			
No.	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
26	tWRP	$\overline{WR}$ Pulse Width (Memory Write Cycles)	75		45		ns	
26a		$\overline{WR}$ Pulse Width (I/O Write Cycles)	130		70		ns	
27	tWDH	Write Data Hold Time from $\overline{WR}$ Rise	10		5		ns	
28	tIOD1	Clock Fall to $\overline{IORQ}$ Fall Delay ($\overline{IOC}$ = 1)		25		15	ns	
		Clock Rise to $\overline{IORQ}$ Fall Delay ($\overline{IOC}$ = 0)		25		15	ns	
29	tIOD2	Clock Fall $\overline{IORQ}$ Rise Delay		25		15	ns	
30	tIOD3	$\overline{M1}$ Fall to $\overline{IORQ}$ Fall Delay	100		80		ns	
31	tINTS	$\overline{INT}$ Setup Time to Clock Fall	20		15		ns	
32	tINTH	$\overline{INT}$ Hold Time from Clock Fall	10		10		ns	
33	tNMIW	$\overline{NMI}$ Pulse Width	35		25		ns	
34	tBRS	$\overline{BUSREQ}$ Setup Time to Clock Fall	10		10		ns	
35	tBRH	$\overline{BUSREQ}$ Hold Time from Clock Fall	10		10		ns	
36	tBAD1	Clock Rise to $\overline{BUSACK}$ Fall Delay		25		15	ns	
37	tBAD2	Clock Fall to $\overline{BUSACK}$ Rise Delay		25		15	ns	
38	tBZD	Clock Rise to Bus Floating Delay Time		40		30	ns	
39	tMEWH	$\overline{MREQ}$ Pulse Width (High)	35		25		ns	
40	tMEWL	$\overline{MREQ}$ Pulse Width (Low)	35		25		ns	
41	tRFD1	Clock Rise to $\overline{RFSH}$ Fall Delay		20		15	ns	
42	tRFD2	Clock Rise to $\overline{RFSH}$ Rise Delay		20		15	ns	
43	tHAD1	Clock Rise to $\overline{HALT}$ Fall Delay		15		15	ns	
44	tHAD2	Clock Rise to $\overline{HALT}$ Rise Delay		15		15	ns	
45	tDRQS	$\overline{DREQi}$ Setup Time to Clock Rise	20		15		ns	
46	tDRQH	$\overline{DREQi}$ Hold Time from Clock Rise	20		15		ns	
47	tTED1	Clock Fall to $\overline{TENDi}$ Fall Delay		25		15	ns	
48	tTED2	Clock Fall to $\overline{TENDi}$ Rise Delay		25		15	ns	
49	tED1	Clock Rise to E Rise Delay		30		15	ns	
50	tED2	Clock Edge to E Fall Delay		30		15	ns	
51	PWEH	E Pulse Width (High)	25		20		ns	
52	PWEL	E Pulse Width (Low)	50		40		ns	
53	tEr	Enable Rise Time		10		10	ns	
54	tEf	Enable Fall Time		10		10	ns	
55	tTOD	Clock Fall to Timer Output Delay		75		50	ns	

Table 8. Z8L180 and Z8S180 Timings (Continued)

			Z8L180 20 MHz		Z80180 33 MHz			
No.	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
56	tSTDI	CSI/O Tx Data Delay Time (Internal) Clock Operation)		75		60	ns	
57	tSTDE	CSI/O Tx Data Delay Time (External Clock Operation)		7.5 tcyc +100 ns		7.5 tcyc +100 ns		
58	tSRSI	CSI/O Rx Data Setup Time (Internal Clock Operation)		1	1		tcyc	
59	tSRHI	CSI/O Rx Data Hold Time (Internal Clock Operation)		1	1		tcyc	
60	tSRSE	CSI/O Rx Data Setup Time (External Clock Operation)		1	1		tcyc	
61	tSRHE	CSI/O Rx Data Hold Time (External Clock Operation)		1	1		tcyc	
62	tRES	$\overline{\text{RESET}}$ Setup time to Clock Fall	40		25		ns	
63	tREH	$\overline{\text{RESET}}$ Hold time from Clock Fall	25		15		ms	
64	tOSC	Oscillator Stabilization Time		20		20	ms	
65	tEXr	External Clock Rise Time (EXTAL)		10		5	ns	
66	tEXf	External Clock Fall Time (EXTAL)		10		5	ns	
67	tRr	$\overline{\text{RESET}}$ Rise Time		50		50	ms	Note[2]
68	tRf	$\overline{\text{RESET}}$ Fall Time		50		50	ms	Note[2]
69	tIr	Input Rise Time (Except EXTAL, $\overline{\text{RESET}}$)		50		50	ns	Note[2]
70	tIf	Input Fall Time (Except EXTAL, $\overline{\text{RESET}}$)		50		50	ns	Note[2]
71	TdCS	$\overline{\text{MREQ}}$ Valid to $\overline{\text{ROMCS}}$, $\overline{\text{RAMCS}}$ Valid Delay		15		10	ns	
72	TdIOCS	$\overline{\text{IORQ}}$ Valid to $\overline{\text{IOCS}}$ Valid Delay		15		10	ns	

NOTES:

1. These AC parameters values are preliminary and subject to change without notice.
All specifications reflect 100% output drive (disabled slew rate limiting feature).
2. Specification 1 through 5 refer to PHI clock output.

ESCC Timing

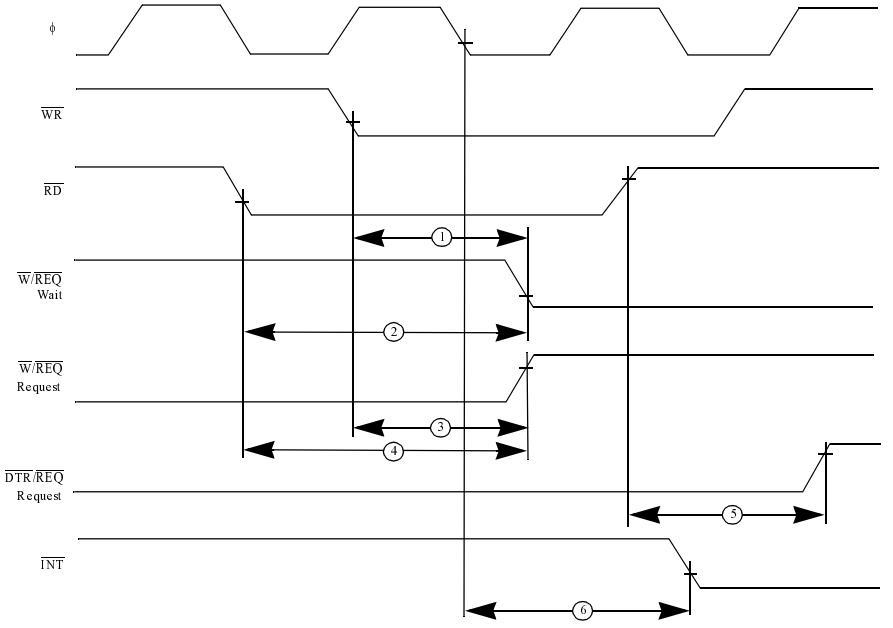


Figure 19. ESCC AC Parameter

Table 9. ESCC Timing Parameters

			20 MHz		
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Unit**
1	TdWR(W)	MR Fall to Wait Valid Delay		50	ns
2	TdRD(W)	$\overline{RD}$ Fall to Wait Valid Delay		50	
3	TdWRf(REQ)	MR Fall to $\overline{W}/\overline{REQ}$			
		Not Valid Delay		65	
4	TdRDf(REQ)	$\overline{RD}$ Fall to /W/$\overline{REQ}$			
		Not Valid Delay		65	
5	TdRdr(REQ)	$\overline{RD}$ Rise to $\overline{DTR}/\overline{REQ}$			
		Not Valid Delay		TBD	
6	TdPC(INT)	Clock to $\overline{INT}$ Valid Delay		160	

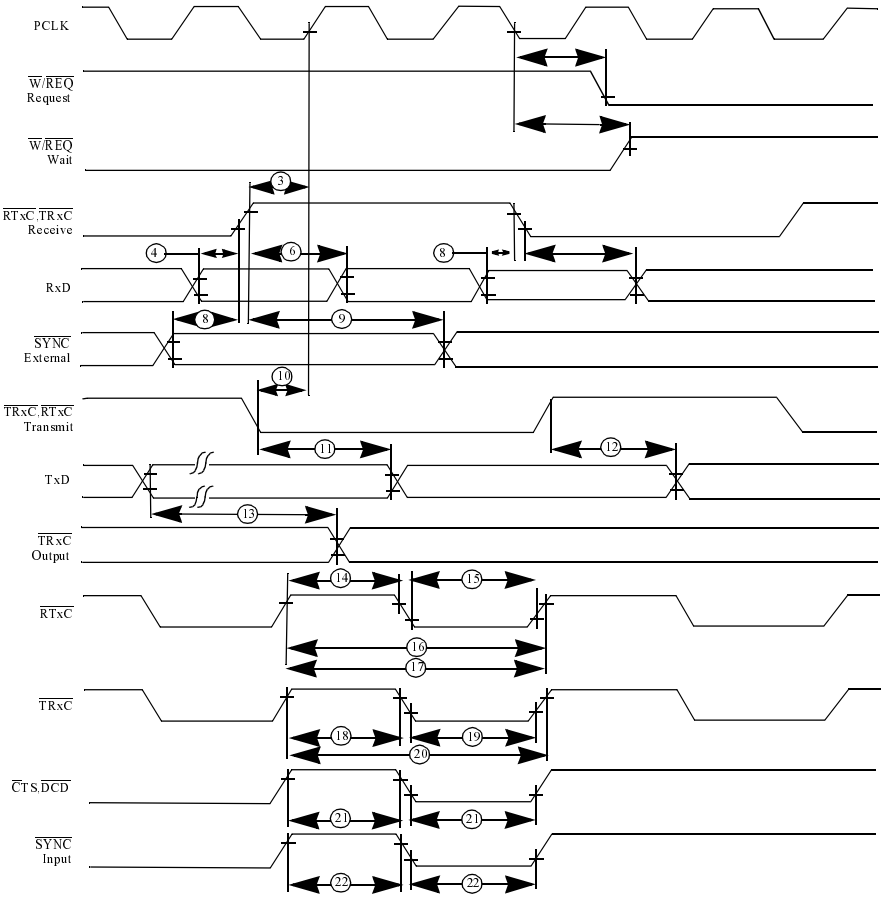


Figure 20. Z85230 General Timing Diagram

Table 10. Z85230 General Timing Table

			20 MHz			
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Notes**	**Units**
1	TdPC(REQ)	$\overline{PCLK}$ to W/REQ Valid		70		ns
2	TdPC(W)	$\overline{PCLK}$ to Wait Inactive		170		ns
3	TsRxC(PC)	$\overline{RxC}$ to $\overline{PCLK}$ Setup Time	N/A		Note[1,2]	
4	TsRxD(RxCr)	RxD to $\overline{RxC}$ Setup Time		0	Note[1]	
5	ThRxD(RxCr)	RxD to $\overline{RxC}$ Hold Time	45		Note[1]	ns
6	TsRxD(RxCf)	RxD to $\overline{RxC}$ Setup Time	0		Note[1,3]	ns
7	ThRxD(RxCf)	RxD to $\overline{RxC}$ Hold Time	45		Note[1,3]	ns
8	TsSY(RxC)	$\overline{SYNC}$ to $\overline{RxC}$ Setup Time	-90		Note[1]	ns
9	ThSY(RXC)	$\overline{SYNC}$ to $\overline{RxC}$ Hold Time	5TcPc		Note[1]	
10	TsTxC(PC)	$\overline{TxC}$ to $\overline{PCLK}$ Setup Time	N/A		Note[4,2]	
11	TdTxCf(TXD)	$\overline{TxC}$ to TxD Delay		70	Note[4]	ns
12	TdTxCr(TXD)	$\overline{TxC}$ to TxD Delay		70	Note[4,3]	ns
13	TdTxD(TRX)	TO to TRxC Delay		70		ns
14	TWRTxh	RTxC High Width	70		Note[5]	ns
15	TWRTxI	TRxC Low Width	70		Note[5]	ns
16a	TcRTx	RTxC Cycle Time	200		Note[5,6]	ns
16b	TxRx(DPLL)	DPLL Cycle Time Min	50		Note[6,7]	ns
17	TcRTxx	Crystal Osc. Period	61	1000	Note[8]	ns
18	TWTRxh	TRxC High Width	70		Note[5]	ns
19	TWTRxl	TRxC Low Width	70		Note[5]	ns
20	TcTRx	TRxC Cycle Time	200		Note[5,6]	ns
21	TwExT	DCD or CTS Pulse Width	60			ns
22	TWSY	SYNC Pulse Width	60			ns

NOTES:

1. These AC parameter values are preliminary and subject to change without notice.
   RxC is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
2. Synchronization of RxC to PCLK is eliminated in divide by four operation.
3. Parameter applies only to FM encoding/decoding.
4. TxC is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
5. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
6. The maximum receive or transmit data rate is 1/4 PCLK.
7. Applies to DPLL clock source only. Maximum data rate of 1/4 PCLK still applies. DPLL clock must have a 50% duty cycle.
8. Both $\overline{RTxC}$ and $\overline{SYNC}$ have 30 pF capacitors to ground connected to them.

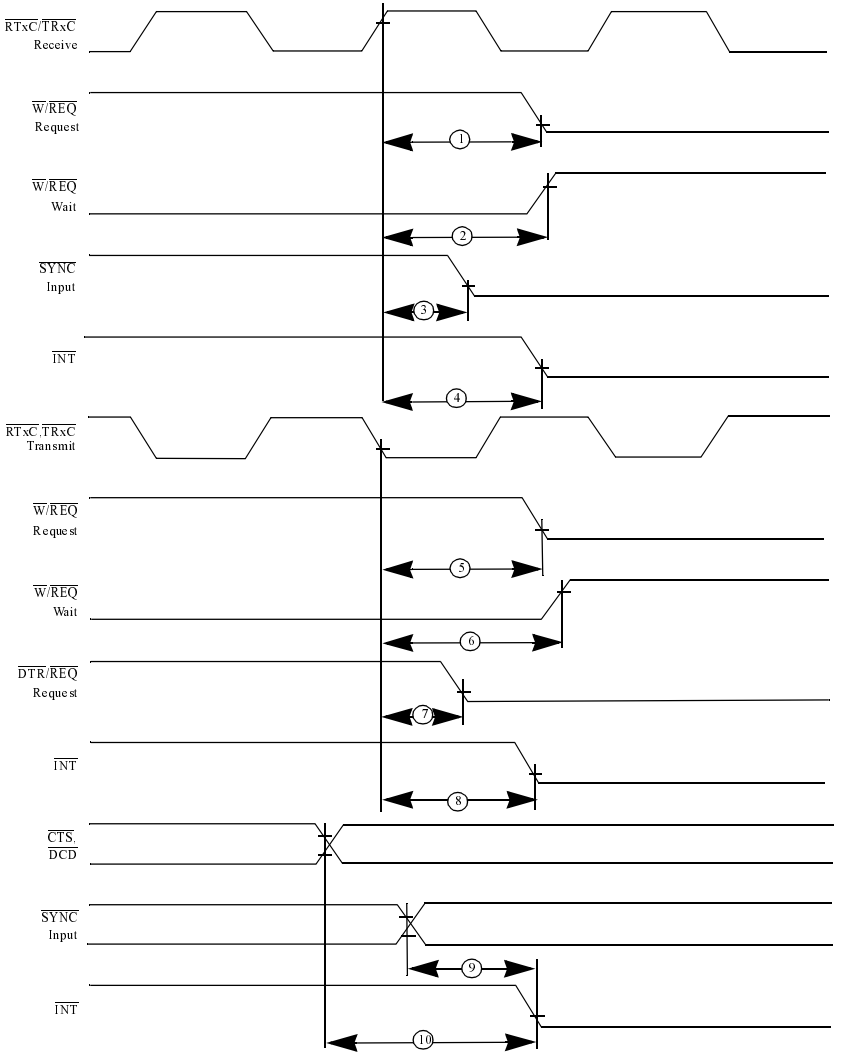


Figure 21. Z85230 System Timing Diagram

Table 11. Z85230 System Timing Table

			20 MHz			
No.	Symbol	Parameter	Min	Max	Notes[1]	Units
1	TdRxC(REQ)	$\overline{RxC}$ to $\overline{W}/\overline{REQ}$ Valid	13	18	Note[2]	ns
2	TdRxC(W)	$\overline{RxC}$ to /Wait Inactive	13	18	Note[2,3]	ns
3	TdRxC(SY)	$\overline{RxC}$ to $\overline{SYNC}$ Valid	9	13	Note[2]	ns
4	TdRxC(INT)	$\overline{RxC}$ to $\overline{INT}$ Valid	15	22	Note[2,3]	ns
5	TdTxC(REQ)	$\overline{TxC}$ to $\overline{W}/\overline{REQ}$ Valid	8	12	Note[4]	ns
6	TdTxC(W)	$\overline{TxC}$ to $\overline{Wait}$ Inactive	8	15	Note[3,4]	ns
7	TdTxC(DRQ)	$\overline{TxC}$ to $\overline{DTR}/\overline{REQ}$ Valid	7	11	Note[4]	ns
8	TdTxC(INT)	$\overline{TxC}$ to $\overline{INT}$ Valid	9	14	Note[3,4]	ns
9	TdSY(INT)	$\overline{SYNC}$ to $\overline{INT}$ Valid	2	6	Note[3]	ns
10	TdExT(INT)	$\overline{DCD}$ or $\overline{CTS}$ to $\overline{INT}$ Valid	3	9	Note[3]	ns

NOTES:
1. These AC parameters values are preliminary and subject to change without notice.. Units equal to TcPc.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. Open-drain output, measured with open-drain test load.
4. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

Table 12. I/O Port Timing

			Z8L182 20 MHz		Z80182 33 MHz		
No.	Symbol	Parameter	Min	Max	Min	Max	Units
1	TsPIA(RD)	Port Data Input Setup to $\overline{RD}$ Fall	20		20		ns
2	ThPIA(RD)	Port Data Input Hold From $\overline{RD}$ Rise	0		0		ns
3	TdWRF(PIA)	Port Data Output Delay From $\overline{WR}$ Rise		30		30	ns
4	TFWRF(PIA)	Port Data Output Float From $\overline{WR}$ Rise	0	30	0	30	ns

Table 13. External Bus Master Timing

			ZSL182 20 MHz		Z80182 33 MHz		
No.	Symbol	Parameter	Min	Max	Min	Max	Units
1	TsA(IORQf)	Address to $\overline{IORQ}$ Fall Setup	10		5		ns
2	TslOf(WRf)	$\overline{IORQ}$ Fall to MR Fall Setup	0		0		
3	TslOf(RDf)	$\overline{IORQ}$ Fall to $\overline{RD}$ Fall Setup	0		0		
4	ThIOR(WRR)	$\overline{IORQ}$ Rise From $\overline{WR}$ Rise Hold	0		0		
5	ThIOR(RDR)	$\overline{IORQ}$ Rise From $\overline{RD}$ Rise Hold	0		0		
6	TdRDf(DO)	$\overline{RD}$ Rise to Data Out Valid Delay		50		45	ns
7	THRDR(DO)	$\overline{RD}$ Rise to Data Out Valid Hold		0		0	
8	TSD(WRR)	Data In to $\overline{WR}$ Fall Setup	50		50		ns
9	THD(WRR)	Data In From $\overline{WR}$ Rise Hold	10	8	10		ns

General-Purpose I/O Port Timing

This figure shows the timing for the Ports A, B and C. Parameters referred to in this figure appear in Tables D and E.

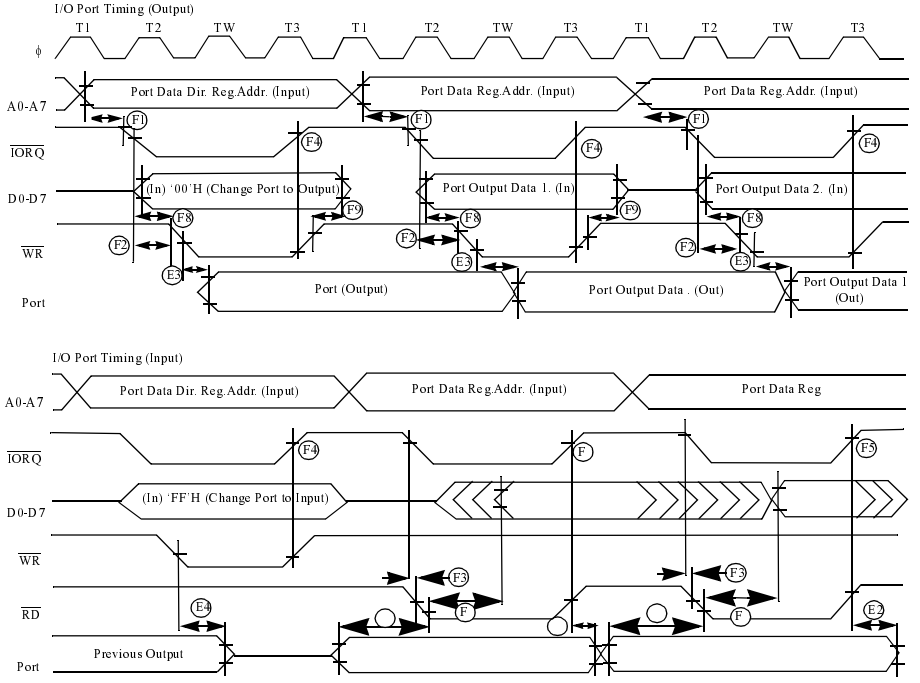


Figure 22. PORT Timing

Read Write External Bus Master Timing

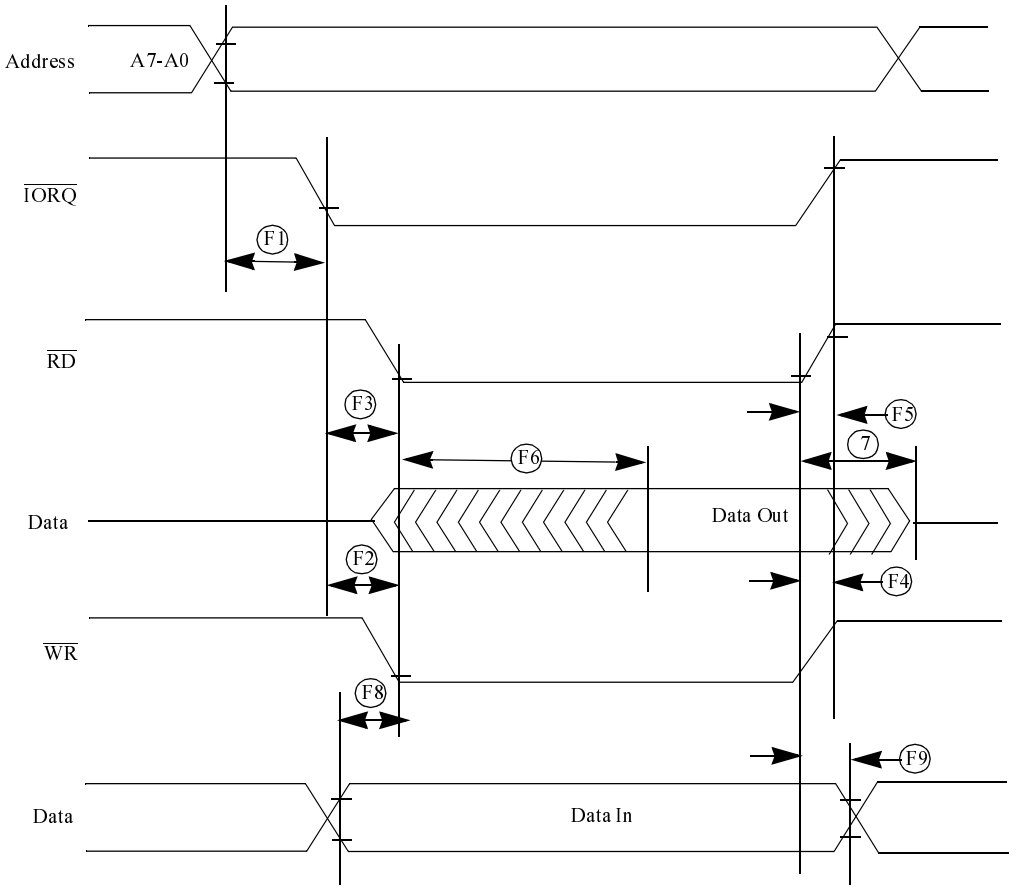


Figure 23. Read/Write External Bus Master Timing

ESCC External Bus Master Timing

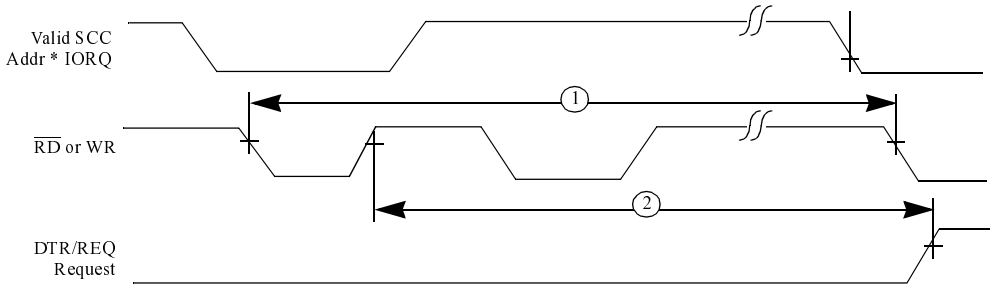


Figure 24. ESCC External Bus Master Timing

Table 14. External Bus Master Interface Timing (SCC Related Timing)

			Z8L82 20 MHz		Z80182 33 MHz			
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TrC	Valid Access Recovery Time	4TcC		4TcC		ns	Note[1]
2	TdRDr(REQ)	$\overline{RD}$ Rise to $\overline{DTR/REQ}$ Not Valid Delay	4TcC		4TcC		ns	

NOTES:
1. These AC parameter values are preliminary and are subject to change without notice. Applies only between transactions involving the ESCC. T_{CC} = ESCC clock period time

16550 MIMIC TIMING

Refer to Figure 25 through Figure 31 for MIMIC AC Timing.

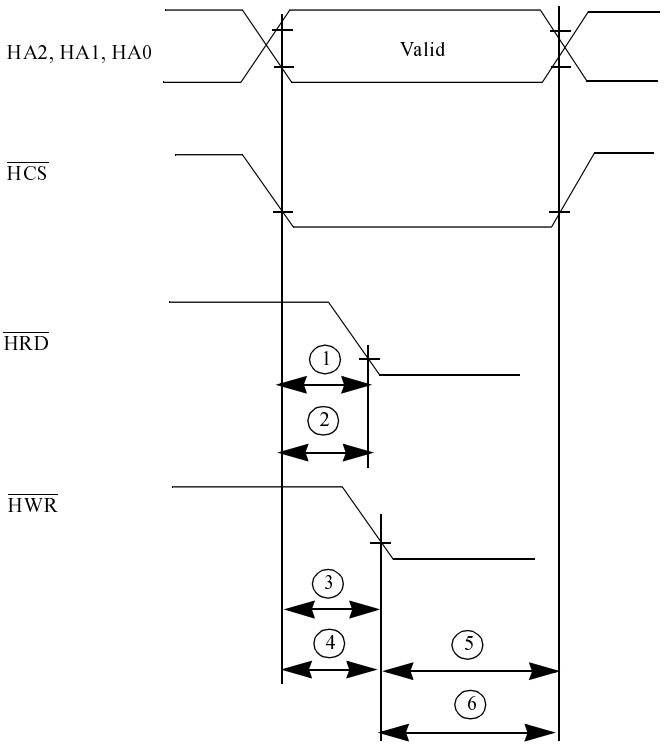


Figure 25. PC Host $\overline{RD}$ $\overline{WR}$ Timing

Table 15. PC Host $\overline{RD}$ $\overline{WR}$ Timing

			Z8L182 20 MHz		Z80182 33 MHz		
No.	Symbol	Parameter[1]	Min	Max	Min	Max	Units
1	tAR	$\overline{HRD}$ Delay from Address	30		30		ns
2	tCSR	$\overline{HRD}$ Delay from $\overline{HCS}$	30		30		ns
3	tAW	$\overline{HWR}$ Delay from Address	30		30		ns

Table 15. PC Host $\overline{RD}$ $\overline{WR}$ Timing

			Z8L182 20 MHz		Z80182 33 MHz		
No.	Symbol	Parameter[1]	Min	Max	Min	Max	Units
4	tCSW	$\overline{HWR}$ Delay from $\overline{HCS}$	30		30		ns
5	tAh	Address Hold Time	20		20		ns
6	tCSh	$\overline{HCS}$ Hold Time	20		20		ns

NOTES:
1. These AC parameter values are preliminary and are subject to change without notice.

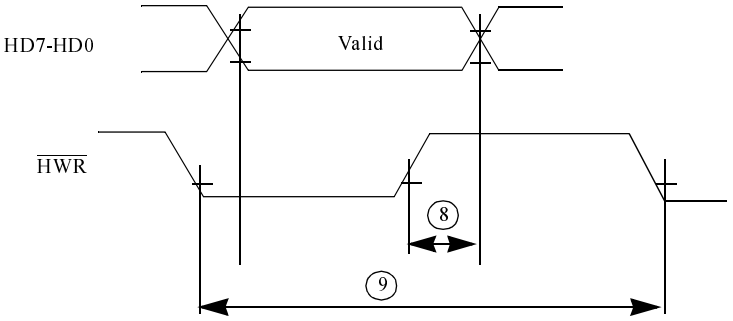


Figure 26. MIMIC Data Setup and Hold, Output Delay, Write Cycle

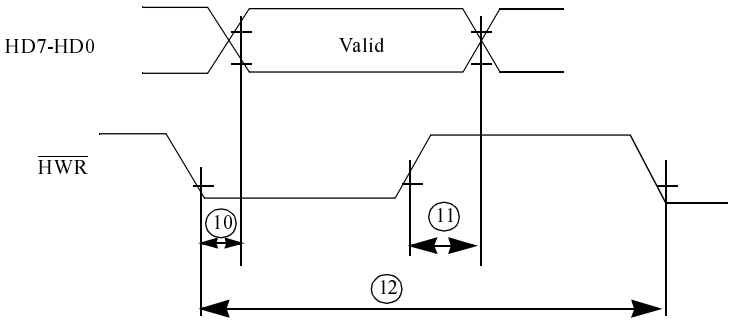


Figure 27. MIMIC Data Setup and Hold, Output Delay, Read Cycle

Table 16. Data Setup and Hold, Output Delay, Read Cycle

			Z8L182 20 MHz		Z80182 33 MHz		
No.	**Sym**	**Parameter[1]**	**Min**	**Max**	**Min**	**Max**	**Units**
7	tDs	Data Setup Time	30		30		ns
8	tDh	Data Hold Time	30		30		ns
9	tWc	Write Cycle Delay	2.5 MPU Clock Cycles		2.5 MPU Clock Cycles		tcyc
10	tRvD	Delay from $\overline{HRD}$ to Data		125		125	ns
11	tHz	$\overline{HRD}$ to Floating Delay		100		100	ns
12	tRc	Read Cycle Delay	2.5		2.5		tcyc

NOTES:
1. These AC parameter values are preliminary and are subject to change without notice.

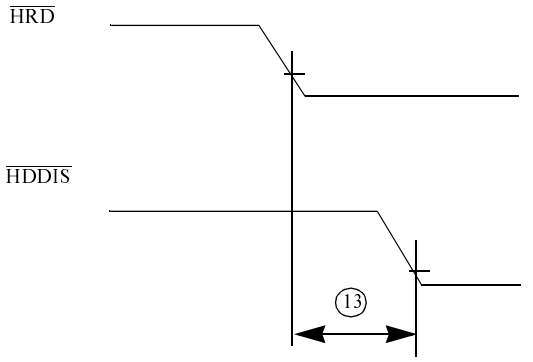


Figure 28. Driver Enable Timing

Table 17. Driver Enable Timing

			ZSL182 20 MHz		Z80182 33 MHz		
No.	**Sym**	**Parameter[1]**	**Min**	**Max**	**Min**	**Max**	**Units**
13	tRDD	HRD to Driver Enable/Disable		60		60	ns

NOTES:
1. These AC parameter values are preliminary and are subject to change without notice.

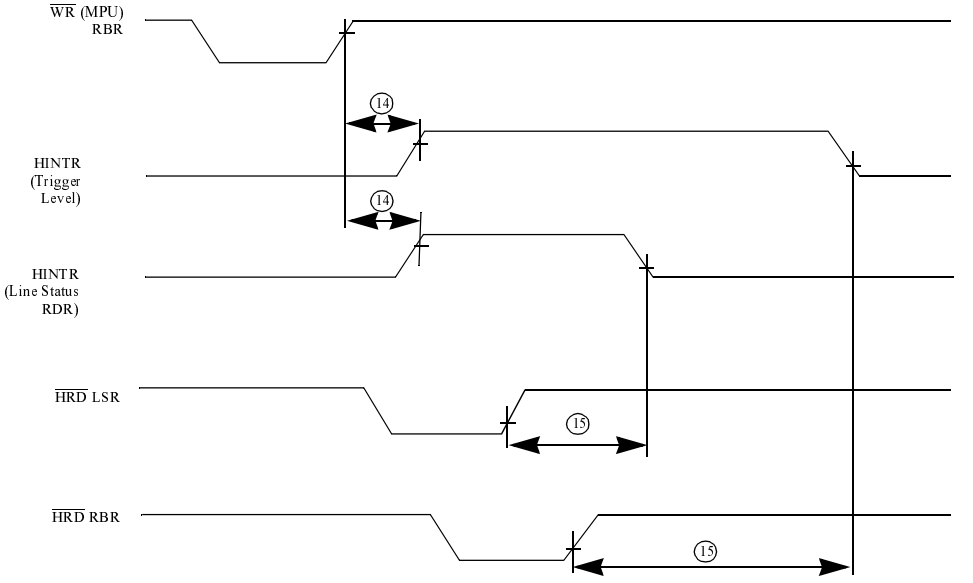


Figure 29. MIMIC Interrupt Timing RCVR FIFO

Table 18. Interrupt Timing RCVR FIFO

			ZSL182 20 MHz		Z80182 33 MHz	
No.	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**
14	tSINT	Delay from Stop to Set Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles
15	tRINT	Delay from HRD (RD RBR or RD LSR) to Reset Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles

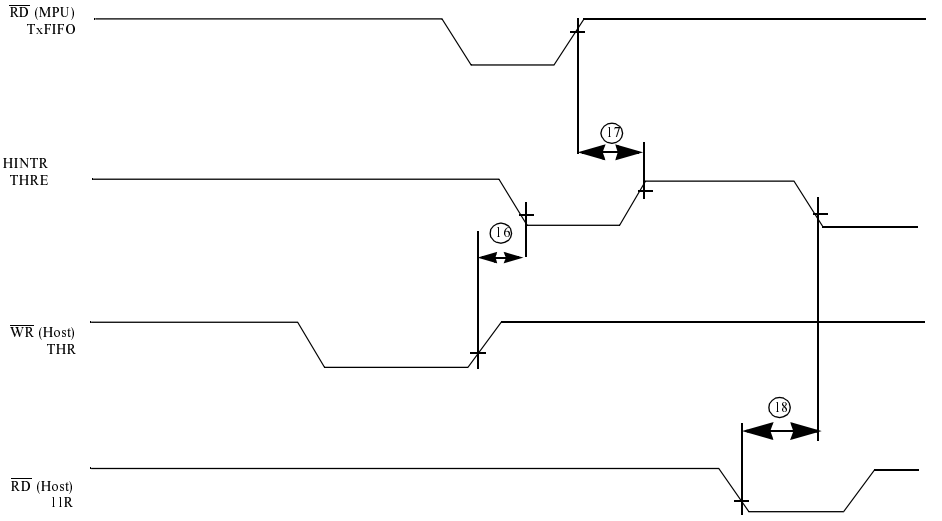


Figure 30. MIMIC Interrupt Timing Transmitter FIFO

Table 19. Interrupt Timing Transmitter FIFO

			ZSL182 20 MHz		Z80182 33 MHz	
No.	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**
16	tHR	Delay from WR (WR THR) to Reset Interrupt		2.5 MPU Clock Cycles		2.5 MPU Clock Cycles
17	TSTI	Delay from Stop to Interrupt (THRE)	2 MPU Clock Cycles		2 MPU Clock Cycles	
18	TIR	Delay from RD (RD IIR) to Reset Interrupt (THRIE)		2.5 MPU Clock Cycles		2.5 MPU Clock Cycles

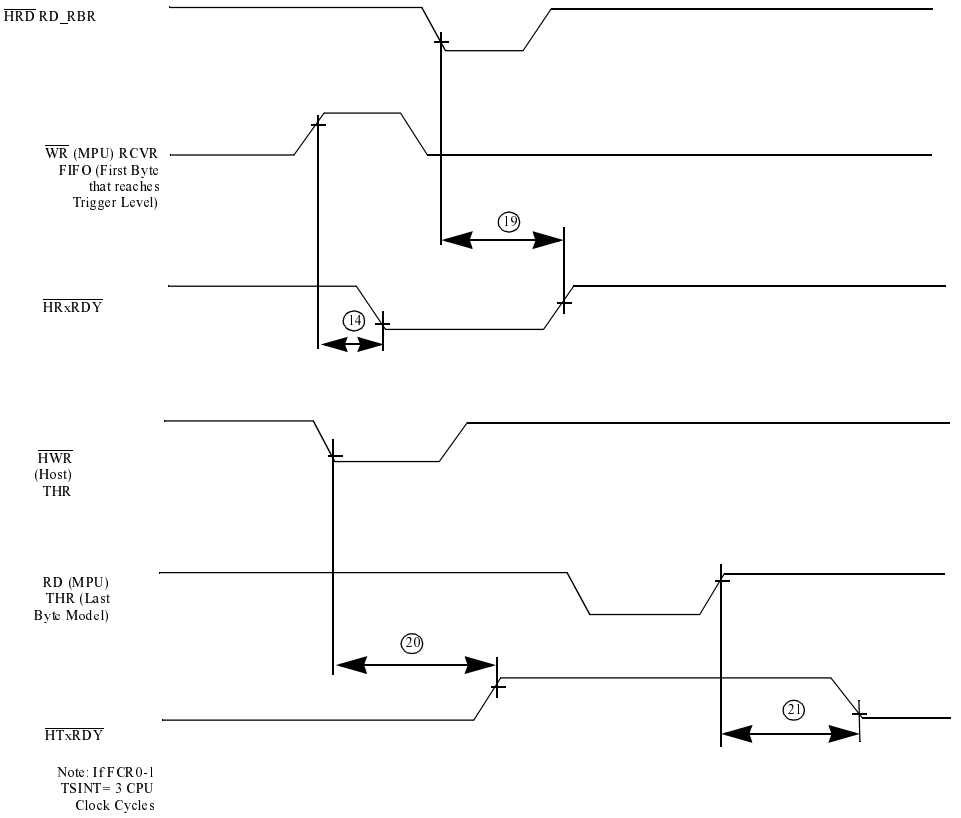


Figure 31. MIMIC RCVR FIFO Bytes Other than First

Table 20. RCVR FIFO Bytes Other than First

No	Sym	Parameter[1]	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max	Units
19	tRXi	Delay from $\overline{HRD}$ RBR to $\overline{HTxRDY}$ Inactive		10 Clock Cycles		10 Clock Cycles	
20	TWxi	Delay from Write to $\overline{HTxRDY}$ Inactive		5 Clock Cycles		5 Clock Cycles	
21	tSXa	Delay From Start to $\overline{HTxRDY}$ Active		3 MPU Clock Cycles		3 MPU Clock Cycles	

NOTES:
1. These AC parameter values are preliminary and are subject to change without notice.

Clock Generator

The Z80182/Z8L182 ZIP™ uses the Z182 MPUs on-chip clock generator to supply system clock. The required clock is easily generated by connection a crystal to the external terminals (XTAL,EXTAL). The clock output runs at half the crystal frequency for X2 mode.

Recommended characteristics of the crystal and the values for the capacitor are as follows (the values change with crystal frequency).

- Type of crystal:
  - Fundamental, parallel type crystal (AT cut is recommended).
- Frequency tolerance:
  - Application dependent.
- CL, Load capacitance:
  - Approximately 22 pF (acceptable range is 20-30 pF).
- RS, equivalent-series resistance:
  - 60 Ohms
  - $C_{IN} = C_{OUT}$ = 15-22 pF.

For PHI > 15 MHz (X2 Mode), it is recommended that an oscillator be used as input to EXTAL.

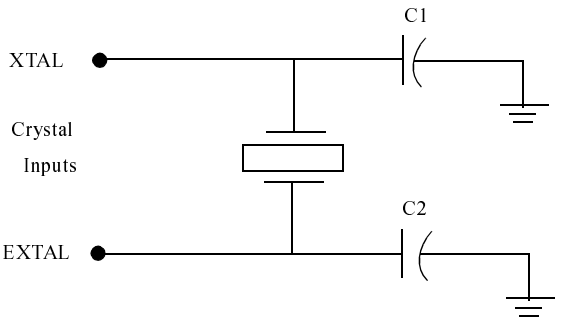


Figure 32. Circuit Configuration For Crystal

Functional Description

Functionally, the on-chip Z182 MPU and ESCC™ are identical to the discrete devices (Figure 1). For a detailed description of each individual unit, refer to the Product Specification/Technical Manuals of each discrete product. The following subsections describe each of the individual units of the Z182.

Z182 MPU FUNCTIONAL DESCRIPTION

This unit provides all the capabilities and pins of the ZiLOG Z8S180 MPU (Static Z80180 MPU). Figure 33 contains the S180 MPU Block Diagram of the Z182. This unit allows 100% software compatibility with existing Z180™ (and Z80® software. The following section is an overview of the major functional units of the Z182.

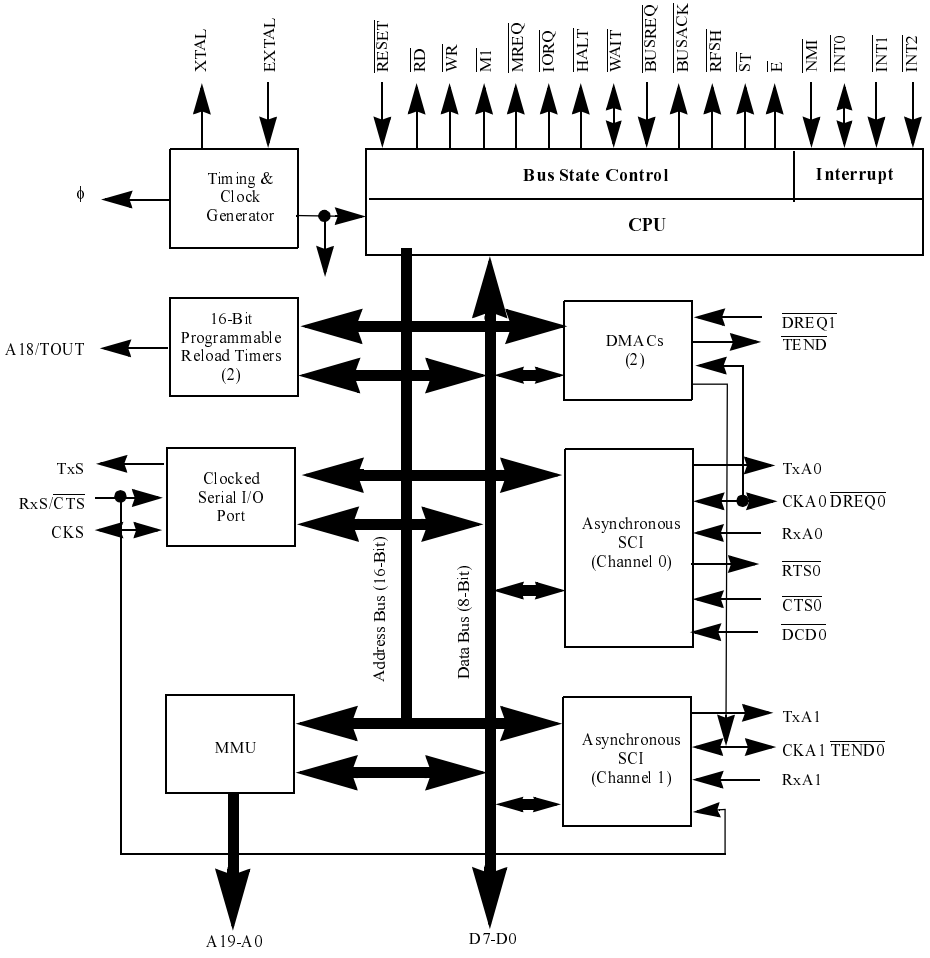


Figure 33. S180 MPU Block Diagram of Z182

Z182 CPU

The Z182 CPU is 100% software compatible with the Z80(R) CPU and has the following additional features:

Faster Execution Speed. The Z182 CPU is "fine tuned," making execution speed, on average, 10% to 20% faster than the Z80 CPU.

Enhanced DRAM Refresh Circuit. Z182 CPU's DRAM refresh circuit does periodic refresh and generates an 8-bit refresh address. It can be disabled or the refresh period adjusted, through software control.

Enhanced Instruction Set. The Z182 CPU has seven additional instructions to those of the Z80 CPU, which include the MLT (Multiply) instruction.

HALT and Low Power Modes of Operation. The Z182 CPU has HALT and Low Power modes of operation, which are ideal for the applications requiring low power consumption like battery operated portable terminals.

System Stop Mode. When the Z182 is in System Stop mode, it is only the Z180 MPU that is in STOP mode. Standby and Idle Mode. Please refer to the Z8S180 Product Specification for additional information on these two additional Low Power modes.

Instruction Set. The instruction set of the Z182 CPU is identical to the Z180. For more details about each transaction, please refer to the Product Specification/Technical Manual for the Z1 80/Z80 CPU.

Z182 CPU Basic Operation

Z182 CPU's basic operation consists of the following events. These are identical to the Z180 MPU. For more details about each operation, please refer to the Product Specification/Technical Manual for the Z180.

- Operation Code Fetch Cycle
- Memory Read/Write Operation
- Input/Output Operation
- Bus Request/Acknowledge Operation
- Maskable Interrupt Request Operation
- Trap and Non-Maskable Interrupt Request Operation
- HALT and Low Power Modes of Operation
- Reset Operation

Memory Management Unit (MMU)

The Memory Management Unit (MMU) allows the user to map the memory used by the CPU (64 Kbytes of logical addressing space) into 1 Mbyte of physical addressing space. The organization of the MMU allows object code compatibility with the Z80 CPU while offering access to an extended memory space. This is accomplished by using an effective common area-banked area scheme.

DMA Controller

The Z182 MPU has two DMA controllers. Each DMA controller provides high-speed data transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory-to/from-I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. The DMA can access the full 1 Mbytes addressing range with a block length up to 64 Kbytes and can cross over 64K boundaries.

Asynchronous Serial Communication Interface (ASCI)

This unit provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels also support a multiprocessor communication format.

Programmable Reload Timer (PRT)

The Z182 MPU has two separate Programmable Reload Timers, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is system clock divided by 20. PRT channel 1 provides an optional output to allow for waveform generation.

Clocked Serial I/O (CSI/O)

The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another CPU or MPU.

Programmable Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z182 MPU unit has a programmable wait state generator. By programming the DMA/WAIT Control Register (DCNTL), up to three wait states are automatically inserted in memory and I/O cycles. This unit also inserts wait states during on-chip DMA transactions. When using RAMCS and ROMCS wait state generators, the wait state controller with the most programmed wait states determines the number of wait states inserted.

Z8S180 MPU Register Map

Note: Registers listed in boldface type represent new registers added to the Z8S180. All register addresses not listed are Reserved.

Table 21. Z8S180 MPU Register Map

Register Name	I/O Addr/Access
Control Register A Ch 0	%0000/40/80 R/W
ASCI Control Register A Ch 1	%0001/41/81 R/W
ASCI Control Register B Ch 0	%0002/42/82 R/W
ASCI Control Register B Ch 1	%0003/43/83 R/W
ASCI Status Register Ch 0	%0004/44/84 R/W
ASCI Status Register Ch 1	%0005/45/85 R/W
ASCI TX Data Register Ch 0	%0006/46/86 R/W
ASCI TX Data Register Ch 1	%0007/47/87 R/W
ASCI RX Data Register Ch 0	%0008/48/88 R/W
ASCI RX Data Register Ch 1	%0009/49/89 R/W
CSIO Control Register	%000A/4A/8A R/W
CSIO Transmit/Receive Data Reg.	%000B/4B/8B R/W
Timer Data Register Ch OL	%000C/4C/8C R/W
Timer Data Register Ch OH	%000D/4D/8D R/W
Reload Register Ch OL	%000E/4E/8E R/W
Reload Register Ch OH	%000F/4F/8F R/W
Timer Control Register	%0010/50/90
ASCIO Extension Control Reg.	%0012/52/92 R/W
ASCII Extension Control Reg.	%0013/53/93 R/W
Timer Data Register Ch 1L	%0014/54/94 R/W
Timer Data Register Ch 1H	%0015/55/95 R/W
Timer Reload Register Ch 1L	%0016/56/96 R/W
Timer Reload Register Ch 1H	%0017/57/97 R/W
Free Running Counter	%0018/58/98 R/W
ASCIO Time Constant Low	%001A/5A/9A R/W
ASCIO Time Constant High	%001B/5B/9B R/W
ASCII Time Constant Low	%00IC/5C/9C R/W
ASCII Time Constant High	%001D/5D/9D RW
Revision Register	%00DA RW

Register Name	I/O Addr/Access
CPU Control Register	%001F/5F/9F R/W
DMA Source Addr Register Ch OL	%0020/60/A0 R/W
DMA Source Addr Register Ch OH	%0021/61/A1 R/W
DMA Source Addr Register Ch OB	%0022/62/A2 R/W
DMA Dest Addr Register Ch OL	%0023/63/A3 R/W
DMA Dest Addr Register Ch OH	%0024/64/A4 R/W
DMA Dest Addr Register Ch OB	%0025/65/A5 R/W
DMA Byte Count Register Ch OL	%0026/66/A6 R/W
DMA Byte Count Register Ch OH	%0027/67/A7 R/W
DMA Memory Addr Register Ch 1L	%0028/68/A8 R/W
DMA Memory Addr Register Ch 1H	%0029/69/A9 R/W
DMA Memory Addr Register Ch 1B	%002A/6A/AA R/W
DMA I/O Addr Register Ch 1L	%002B/6B/AB R/W
DMA I/O Addr Register Ch 1H	%002C/6C/AC R/W
DMA I/O Addr Register Ch 1B	%002D/6D/AD R/W
DMA Byte Count Register Ch 1L	%002E/6E/AE R/W
DMA Byte Count Register Ch 1H	%002F/6F/AF R/W
DMA Status Register	%0030170/B0 R/W
DMA Mode Register	%0031/71/B1 R/W
DMA/WAIT Control Register	%0032/72/B2 R/W
IL Register	%0033/73/B3 R/W
INT/TRAP Control Register	%0034/74/B4 R/W
Refresh Control Register	%0036/76/B6 R/W
MMU Common Base Register	%0038/78/B8 R/W
MMU Bank Base Register	%0039/79/B9 R/W
MMU Common/Bank Area Register	%003A/7A/BA R/W
Operation Mode Control Register	%003E/7E/BE R/W
I/O Control Register	%003F/7F/BF R/W

Z85230 ESCC™ FUNCTIONAL DESCRIPTION

The Zilog Enhanced Serial Communication Controller ESCC™ is a dual channel, multi-protocol data communication peripheral. The ESCC

functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.) The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem control in both channels in applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (number of the registers varies depending on the version), the user can configure the ESCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements. The ESCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the ESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The ESCC (Enhanced SCC) is pin and software compatible to the CMOS SCC version. The following enhancements were made to the CMOS SCC:

- Deeper Transmit FIFO (4 bytes)
- Deeper Receive FIFO (8 bytes)

- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced High with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers, 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced $\overline{\text{DTR}}$, /RTS deactivation timing

The following features are common to both the ESCC and the CMOS SCC:

- Two independent full-duplex channels
- Synchronous/Isochronous data rates:
  - Up to 1/4 of the PCLK using external clock source
  - Up to 5 Mbits/sec at 20 MHz PCLK (ESCC).

- Asynchronous capabilities
  - 5, 6, 7 or 8 bits/character (capable of handling 4 bits/character or less)
  - 1, 1.5, or 2 stop bits
  - Odd or even parity
  - Times 1, 16, 32 or 64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection
- Byte oriented synchronous capabilities:
  - Internal or external character synchronization
  - One or two sync characters (6 or 8 bits $\overline{\text{SYNC}}$ character) in separate registers
  - Automatic Cyclic Redundancy Check (CRC) generation/ detection
- SDLC/HDLC capabilities:
  - Abort sequence generation and checking
  - Automatic zero insertion and detection
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - CRC generation/detection
  - SDLC loop mode with EOP recognition/loop entry and exit
- NRZ, NRZI or FM encoding/decoding. Manchester Code Decoding (Encoding with External Logic).
- Baud Rate Generator in each Channel
- Digital Phase-Locked Loop (DPLL) for Clock Recovery
- Crystal Oscillator

The following features are implemented in the ESCC' for the Z80182/ Z8L182 only:

- New 32-bit CRC-32 (Ethernet Polynomial)
- ESCC Programmable Clock
  - programmed to be equal to system clock divided by one or two
  - programmed by Z80182 Enhancement Register

    Note: The ESCC-programmable clock must be programmed to divide-by-two mode when operating above the following conditions:
    PHI > 20 MHz at 5.0 V
    PHI > 10 MHz at 3.0 V

Z85230 ESCC™ Block Diagram

For a detailed description of the Z85230 ESCC, refer to the ESCC Technical Manual. Figure 34 contains the block diagram of the discrete ESCC, which was integrated into the Z182. The $\overline{INT}$ line is internally connected to INTO of the Z182.

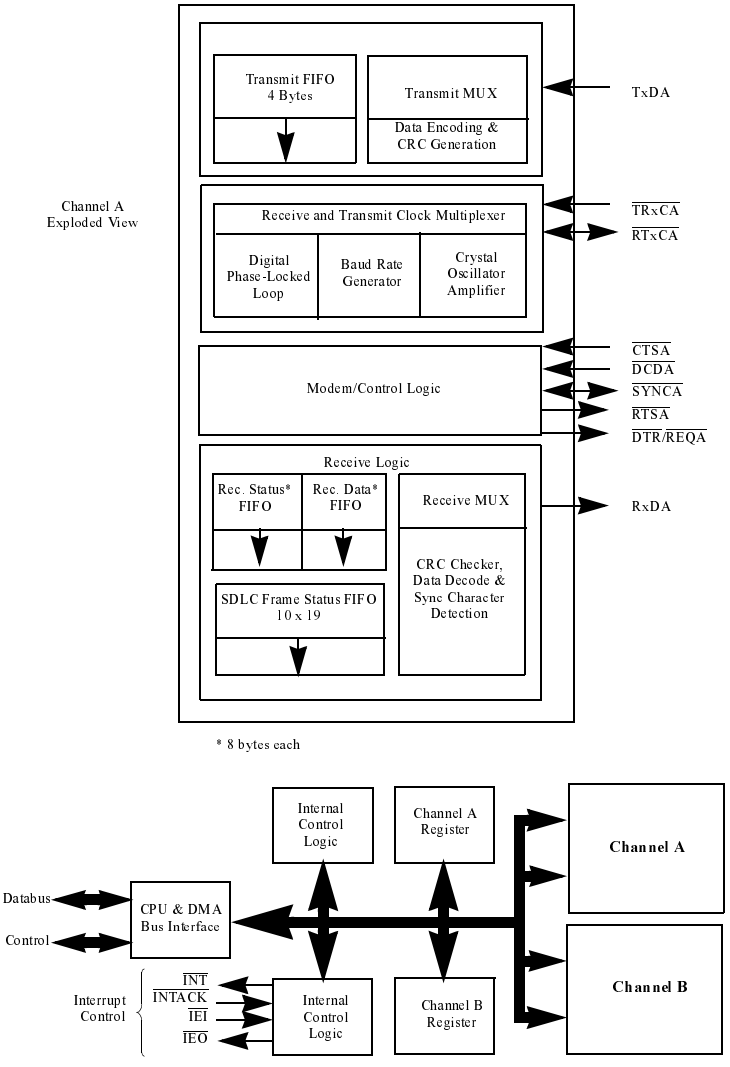


Figure 34. ESCC Block Diagram

16550 MIMIC Interface Functional Description

The Z801182/Z8L182 has a 16550 MIMIC interface that allows it to mimic the 16550 device. It has all the interface pins necessary to connect to the PC/XT/AT bus. It contains the complete register set of the part with the same interrupt structure. The data path allows parallel transfer of data to and from the register set by the internal Z80180 of the Z80182/ Z8L182. There is no shift register associated with the mimic of the 16550 UART. This interface saves the application from doing a serial transfer before performing data compression or error correction on the data.

Control of the register set is maintained by six priority encoded interrupts to the Z80182/Z8L182. When the PC/XT/AT writes to THR, MCR, LCR, DLL, DLM, FCR or reads the RBR, an interrupt to the Z80182/Z8L182 is generated. Each interrupt can be individually masked off or all interrupts can be disabled by writing a single bit. Both mode 0 and mode 2 interrupts are supported by the 16550 MIMIC interface.

Two eight-bit timers are also available to control the data transfer rate of the 16550 MIMIC interface. Their input is tied to the ESCC channel B divide clock, so a down count of 24 bits is possible. An additional two eight-bit timers are available for programming the FIFO timeout feature (Four Character Time Emulation) for both Receive and Transmit FIFO's.

The 16550 MIMIC interface supports the PC/XT/AT interrupt structure as well as an additional mode that allows for a wired Logic AND interrupt structure. The 16550 MIMIC interface is also capable of high speed parallel DMA transfers by using two control lines and the transmit and receive registers of the 16550 MIMIC interface.

All registers of the 16550 MIMIC interface are accessible in any page of I/O space since only the lowest eight address lines are decoded. See Figure 35 for a block diagram of the 16550 MIMIC interface.

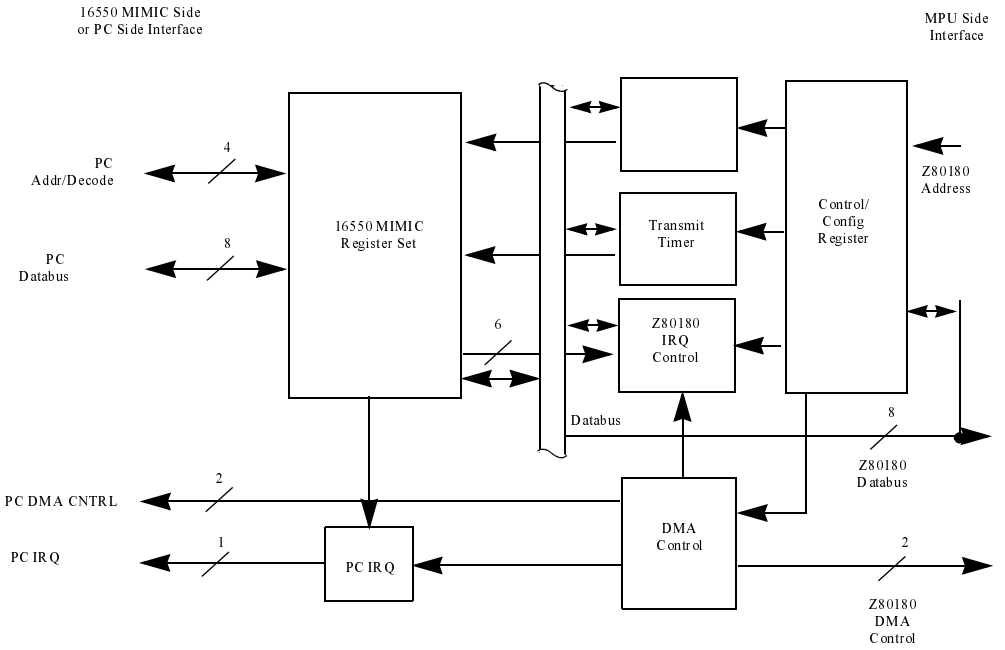


Figure 35. 16550 MIMIC Block Diagram

16550 MIMIC FIFO Description

The receiver FIFO consists of a 16-word F17O capable of storing eight data bits and three error bits for each character stored (Figure 36). Parity error, Framing error and Break detect bits are stored along with the data bits by copying their value from three shadow bits that are Write Only bits for the Z80180 MPU LSR address. The three shadow bits are cleared after they are copied to the FIFO memory. In FIFO mode, to write error bits into the receiver FIFO, the MPU must first write the Parity, Framing and Break detect status to the Line Status Register (shadow bits) and then

write the character associated into the receiver buffer. The data and error bits move into the same address in the FIFO. The error bits become available to the PC side of the interface when that particular location becomes the next address to read (top of FIFO). At that time, they may either be read by the PC by accessing them in the LSR, or they may cause an interrupt to the PC interface if so enabled. The error bits are set by the error status of the byte at the top of the FIFO, but may only be cleared by reading the LSR. If successive reads of the receiver FIFO are performed without reading the LSR, the status bits are set if any of the bytes read have the respective error bit set. See Table 22 for the setting and clearing of the Line Status Register bits.

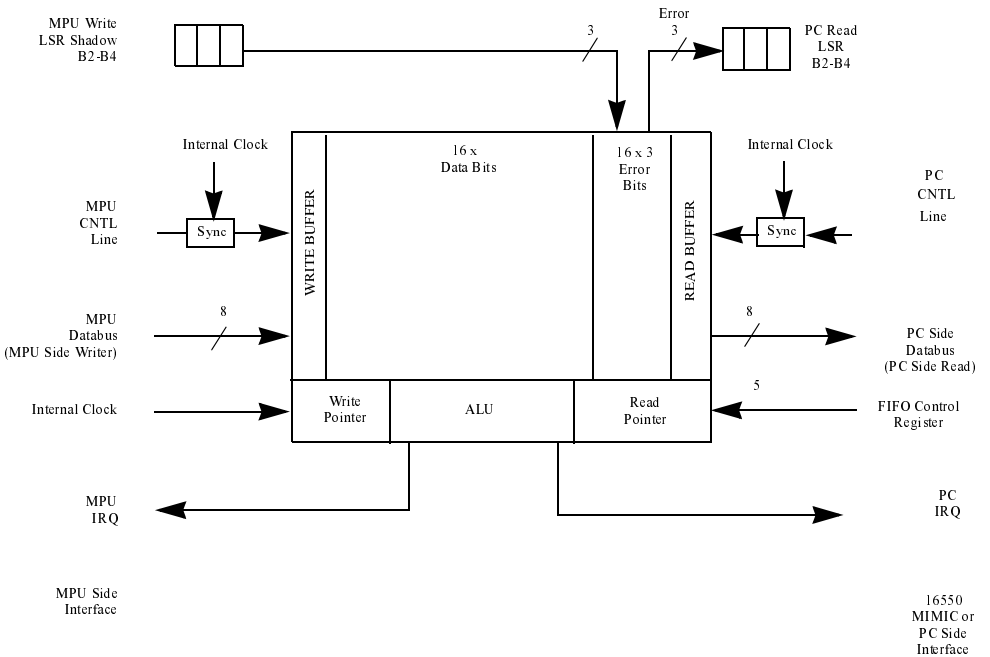


Figure 36. 16550 MIMIC Receiver FIFO Block Diagram

Table 22. 16550 Line Status Register

Error	Description	How to Set	How to Clear
Error in RCVR FIFO	At least one data byte available in FIFO with one error	At least one error in receiver FIFO	When there are no more errors
TEMT [1]	Transmitter empty	MPU writes a 1	MPU writes a 0
**THRE [2]	Transmitter holding register is empty	When MPU has read or emptied the holding register	When holding register is not empty
Break Detect	Break occurs when received data input is held in logic-0 for longer than a full word transmission	MPU writes 1	There is a PC-side read of the LSR
Framing Error	Received character did not have a valid stop bit	MPU writes 1	There is a PC-side read of the LSR
Parity Error	Received character did not have correct even or odd parity	MPU writes 1	There is a PC-side read of the LSR
Overrun Error	Overlapping received characters, thereby receiver destroying the previous character	MPU makes two writes to buffer register	There is a PC-side read of the LSR
*Data Ready	Indicates complete incoming data has been received	MPU writes to RCVR FIFO or receiver buffer register	Empty Receiver or Receiver FIFO

NOTES:
1. The TEMT and THRE bits take on different functions when TEMT/Double Buffer mode is enabled.
2. These signals are delayed to HOST when using character emulation delay.

The PC interface may be interrupted when 1, 4, 8 or 14 bytes are available in the receiver FIFO by setting bits 6 and 7 in the FCR (FIFO Control Register, PC address 02H) to the appropriate value. If the FIFO is not empty, but below the above trigger value, a timeout interrupt is available if the receiver FIFO is not written by the MPU or read by the PC from an interval determined by the Character Timeout Timer. This is an additional Timer with MPU access only that is used to emulate the 16550 4 character timeout delay.

The Receive FIFO timeout timers are designed to reload and begin countdown after every read or write of the Rx FIFO, regardless of the Rx trigger level or number of bytes in the FIFO. Therefore, it is possible to get Timeout interrupts more often than Receive data interrupts.To closely emulate a 16550, a receive timeout timer enhancement is provided. When enabling this feature, the timeout timer does not begin counting down

until the character emulation timer for each byte of data in the Rx FIFO has expired.

Note: Enabling this feature facilitates increased 16550 compatibility but may impede throughput.

If the Receive Timeout interrupt occurs, the PC HOST is allowed to read up to 4-5 consecutive characters before the Data Ready bit is forced to zero (even if there is still more data in FIFO). This capability is required to maintain character pacing.

The timer receives the ESCC $\overline{\text{TRxCB}}$ as its input clock. Software must determine the correct values to program into the Receiver Timeout register and the ESCC $\overline{\text{TRxCB}}$ to achieve the correct delay interval for timeout. These interrupts are cleared by the FIFO reaching the trigger point or by resetting the Timeout Interval Timer by FIFO MPU write or PC read access.

With FIFO mode enabled, the MPU is interrupted when the receiver FIFO is empty, corresponding to bit 5 being set in the IUS/IP register (MPU access only). This bit corresponds to a PC read of the receive buffer in non-FIFO (16450) mode. The interrupt source is cleared when the FIFO becomes non-empty or the MPU reads the IUS/IP register.

The transmitter FIFO is 16-byte FIFO with PC write and MPU read access (Figure 37). In FIFO mode, the PC receives an interrupt when the transmitter becomes empty corresponding to bit 5 being set in the LSR. This bit and the interrupt source are cleared when the transmit FIFO becomes non-empty or the Interrupt Identification Register (IIR) register is read by the PC.

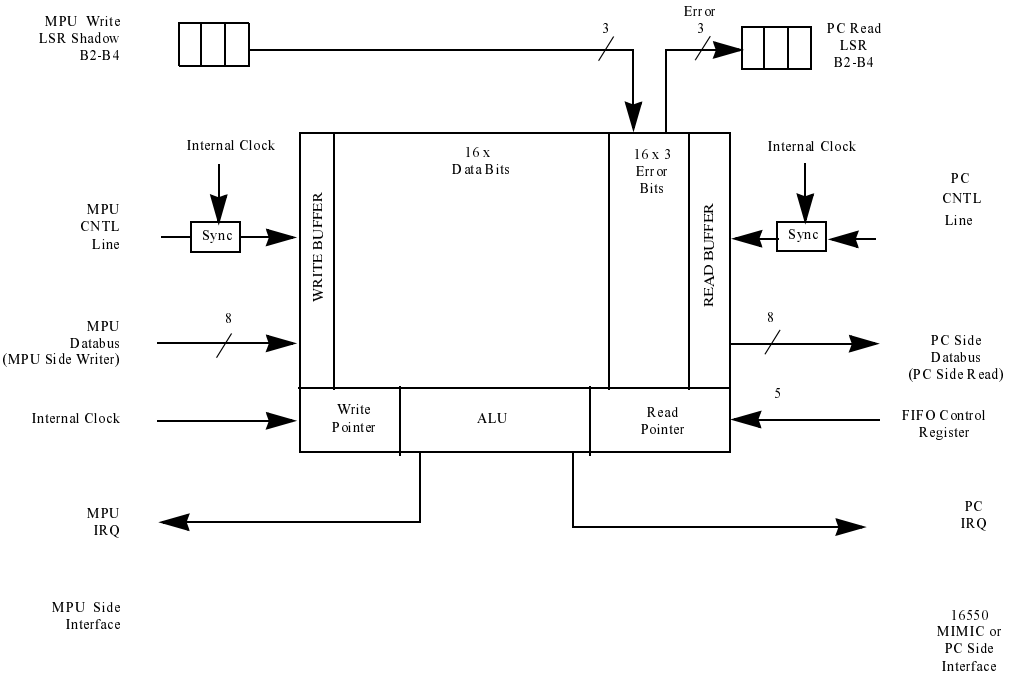


Figure 37. 16550 MIMIC Transmitter FIFO Block Diagram

On the MPU interface, the transmitted data available can be programmed to interrupt the MPU on 1, 4, 8 or 14 bytes of available data by seeing the appropriate value in the MPU FSCR control register (MPU write only xxECH) bits 6 and 7. A timeout feature exists, Transmit Timeout Timer, which is an additional 8-bit timer with SCC $\overline{\text{TxRCB}}$ as the input source. If the transmitter FIFO is non-empty and no PC write or MPU read of the FIFO has taken place within the timer interval, a timeout occurs causing a corresponding interrupt to the MPU.

Register Descriptions

16550 MIMIC INTERFACE REGISTERS

MIMIC Master Control Register (MMC)

The 16550 MIMIC interface is controlled by the MMC register. Setting it allows for different modes of operation such as using the 8-bit counters, DMA accesses, and which IRO structure is used with the PC/XT/AT.

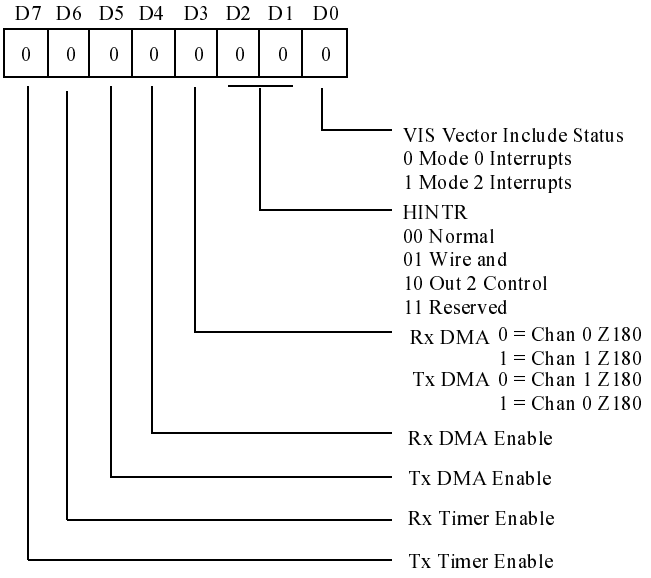


Figure 38. MIMIC Master Control Register (Z180 MPU Read/Write, Address xxFFH)

Bit 7 Transmit Emulation Delay Counter Enable (Read/Write)

If bit 7 is set to 1, it enables the transmit delay timer. When the Z180 reads the Transmit Register, it loads the transmit delay timer from the Transmit Time Constant Register and enables the timer to count down to zero. This timer delays setting the Transmit Holding Register Empty (THRE) bit until the timer times out. If this bit is 0, then THRE is set immediately on a Z180 read of the Transmit Register. This bit also enables the emulation timer used in Transmitter Double Buffering.

Bit 6 Receive Emulation Delay Counter Enable (Read/Write)

If bit 6 is set to 1, it enables the receive delay timer. When the Z180 writes to the Receive Buffer, it loads the receive delay timer from the Receive Time Constant Register and enables the timer to count down to zero. This timer delays setting the Data Ready (DR) bit in the LSR until the timer times out. If this bit is 0 then DR is set immediately on a Z180 write to the Receive Buffer.

Both counters are single pass and stop on a count of Zero. Their purpose is to delay data transfer just as if the 16550 UART had to shift the data in and out. This is provided to alleviate any software problems a high speed continuous data transfer might cause to existing software. If this is not a concern, then data can be read and written as fast as the two machines can access the devices. In FIFO mode of operation, the timers are used to delay the status to the PC interface by the time required to actually shift the characters out, or in, if an actual UART were present.

Bit 5 Transmit DMA Enable (Read/Write)

If this bit is set to 1, it enables the Transmit DMA function.

Bit 4 Receive DMA Enable (Read/Write)

If this bit is set to 1, it enables the Receive DMA function.

Bit 3 Receive DMA Channel Select (Read/Write)

If bit 3 is set to 0, then Receive DMA transfer is done through Z180 DMA channel 0 and the Transmit DMA is done through DMA channel 1. If bit 3 is set to 1, then Receive DMA transfer is done through Z180 DMA channel 1 and the Transmit DMA is done through DMA channel 0.

Bits 2,1 Interrupt Select (Read/Write).

See Table 23.

Bit 0 Vector Include Status (Read/Write)

This bit is used to select the interrupt response mode of the Z180. A 0 in this bit enables Mode 0 interrupts; a 1 enables Mode 2 response.

Table 23. MIMIC Master Control Register Interrupt Select

Bit 2	Bit 1	HINTR Function
0	0	HINTR is set to normal 16550 MIMIC mode. A fully driven output is required when external priority arbiters are used.
0	1	A wired AND condition on the HINTR pin is possible to the PC/XT/AT. The interrupt is active High with only the pull-up of the HINTR pin driving; otherwise this pin is tristate. Wired AND is needed when an external arbiter is not available.
1	0	HINTR is driven when out 2 of the Modem Control Register is 1. HINTR is tristate when MCR out 2 is 0.
1	1	RESERVED

IUS/IP Register

The IUS/IP Register is used by the Z180MPU to determine the source of the interrupt. This register contains the appropriate bit set when an interrupt occurs.

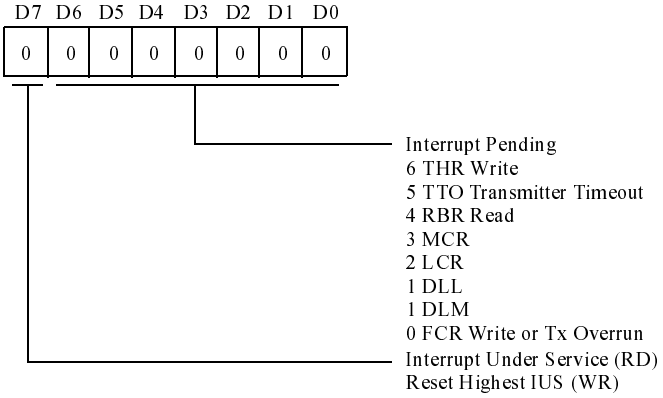


Figure 39. IUS/IP Register (Z180 MPU, Address xxFEH)

Bit 7 Interrupt Under Service (Read/Write)

This bit represents a logical OR of each individual [US bit for the internal MIMIC interrupt daisy chain. An IUS bit is set when an interrupt is registered (IP set) and enabled (IE set), the incoming IEI daisy chain is active (chain enabled) and an interrupt acknowledge cycle is entered. By writing a 1 to this bit the highest priority [US bit that is set is reset. Writing a 0 to this bit has no effect.

Note: Perform this process at the end of every MIMIC Interrupt Service routine.

Bit 6 Transmit Holding Register Written (Read Only)

This bit is set when the PC/XT/AT writes to the Transmit Holding Register. It is reset when the Z180 MPU reads the Transmit Holding Register. In FIFO mode, this bit is set when the trigger level is reached (4,8,14 bytes available).

Note: The THR bit is set (interrupts) when the transmitter FIFO reaches the data available trigger level set in the MPU FCR control register. The bit and interrupt source is cleared when the number of data bytes falls below the set trigger level.

Bit 5 Transmitter Timeout with Data in FIFO (Read Only)

This bit is set when the transmitter FIFO has been idle (no read or write and timer decrements to zero) with data bytes below the trigger level. It is cleared when the FIFO is read or written.

Bit 4 Receive Buffer Read (Read Only)

This bit is set when the PC/XT/AT reads the Receive Buffer Register. It is reset when the Z180 MPU writes to the Receive Buffer Register. In FIFO mode, this bit is set upon the PC reading all the data in the receive FIFO. Note: RBR is set and interrupts when the receive FIFO has been emptied by the PC. This bit and interrupt are cleared when one or more bytes are written into the receive FIFO by the MPU.

Bit 3 Modem Control Register Write (Read Only)

This bit is set when the PC/XT/AT writes to the Modem Control Register. It is reset when the Z180MPU reads the Modem Control Register.

Bit 2 Line Control Register Write (Read Only)

This bit is set when the PC/XT/AT writes to the Line Control Register. It is reset when the Z180 MPU reads the Line Control Register.

Bit 1 Divisor Latch LS/MS Write (Read Only)

This bit is set when the PC/XT/AT writes to the Divisor Latch Least Significant or Most Significant bytes. It is reset when the PC reads the LS/MS register(s). To determine which byte(s) have been written, the Z180 must read either LS or MS locations and then re-poll this bit. If only one location is interrupting, the interrupt is cleared when that location is read by the Z180.

Bit 0 FIFO Control Register Write (Read Only)

This bit is set when the PC/XT/AT writes to the FCR. This bit is also set when Transmit occurs. It is reset when the Z180 MPU reads this register.

Interrupt Enable Register

The IE Register allows each of the 16550/8250 interrupts to the Z180™ MPU to be masked off individually or globally.

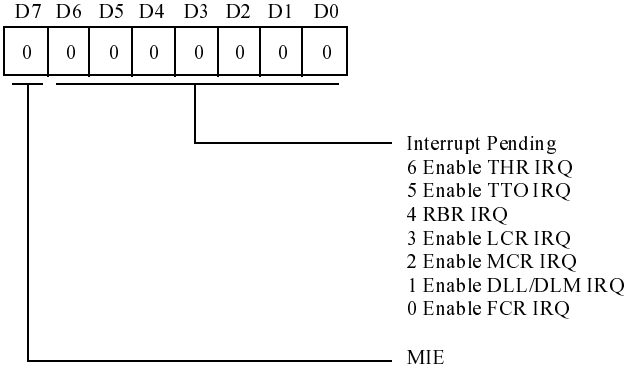


Figure 40. IE Register (Z180 MPU, Address xxFDH)

Bit 7 Master Interrupt Enable (Read/Write)

If bit 7 is 0, all interrupts from the 16550 MIMIC are masked off. If this bit is 1, then interrupts are enabled individually by setting the appropriate bit.

Bit 6 Enable THR Interrupt (Read/Write)

If this bit is 1, it enables the Transmit Holding Register Interrupt.

Bit 5 Enable TTO Interrupt (Read/Write)

If this bit is 1, it enables the Transmitter Timeout Interrupt. This interrupts the CPU when characters remain in the FIFO below the trigger level and the FIFO is not read or written for the length of time in the transmitter timeout register.

Bit 4 Enable RBR Interrupt (Read/Write)

If this bit is 1, it enables the Receive Buffer Register Interrupt.

Bit 3 Enable LCR Interrupt (Read/Write)

If this bit is 1, it enables the Line Control Register interrupt.

Bit 2 Enable MCR Interrupt (Read/Write)

If this bit is 1, it enables the Modem Control Register Interrupt.

Bit 1 Enable DLL/DLM Interrupt (Read/Write)

If this bit is 1, it enables the Divisor Latch Least and Most Significant Byte interrupts.

Bit 0 Enable FCR Interrupt (Read/Write)

If this bit is 1, then interrupts are enabled for a PC write to the FIFO control register (FCR) or for occurrence of Tx Overrun.

Priority of interrupts are in this order:

(Highest)	6	THR IRQ
	5	TTO IRQ
	4	RBR IRQ
	3	MCR IRQ
	2	LCR IRQ
	1	DLL IRO
	1	DLM IRQ
(Lowest)	0	FCR or Tx OVERRUN IRQ

Interrupt Vector Register

The Interrupt Vector Register contains either the opcode (Z180 Interrupt Mode 0) or the modified vector used as the lower address for a Z180 interrupt service routine (Z180 Interrupt Mode 2), depending upon the VIS bit in the MMC Register (MIMIC Master Control Register). If the VIS bit is 0, then Z180 Mode 0 interrupt is selected; if VIS is 1, then Z180 Mode 2 is selected. Note that in Z180 Interrupt Mode 0, the data input to the MPU during the interrupt acknowledge cycle is an instruction opcode; in Z180 Interrupt Mode 2, this data (modified depending on the source of the interrupt) becomes part of an address from which to get the starting address of the interrupt service routine.

Bits 7-4 Upper Nibble IVEC (Read/Write)

These four bits generate either an opcode for Z180 Interrupt Mode 0, or the upper four bits of the interrupt modified vector used as an 8-bit address to support the Z180 Interrupt Mode 2. These bits are read/write and always read back what was last written to them.

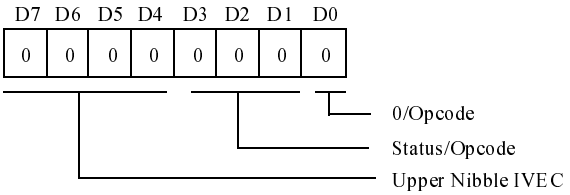


Figure 41. IVEC Register (Z180 MPU, Address xxFCH)

Bits 3-1 Interrupt Modified Vector/Opcode (Read/Write Table 21)

These three bits are the Interrupt Status bits when VIS in the MMC register is 1 (Z180 Interrupt Mode 2). If VIS bit is 0, then this field contains bit 3-bit 1 of the opcode. If the VIS bit is 0, then these bits contain what was last written to them.

Table 24. Interrupt Status Bits

Bits 3, 2, 1	Interrupt Request
000	NO IRQ
001	FCR or Tx OVRN IRQ
010	DLL/DLM IRQ
011	LCR IRQ[1]
100	MCR IRQ[1]
101	RBR IRQ
110	TTO IRQ
111	THR IRQ

NOTES:
1. The order of LCR and MCR does not follow that of the IE Register.

Bit 0 0/Opcode (Read/Write)

This bit is always 0 when the VIS bit is 1. If the VIS bit is 0, this bit reads back what was last written to it.

The Interrupt Vector Register serves both interrupt modes. When the VIS bit is 0, the last value written to the register can be read back. If the VIS bit is 1, and an interrupt is pending, the value read is the last value written to the upper nibble plus the status for the interrupt that is pending. If no interrupt is pending, then the last value written to the upper nibble plus the lower nibble is read from the register.

If the vector includes the status, then the lower four bits of the vector change asynchronously depending on the interrupting source. Since this vector changes asynchronously, then the interrupt service routine to read the IVEC register might read the source of the most recent IRQ/INTACK cycle if that IRQ does not have its IUS set.

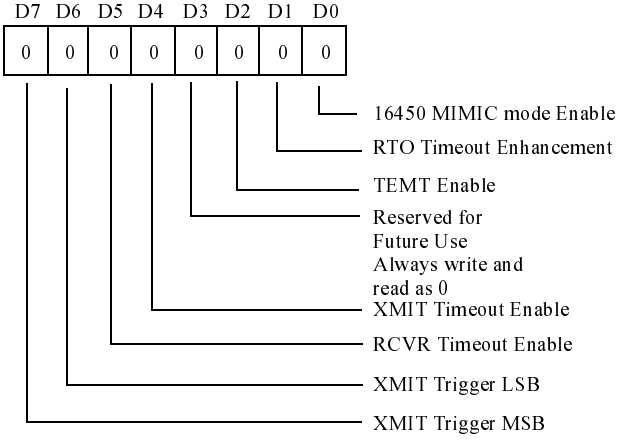


Figure 42. FIFO Status and Control Register (Z180 MPU Read/Write, Address xxECH)

Bit 7 and Bit 6 XMIT Trigger MSB,LSB

This field determines the number of bytes available to read in the transmitter FIFO before an interrupt occurs to the MPU (Table 22).

Table 25. Transmitter Trigger Level

b7	b6	Level (# bytes)
0	0	1
0	1	4
1	0	8
1	1	14

Bit 5 Receive Timeout Enable

This bit enables the Z80182/Z8L182 Receive Timeout Timer that is used to emulate the four character timeout delay that is specified by the 16550. If no read or write to the RCVR FIFO has taken place and data bytes are available, but are below the PC trigger level. If this timer reaches zero, an interrupt is sent to the PC.

Bit 4 Transmitter Timeout Enable

This bit enables the Z80182/Z8L182 timer that is used to interrupt the Z180 MPU if characters are available, but are below the trigger level. The timer is enabled to count down if this bit is 1 and the number of bytes is below the set transmitter trigger level. The timer times out and interrupts the MPU if no read or write to the XMIT FIFO takes place within the timer interval.

Bit 3 Reserved. Program to zero.

Bit 2 (Reset value = 0) TEMT/Double Buffer

When enabled the Tx buffer can hold one extra byte (2 bytes total in 16450 mode). Do not enable in 16550 mode.

TEMT Emulation

If character delay emulation is not used the TEMT bit is automated. (Refer to “Z80182 MIMIC Double Buffering for the Transmitter” on page 116 for TEMT/Double Buffer information.)

Bit 1 RTO Timeout Enhancement

(Reset value = 0) Setting this bit enables the RTO timeout to emulate the 16550 device. When enabling this feature, the receive timeout timer does not begin counting down until the character emulation timer for each byte of data in the Rx FIFO has expired.

Bit 0 16450 MIMIC Mode Enable

(Reset value--O) This bit =1 forces the MIMIC into 16450 mode. Bit 0 in the FCR reg is forced to zero as well as the mimic internal FIFO enable. When used, this bit must be programmed at MIMIC initialization and not modified afterwards.

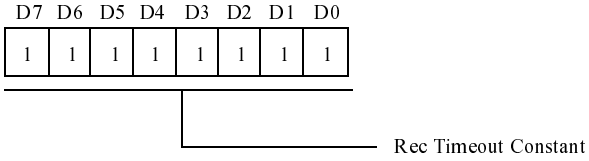


Figure 43. Receive Timeout Timer Constant (Z180 MPU Read/Write, Address xxEAH)

This register contains an 8-bit constant for emulation of the 16550 four character timeout feature. Software must determine the value to load into this register based on the bit rate and word length specified by the MIMIC interface with the PC. This timer receives its input from the $\overline{\text{TRxCB}}$ Clock of the ESCC. This timer is enabled to down count when the enable bit in the FSR register is set and the trigger level interrupt has not been activated on the RCVR FIFO. The counter reloads and counts down each time there is a read or write to the RCVR FIFO.

The receive timeout timer is enhanced to emulate the actual 16550 when bit 1 of the FIFO status and control register is enabled. Under most circumstances, this register must be programmed for four character timers (40d,8-N-1).

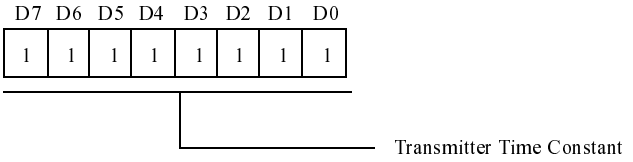


Figure 44. Transmit Timeout Timer Constant (Z180 MPU Read/Write, Address xxEBH)

This register contains an 8-bit constant for determining the interval for the Transmit Timeout Timer. If allowed to decrement to zero, this timer interrupts the MPU by setting the THR bit in the IUS/IP register. This timer receives its input from the $\overline{\text{TRxCB}}$ Clock of the SCC. The timer is enabled to down count when the enable bit in the FSR register is set and the trigger level has not been reached on the XMIT FIFO. The counter reloads each time there is a read or write to the XMIT FIFO.

Transmit And Receive Timers

Because of the speed at which data transfers can take place between the Z180™ MPU and the PC/XT/AT, two timers have been added to alleviate any software problems that a high speed parallel data transfer might cause. These timers allow the programmer to slow down the data transfer just as if the 16550 MIMIC interface had to shift the data in and out serially. The Timers receive their input from the $\overline{\text{TRxCB}}$ Clock since, in 16550 MIMIC mode, the ESCC channel B is disabled. For example, the clock source for the 8-bit registers: RTTC (Receive Timeout Time Constant, xxEAH), TTTC (Transmit Timeout Time Constant, xxEBH), TTCR (Transmit Time Constant Register, xxFAH) and RTCR (Receive Time Constant Register, xxFBH) uses the $\overline{\text{TRxCB}}$ Clock output. The $\overline{\text{TRxCB}}$ Clock output needs to be generated by the ESCC's channel B's 16-bit BRG as its clock source, thus allowing the programmer to access a total of 24 bits as a timer to slow down the data transfer.

In most cases, ESCC Ch. B BRG must be programmed to output at a frequency equivalent to the desired serial transfer rate. Route the output of the BRG to the $\overline{\text{TRxCB}}$ pin.

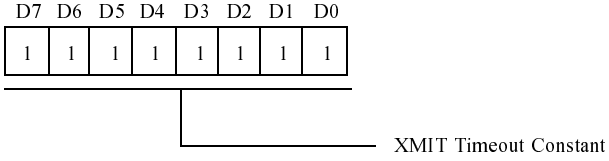


Figure 45. Transmitter Time Constant Register (Z180 MPU Read/Write, Address xxFAH)

When a write from the PC/XT/AT is made to the Transmit Holding Register, an interrupt to the Z180 MPU is generated. The Z180 MPU then reads the data in the Transmit Holding Register. Upon this read, if the Transmitter timer is enabled, the time constant from the Transmitter Time Constant Register is loaded into the Transmitter timer and enables the

count. After the timer reaches a count of zero the Transmit Holding Register Empty bit is set. However, the above is only true when the PC/XT/AT is reading the Transmit Holding Register Empty bit. To allow the Z180 MPU to know that it has already read the byte of data, immediately following a read from the Transmit Holding Register, a mirrored Transmit Holding Register, Empty bit is set. This mirrored bit is always read back to the Z180 MPU when it reads the Line Status Register.

If the transmitter timer is not enabled when the Z180 MPU reads the Transmit Holding Register, both Transmit Holding Register Empty bits are set immediately. In FIFO mode of operation, the effect is similar as the status to PC is always delayed such that a PC interrupt for empty FIFO does not occur before the time required for each character read from the FIFO by the Z180 has elapsed. The effect is that the PC does not detect data requests from an empty FIFO any faster than would occur with a true UART when the delay feature is enabled. This timer also delays data transfer for TSR buffer to Z80182 THR in double buffer mode.

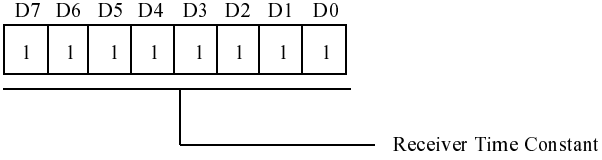


Figure 46. Receive Time Constant Register (Z180 MPU Read/Write, Address xxFBH)

When the Z180™ MPU writes to the Receive Buffer register and the Receive Timer is enabled, the Receive Timer is loaded with the Receive Time Constant, the timer is enabled and counts down to zero. When the timer reaches zero, the Data Ready bit in the Line Status Register is set. As with the Transmit Timer, the Data Ready bit is also mirrored. Immediately upon a write to the Receive Buffer, the mirrored bit is set to let the Z180 MPU know that the byte has already been written. If the timer is not enabled, then both Data Ready bits are set immediately upon

a write to the Receive Buffer. The FIFO mode of operation is similar in that the status to the PC is always delayed by the time required for each character written to the FIFO by the Z180. The effect is that the PC does not detect a FIFO trigger level or DMA request faster than would occur with a true UART when the delay feature is enabled.

16550 MIMIC Registers

The Z80182/Z8L182 contains the following set of registers for interfacing with the PC/XT/AT.

- Receive Buffer Register
- Transmit Holding Register
- Interrupt Enable Register
- Interrupt Identification Register
- FIFO Control Register
- Line Control Register
- Modem Control Register
- Line Status Register
- Modem Status Register
- Scratch Register
- Divisor Latch Least/Most Significant Bytes
- FIFO Control Register

These registers emulate the 16550 UART and enable the PC/XT/AT to interface with them as with an actual 16550 UART. This emulation allows the Z80182/Z8L182 to be software compatible with existing modem software.

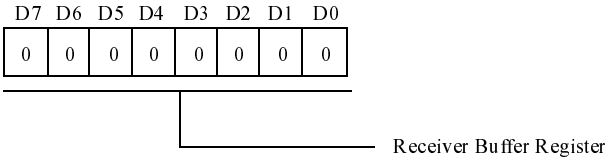


Figure 47. Receive Buffer Register
(PC Read Only, Address 00H, DLAB = 0, R/W = Read)
(Z180™ MPU Write Only, Address XXF0H)

Receive Buffer Register

When the Z180 has assembled a byte of data to pass to the PC/XT/AT, it places it in the Receive Buffer Register. If the Received Data Available interrupt is enabled then an interrupt is generated for the PC/XT/AT and the Data Ready bit is set (if the Receive Timer is enabled, the interrupt and setting of the Data Ready bit is delayed until after the timer times out). Also the shadowed bits of the Line Status Register are transferred to their respective bits when the Z180 MPU writes to the Receive Buffer Register (See Line Status Register Bits 1, 2, 3 and 4). This allows a simultaneous setting of error bits when the data is written to the Receive Buffer Register. In FIFO, mode this address reads (PC) and writes (Z180) the Receive FIFO.

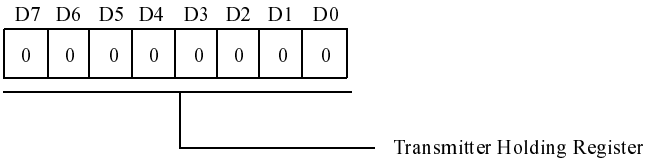


Figure 48. Transmit Holding Register
(PC Write Only, Address 00H, DLAB = 0, R/$\overline{W}$ = Write)
(Z180 MPU Read Only, Address xxF0H)

Transmit Holding Register

When the PC/XT/AT writes to the Transmit Holding Register, the Z80182/Z8L182 responds by setting the appropriate bit in the IP register and by generating an interrupt to the Z180 MPU if it is enabled. When the Z180 MPU reads this register the Transmit Holding Register empty flag is set (if the transmitter timer is enabled, this bit is set after the timer times out). In FIFO mode of operation, this address is used to read (Z180) and write (PC) the Transmitter FIFO.

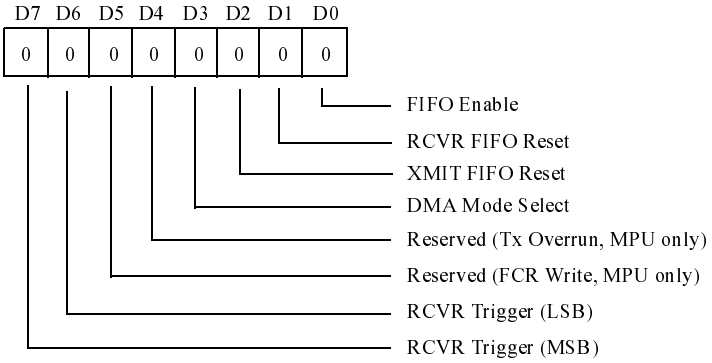


Figure 49. FIFO Control Register (PC Write Only, Address 02H) (Z180 MPU Read Only, Address xxE9H)

FIFO Control Register

Bit 6 and Bit 7 RCVR trigger LSB and MSB bits

This 2-bit field determines the number of available bytes in the receiver FIFO before an interrupt to the PC occurs (see Table 26).

Bit 4 and Bit 5

Reserved for future use (PC side). Note: From the MPU side, bit 4 and bit 5 flags two sources of interrupts. Bit 5 is a FIFO interrupt indicating that the FCR had changed; bit 4 is a Tx overrun interrupt, indicating transmit overrun. A read of the FCR from the MCU side clears a previously set bit 4 or bit 5.

Bit 3 DMA Mode Select

Setting this bit to 1 causes the MIMIC DMA mode to change from mode 0 to mode 1 (if bit 0 is 1, FIFO mode is enabled). This affects the DMA mode of the FIFO. A 1 in this bit enables multi-byte DMA). Bit 2 XMIT FIFO Reset Setting this bit to 1 causes the transmitter FIFO pointer logic to be reset; any data in the FIFO is lost. This bit is self clearing; however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 1 RCVR FIFO Reset

Setting this bit to 1 causes the receiver FIFO pointer logic to be reset; any data in the FIFO is lost. This bit is self clearing, however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 0 FIFO Enable

The PC writes this bit to logic 1 to put the 16550 MIMIC into FIFO mode. This bit must be 1 when writing to the other bits in this register or they can not be programmed. When this bit changes state, any data in the FIFO's or transmitter holding and Receive Buffer Registers is lost and any pending interrupts are cleared. This feature can be forced in a disabled state by the MPU.

This bit is disabled by default.

Table 26. Receive Trigger Level

b7	b6	Trigger Level, Number of Bytes
0	0	1
0	1	4
1	0	8
1	1	14

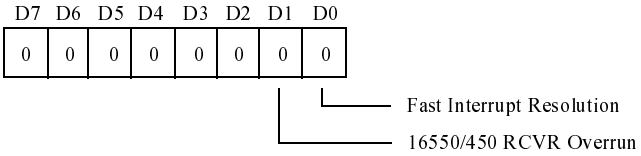


Figure 50. MIMIC Modification Register (Z180 MPU Write only, Address xxE9h)

Bit 7-2 Reserved. Program to zero.

Bit 1 RCVR Overrun Modification

The actual 16450/16550 device allows the last position in FIFO to be overwritten by DCE during receiver overrun condition. When this bit is enabled (programmed to 1) the last position in FIFO can be overwritten by Z180 during receiver overrun. This feature is disabled by default. When this modification is not enabled, the MIMIC ignores any write to RBR during an overrun condition.

Bit 0 Fast MIMIC-ESCC Interrupt Resolution

When enabling this modification, the internal MIMIC IEO signal into the ESCC IEI input is forced Low when the MIMIC Interrupt line becomes active. This is required to prevent the ESCC from putting its vector on the databus during an INTACK cycle (given that the MIMIC is programmed to have higher interrupt priority).

When disabled, the internal MIMIC IEO becomes deasserted only after an interrupt acknowledge cycle. In this case, it is possible for the ESCC to force its interrupt vector onto the data bus even when the MIMIC has a pending interrupt and is higher in priority. MIMIC and ESCC interrupts.

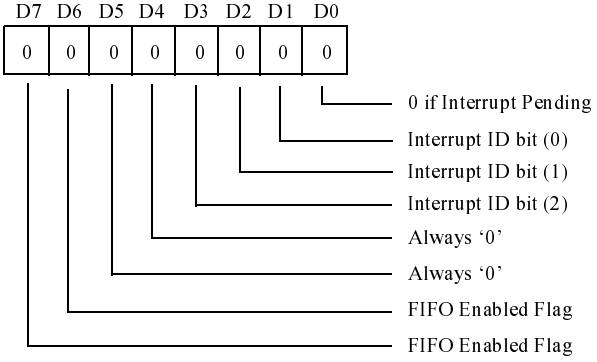


Figure 51. Interrupt Identification Register (PC Read Only, Address 02H) (Z180 MPU no access)

Interrupt Identification Register

Bit 7 and Bit 6 FIFO’s Enabled

These bits read 1 if the FIFO mode is enabled on the MIMIC.

Bit 5 and Bit 4 Always Read 0

Reserved bits.

Bits 3-1 Interrupt ID Bits

This 3-bit field determines the highest priority interrupt pending (see Table 27).

Bit 0 Interrupt Pending

This bit is logic 0 and interrupt is pending. When the PC accesses the IIR, the contents of the register and all pending interrupts are frozen. Any new interrupts are recorded, but not acknowledged, during the IIR access.

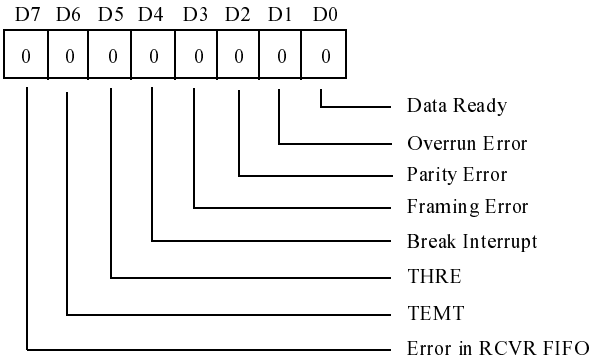


Figure 52. Line Status Register (PC Read Only, Address 05H) (Z180 MPU Read/Write bits 6, 4, 3, 2, Address xxF5H)

Table 27. Interrupt Identification Field

b3	b2	b1	Priority	Interrupt Source	INT Reset Control
0	1	1	Highest	Overrun, Parity, Framing error or Break detect bits set by MPU	Read Line Status Register
0	1	0	2nd	Received Data trigger level	RCVR FIFO drops below trigger level
1	1	0	2nd	Receiver Timeout with data in RCVR FIFO.	Read RCVR FIFO
0	0	1	3rd	Transmitter Holding Register is Empty.	Writing to the Transmitter Holding Register or reading the Interrupt Identification Register when the THRE is the source of the interrupt.
0	0	0	4th	MODEM status: CTS, DSR, RI or DCD	Reading the MODEM status register.

Line Status Register

Bit 7 Error in RCVR FIFO

In 16450 mode, this bit reads logic 0. In 16550 mode this bit is set if at least one data byte is available in the FIFO with one of its associated error bits set. This bit clears when there are no more errors (or break detects) in the FIFO.

Bit 6 Transmitter Empty

This bit must be set or reset by the MPU by a write to this register bit. If Double Buffer Mode is enabled, the TEMT bit is set/reset automatically. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to “Z80182 MIMIC Double Buffering for the Transmitter” on page 116 for TEMT/Double Buffer information.

Bit 5 Transmit Holding Register Empty, THRE

This bit is set to 1 when either the THR has been read (emptied) by the MPU (16450 mode) or the XMIT FIFO is empty (16550 mode). This bit is set to 0 when either the THR or XMIT FIFO become non-empty. A shadow bit exists so that the register bit setting to 1 is delayed by the Transmitter Timer if enabled. The MPU when reading this bit does not detect the delay. Both shadow and register bits are cleared when the PC writes to the THR of XMIT FIFO. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to “Z80182 MIMIC Double Buffering for the Transmitter” on page 116 for TEMT/ Double Buffer information.

Bit 2, 3, 4 Parity Error, Framing Error, Break Detect

These bits are written, indirectly, by the MPU as follows: The bits are first written to shadow bit locations when the MPU write accesses the LSR. When the next character is written to the Receive Buffer or RCVR FIFO, the data in the shadow bits is then copied to the LSR (16450 mode) or FIFO RAM (16550 mode). In FIFO mode bits become available to the PC when the data byte associated with the bits is next to be read (top of FIFO). In FIFO mode, with successive reads of the receiver, the status bits are set if an error occurs on any byte. After the MPU writes to the Receive Buffer or RCVR FIFO, the shadow bits are auto cleared. The register bits are cleared upon the PC reading the LSR. In FIFO mode these bits are set if any byte has the respective error bit set while the PC reads multiple characters from the FIFO.

Bit 1 Overrun Error

This bit is set if the Z180 MPU makes a second write to the Receive Buffer before the PC reads the data in the Buffer (16450 mode) or with a full RCVR FIFO (16550 mode.) No data transfers to the RCVR FIFO under these circumstances. This bit is reset when the PC reads the Line Status Register.

Bit 0 Data Ready

This bit is set to 1 when received data is available, either in the RCVR FIFO (16550 mode) or Receive Buffer Register (16450 mode). This bit is set immediately upon the MPU writing data to the Receive Buffer or FIFO if the Receive Timer is not enabled but is delayed by the timer interval if the Receive Timer is enabled. For MPU read access a shadow bit exists so that the MPU does not see the delay the PC does. Both bits are cleared to logic zero immediately upon reading all the data in either the Receive Buffer or FIFO.

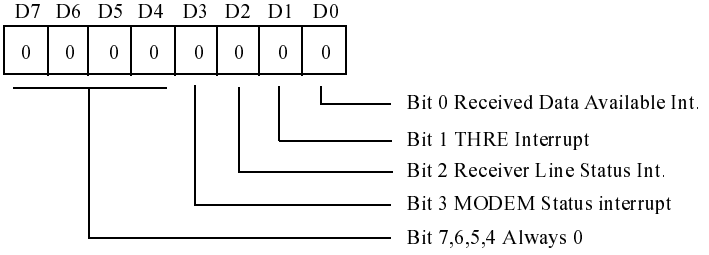


Figure 53. Interrupt Enable Register (PC Read/Write, Address 01H) (Z180 MPU Read Only, Address xxF1H)

Interrupt Enable Register

Bits 7, 6, 5, 4 Reserved These bits are always read 0 (PC and MPU).

Bit 3 Modem Status IRQ

If bits 0, 1, 2 or 3 of the Modem Status Register are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 2 Receive Line Status IRQ

If bits 1, 2, 3 or 4 of the LSR are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 1 Transmit Holding Register Empty IRQ

If bit 5 of the LSR is set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 0 Received Data Available IRQ

An interrupt to the PC is generated if bit 0 of the LSR is set or a Receive Timeout occurs and this enable bit is a logic 1.

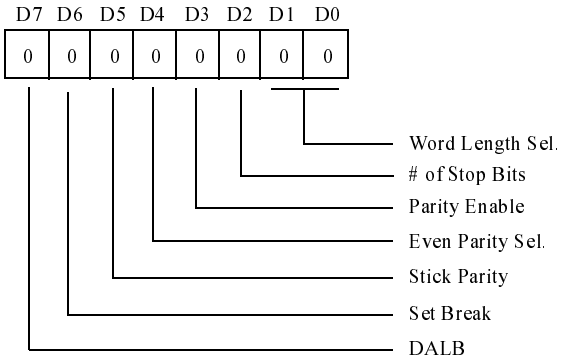


Figure 54. Line Control Register (PC Read/Write, Address 03H) (Z180 MPU Read Only, Address xcF3H)

Line Control Register

Bit 7 Divisor Latch Access Bit (DALB)

This bit allows access to the divisor latch by the PC/XT/AT. If this bit is set to 1, access to the Transmitter, Receiver and Interrupt Enable

Registers is disabled. When an access is made to address 0 the Divisor Latch Least Significant byte is accessed. If an access is made to address 1, the Divisor Latch Most Significant byte is accessed.

Bit 6-Bit 0

These bits do not affect the Z80182/Z8L182 directly, however they can be read by the Z180 MPU and the 16550 MIMIC modes can be emulated by the Z180 MPU.

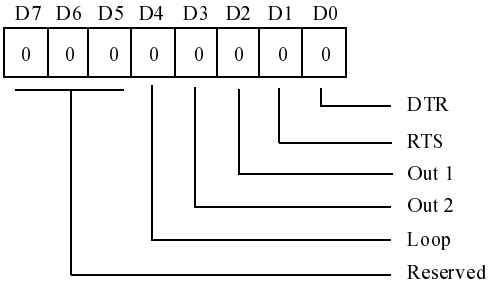


Figure 55. Modem Control Register (PC Read/Write, Address 04H) (Z180 MPU Read Only, Address xxF4H)

Modem Control Register

Bit 7-5 Reserved

Reserved for future use, always 0.

Bit 4 Loop

When this bit is set to 1, D3-D0 field reflects the status of Modem Status Register, as follows:

RI = Out 1

DCD = Out 2

DSR = DTR

CTS = RTS

Emulation of the 16550 UART loop back feature must be done by the Z180 MPU, except in the above conditions.

Bit 3 Out 2

This bit controls the tristate on the HINTR pin if bits 2 and 1 are 10. Otherwise it can be read by the Z180 MPU.

Bits 2, 1, 0

These bits have no direct control of the 16550 MIMIC interface and the Z180 MPU must emulate the function if it is to be implemented.

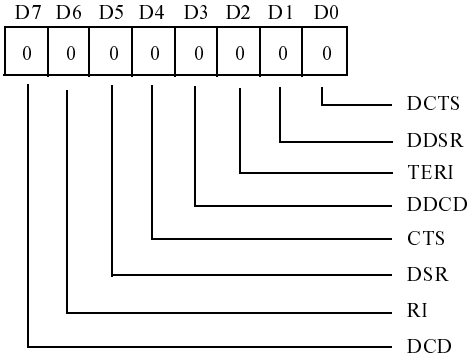


Figure 56. Modem Status Register (PC Read Only, Address 06H) (Z180 MPU Read/Write bits 7-4, Address xxF6H)

Modem Status Register

Bit 7 Data Carrier Detect

This bit must be written by the Z180 MPU.

Bit 6 Ring Indicator

This bit must be written by the Z180 MPU.

Bit 5 Data Set Ready

This bit must be written by the Z180 MPU.

Bit 4 Clear to Send

This bit must be written by the Z180MPU.

Bit 3 Delta Data Carrier Detect

This bit is set to 1 whenever the Data Carrier Detect bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

Bit 2 Trailing Edge Ring Indicator

This bit is set to 1 on the falling edge of the Ring Indicator bit. This bit is reset when the PC/XT/AT reads the Modem Status Register.

Bit 1 Delta Data Set Ready

This bit is set to 1 whenever the Data Set Ready bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

Bit 0 Delta Clear To Send

This bit is set to 1 whenever the Clear To Send bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

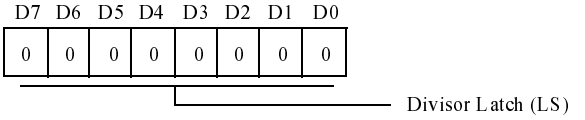


Figure 57. Scratch Register (PC Read/Write, Address 07H) (Z180 MPU Read Only, Address xxF7H)

Scratch Register

Bits 7-0 Scratch Register

This register is used by the PC/XT/AT programmer for temporary data storage. The Z180 MPU is able to read this register. If the PC/XT/AT writes to this register, no interrupt to the Z180 MPU is generated.

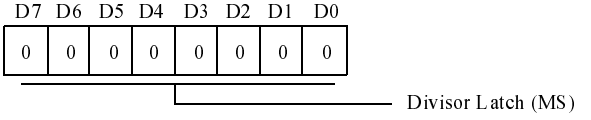


Figure 58. Divisor Latch (LS) (PC Read/Write, Address 00H and DLAB=1) (Z180 MPU Read Only, Address xxF8H)

Divisor Latch (LS)

Bit 7-0 Divisor Latch Most Significant Byte (MS)

This register contains the Low order byte of the Baud rate divisor. Writing to this register with the PC/XT/AT generates an interrupt to the Z180 MPU. It next reads the Baud rate divisor and sets up the application.

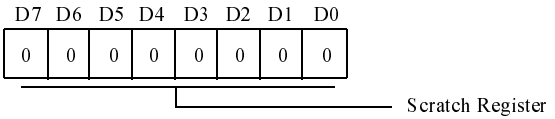


Figure 59. Divisor Latch (MS) (PC Read/Write, Address 01H and DLAB=1) (Z180 MPU Read Only, Address xxF9H)

Divisor Latch (MS)

Bit 7-0 Divisor Latch Most Significant Byte (MS)

This register contains the High order byte of the Baud rate divisor. Writing to this register with the PC/XT/AT generates an interrupt to the Z180 MPU. It next reads the Baud rate divisor and sets up the application.

Programming Considerations

Z80182/Z8L182 MIMIC SYNCHRONIZATION

Because of the asynchronous nature of the FIFO's on the MIMIC, some synchronization plan must be provided to prevent conflict from the dual port accesses of the MPU and the PC.

To solve this problem, I/O to the FIFO is buffered and the buffers allow both PC and MPU to access the FIFO asynchronously. Read and Write requests are then synchronized by means of the MPU clock. Incoming signals are buffered in such a way that metastable input levels are stabilized to valid 1 or 0 levels. Actual transfers to and from the buffers, from and to the FIFO memory, are timed by the MPU clock. ALU evaluation is performed on a different phase than the transfer to ensure stable pointer values.

Another potential problem is that of simultaneous access of the MPU and PC to any of the various 'mailbox' type registers. This problem is solved by dual buffering of the various read/write registers. During a read access by either the MPU or PC to a mailbox register, the data in the output or slave portion of the buffered register is not permitted to change. Any write that might take place during this time are stored in the input of master part of the register. The corresponding status/interrupt is reset appropriately based on the write having followed the read to the register. For example, the IUS/IP bit for the LCR write is not be cleared by the MPU read of the LCR if a simultaneous write to the LCR by the PC takes place. Instead the LSR data changes after the read access and IUS/IP bit 3 remains at logic 1.

Z80182 MIMIC DOUBLE BUFFERING FOR THE TRANSMITTER

The Z80182 implements double buffering for the transmitter in 16450 mode and sets the TEMT bit in the LSR Register automatically.

When this feature is enabled and character delay emulation is being used (see Figure 60):

1. The PC THRE bit in the LSR Register is set when the THR Register is empty;
2. PC Host writes to the 16450 THR Register;
3. Whenever the Z80182 TSR buffer is empty and one character delay timer is in a timed-out state, the byte from the THR Register is transferred to the TSR buffer; the timer is in timed-out state after FIFO Reset or after Host TEMT is set. This allows a dual write to THR when Host TEMT is set.
4. Restart character delay timer (timer reloads and counts down) with byte transfer from THR Register to the TSR buffer;
5. Whenever the TSR buffer is full, the TEMT bit in MPU LSR Register is reset with no delay;
6. MPU reads TSR buffer;
7. TEMT bit in LSR Register for MPU is set with no delay whenever the TSR buffer is empty;
8. When the TSR buffer is read by MPU and THR Register is empty and one character delay timer reaches zero, the TEMT bit in the LSR Register for Host is set from 0 to 1.

The PC THRE bit in the LSR Register is reset whenever the THR Register is full and set whenever THR Register is empty.

MPU IREQ and DMA Request for the transmit data is triggered whenever TSR buffer is full and cleared whenever TSR buffer is empty.

If character delay emulation is not used the TEMT bit in the LSR Register is set whenever both the THR Register and the TSR buffer are both empty. The Host TEMT bit is clear if there is data in either the TSR buffer of THR Register.

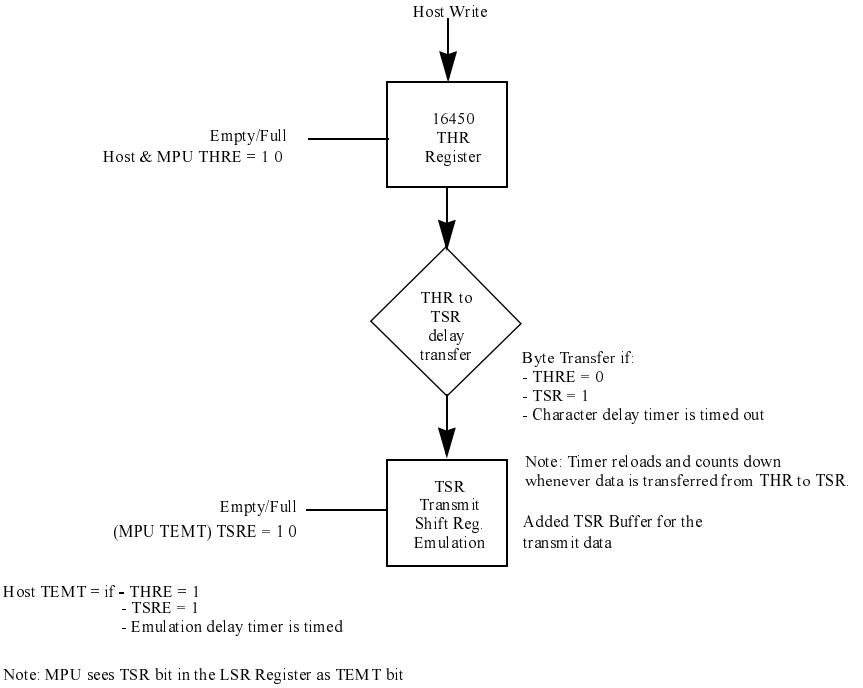


Figure 60. TEMT Emulation Logic Implementation

PARALLEL PORTS FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output (with the exception of PC6 and PC7 which are inputs only). The Ports are controlled through two registers: the Port Direction Control Register and the Port Data Register. (Please see register description for Ports A, B and C).

Programming

The following subsections explain and define the parameters for I/O Address assignments. The three tables in this section describe the mapping of the common registers shared by the MPU and the 16550 MIMIC. The MPU address refers to the I/O address as accessed from the MPU side (the Z180™ MPU interface side of the 16550 MIMIC). Note that only the lowest eight address lines are decoded for Z182 peripheral access. The full sixteen address lines are decoded for on-chip Z180 MPU access. The PC address (coined because the UART is common in PCs) is the address needed to access the MIMIC registers through the MIMIC interface signals. The MIMIC interface signals are multiplexed with the ESCC channel B and the Port A signals, and must be activated through the System Configuration Register and the Interrupt Edge/Pin MUX Register.

Table 28. Z80182/Z8L182 MPU Registers

Register Name	MPU Addr	PC Addr
Z80182/Z8L182 MPU Control Registers	0000H to 00x3FH (Relocatable to 0040H to 007FH or 0080H to 00BFH)	None

Table 29. Z80182/Z8L182 MIMIC Register MAP

Register Name	MPU Addr/Access[1]		PC Addr/Access	
MMC MIMIC Master Control Register	xxFFH	R/W	None	
IUS/IP Interrupt Pending	xxFEH	R/Wb7	None	
IE Interrupt Enable	xxFDH	R/W	None	
IVEC Interrupt Vector	xxFCH	R/W	None	
TTCR Transmit Time Constant	xxFAH	R/W	None	
RTCR Receive Time Constant	xxFBH	R/W	None	
FSCR FIFO Status and Control	xxECH	R/W7-4	None	
RTTC Receive Timeout Time Constant	xxEAH	R/W	None	
TTTC Transmit Timeout Time Constant	xxEBH	R/W	None	
RBR Receive Buffer Register	xxF0H	W only	00H	DLAB = 0, R only
THR Transmit Holding Register	xxF0H	R only	00H	DLAB = 0, W only
IER Interrupt Enable Register	xxF1H	R only	01H	DLAB = 0, R/W
IIR Interrupt Identification	None		02H	R only
FCR FIFO Control Register	xxE9H	R only	02H	W only
MM REGISTER xxE9H W only	None			
LCR Line Control Register	xxF3H	R only	03H	R/W
MCR Modem Control Register	xxF4H	R only	04H	R/W
LSR Line Status Register	xxF5H	R/Wb6432	05H	R only
MSR Modem Status Register	xxF6H	R/Wb7-4	06H	R only

Table 29. Z80182/Z8L182 MIMIC Register MAP (Continued)

Register Name	MPU Addr/Access[1]		PC Addr/Access	
SCR Scratch Register	xxF7H	R only	07H	R/W
DLL Divisor Latch (LSByte)	xxF8H	R only	00H	DLAB = 1, R/W
DLM Divisor Latch (MSByte)	xxF9H	R only	01H	DLAB = 1, R/W

NOTES:
1. "x" indicates don't care condition.

Table 30. Z80182/Z8L182 ESCC, PIA and MISC Registers

Register Name	MPU	Addr/Access	PC Addr/Access
WSG Chip Select Register	xxD8H	R/W	None
Z80182 Enhancements Register	xxD9H	R/W	None
PC Data Direction Register	xxDDH	R/W	None
PC Data Register	xxDEH	R/W	None
Interrupt Edge/Pin MUX Control	xxDFH	R/W	None
ESCC Chan A Control Register	xxE0H	R/W	None
ESCC Chan A Data Register	xxE1H	R/W	None
ESCC Chan B Control Register	xxE2H	R/W	None
ESCC Chan B Data Register	xxE3H	R/W	None
PB Data Direction Register	xxE4H	R/W	None
PB Data Register	xxE5H	R/W	None
RAMUBR RAM Upper Boundary Register	xxE6H	R/W	None
RAMLBR RAM Lower Boundary Register	xxE7H	R/W	None
ROM Address Boundary Register	xxE8H	R/W	None
PA Data Direction Register	xxEDH	R/W	None
PA Data Register	xxEEH	R/W	None
System Configuration Register	xxEFH	R/W	None
Clock Multiplier Register	xx1E	R/W	None
Revision Register	xxDA	R/W	None

Z182 MPU CONTROL REGISTERS

Figure 61 through Figure 64 refer to the Z80182/Z8L182 MPU Control registers. For additional information, refer to the Z8S180 Product Specification and Technical Manual.

ASCI Channels Control Registers

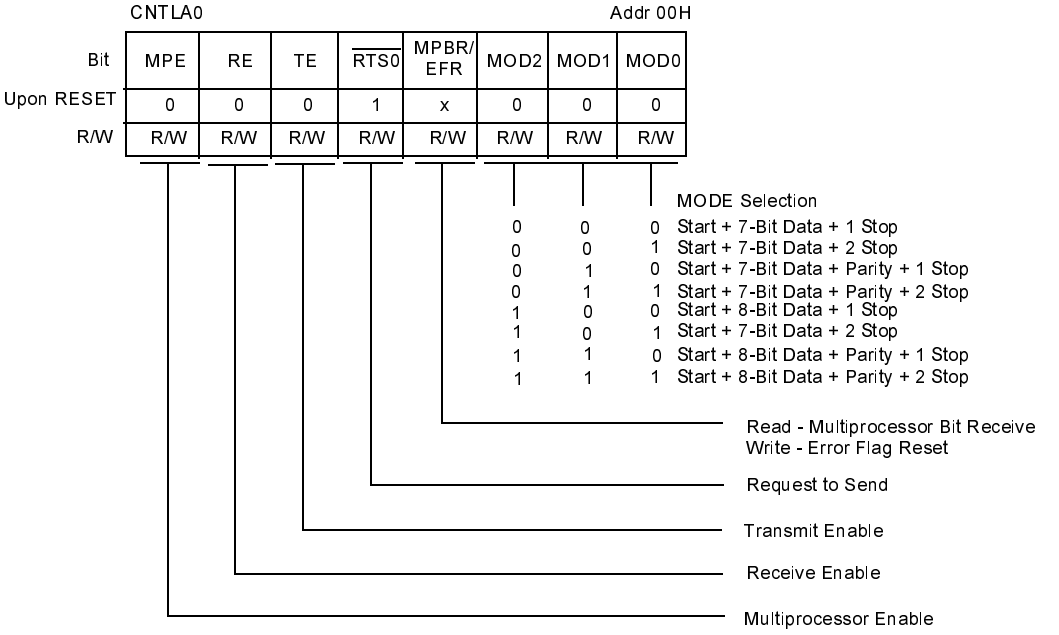


Figure 61. ASCI Control Register A (Ch. 0)

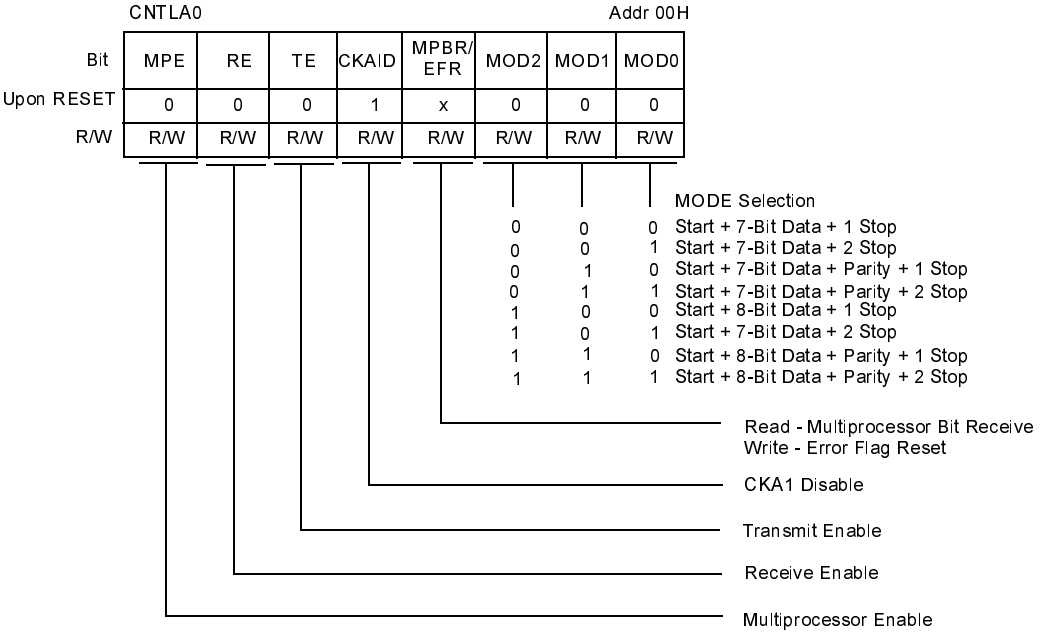


Figure 62. ASCI Control Register A (Ch. 0)

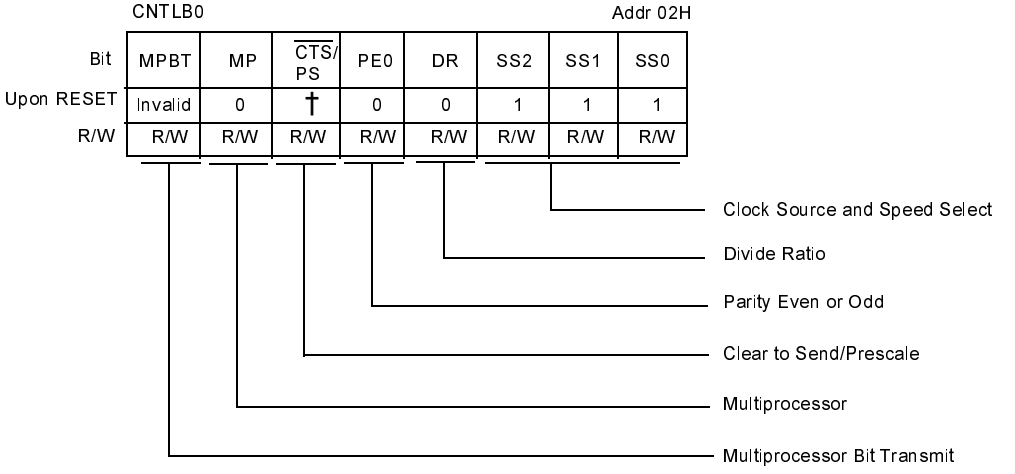


Figure 63. ASCI Control Register B (Ch. 0)

Table 31. ASCI Control Register B (Ch. 0)

General Divide Ratio	PS = 0 (Divide Ratio 10)		PS =1 = 30) (Divide Ratio =30)	
SS, 2, 1, 0	DR = 0 (x16)	DR =1 (x64)	DR = 0 (x16)	DR =1 (x64)
000	Ø 160	Ø 640	Ø 480	Ø 1920
001	Ø 320	Ø 1280	Ø 960	Ø 3840
010	Ø 640	Ø 2560	Ø 1920	Ø 7680
011	Ø 1280	Ø 5120	Ø 3840	Ø 15360
100	Ø 2560	Ø 10240	Ø 7680	Ø 30720

Table 31. ASCI Control Register B (Ch. 0) (Continued)

General Divide Ratio SS, 2, 1, 0	PS = 0 (Divide Ratio 10)		PS =1 = 30) (Divide Ratio =30)	
	DR = 0 (x16)	DR =1 (x64)	DR = 0 (x16)	DR =1 (x64)
101	Ø 5120	Ø 20480	Ø 15360	Ø 61440
110	Ø 10240	Ø 40960	Ø 30720	Ø 122880
111	External Clock (Frequency < Ø 40			

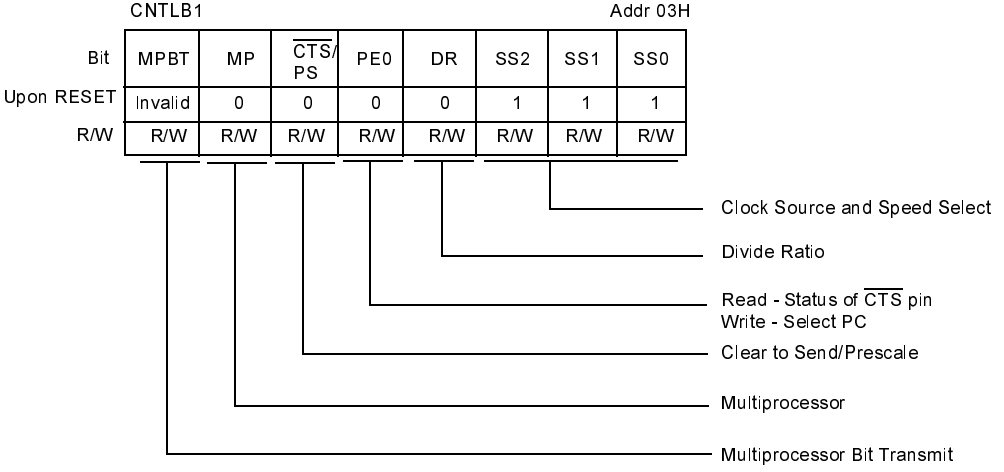


Figure 64. ASCI Control Register B (Ch. 1)

Table 32. ASCI Control Register B (Ch. 1)

General Divide Ratio	PS = 0 (Divide Ratio 10)		PS =1 = 30) (Divide Ratio =30)	
SS, 2, 1, 0	DR = 0 (x16)	DR =1 (x64)	DR = 0 (x16)	DR =1 (x64)
000	Ø 160	Ø 640	Ø 480	Ø 1920
001	Ø 320	Ø 1280	Ø 960	Ø 3840
010	Ø 640	Ø 2560	Ø 1920	Ø 7680
011	Ø 1280	Ø 5120	Ø 3840	Ø 15360
100	Ø 2560	Ø 10240	Ø 7680	Ø 30720
101	Ø 5120	Ø 20480	Ø 15360	Ø 61440
110	Ø 10240	Ø 40960	Ø 30720	Ø 122880
111[1]	External Clock (Frequency < Ø40)			

NOTES:
1. Baud rate is external clock rate 16; therefore, 0 (40 x 16) is maximum baud rate using external clocking.

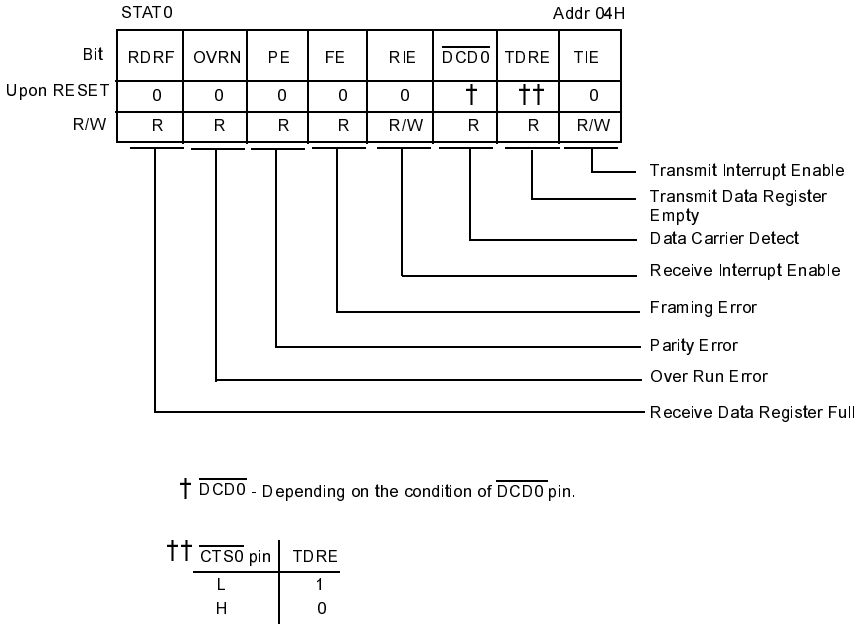


Figure 65. ASCI Status Register

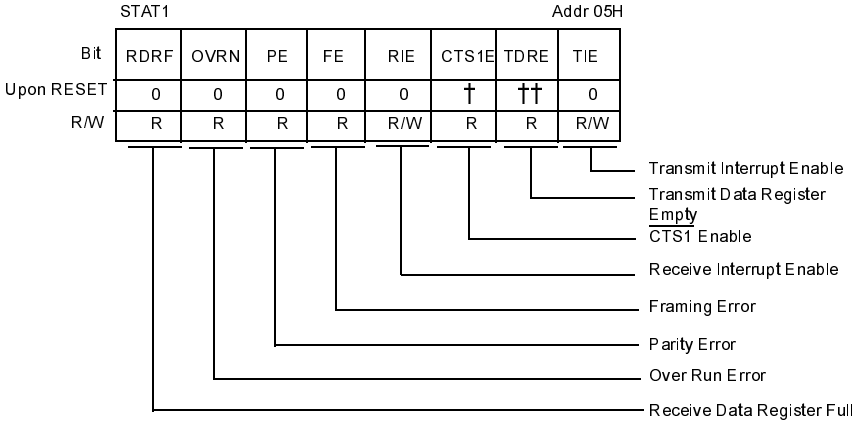


Figure 66. ASCI Status Register (Ch. 1)

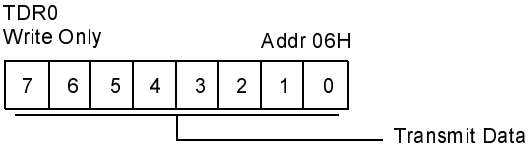


Figure 67. ASCI Transmit Data Register (Ch. 0)

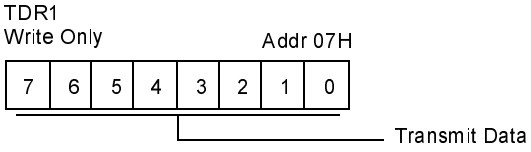


Figure 68. ASCI Transmit Data Register (Ch. 1)

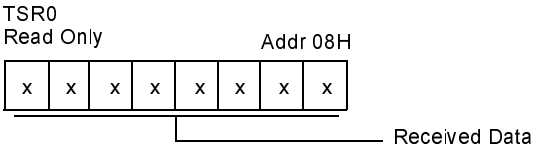


Figure 69. ASCI Receive Data Register (Ch. 0)

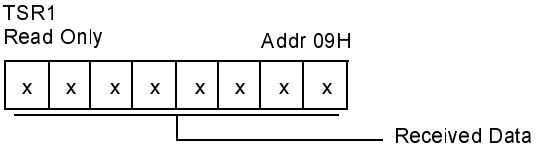


Figure 70. ASCI Receive Data Register (Ch. 1)

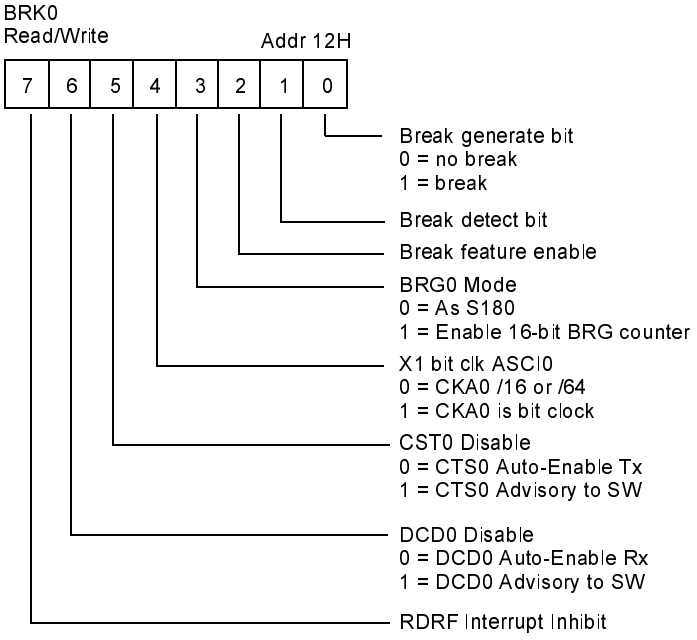


Figure 71. ASCI Break Control Register (Ch. 0)

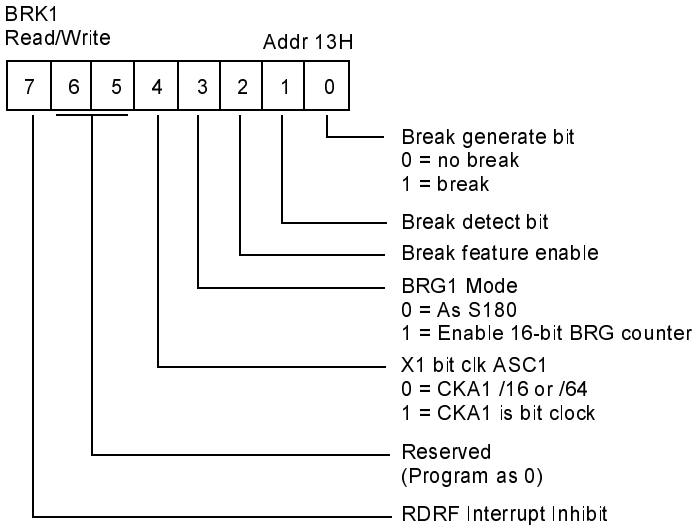


Figure 72. ASCI Break Control Register (Ch. 1)

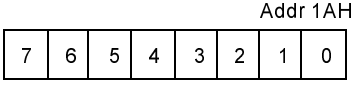


Figure 73. ASCI0 Time Constant Low

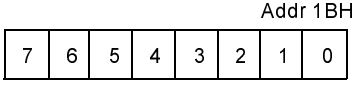


Figure 74. ASCI0 Time Constant High

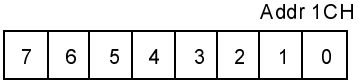


Figure 75. ASCI1 Time Constant Low

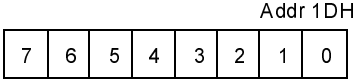


Figure 76. ASCI1 Time Constant High

CSI/O Registers SS2

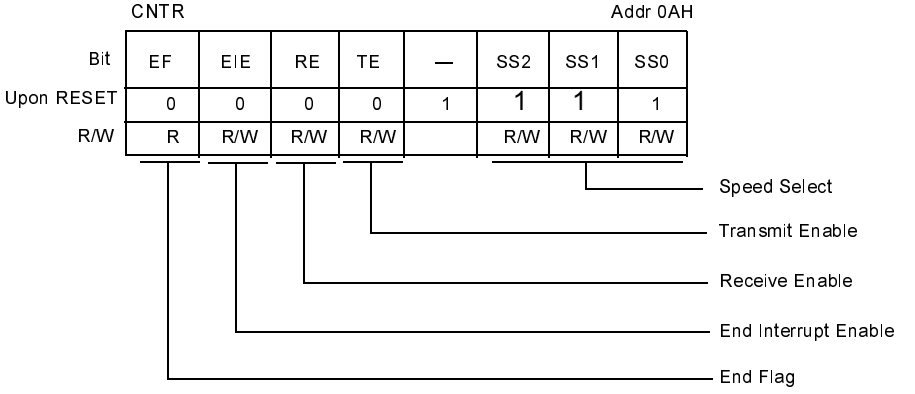


Figure 77. CSI/O Control Register

Table 33. CSI/O Control Register

SS2, 1,0	Baud Rate	SS2, 1, 0	Baud Rate
000	Ø 20	100	Ø 320
001	Ø 40	101	Ø 640
010	Ø 80	110	Ø 1280
011	Ø 100	111	External Clock (Frequency < 0 20)

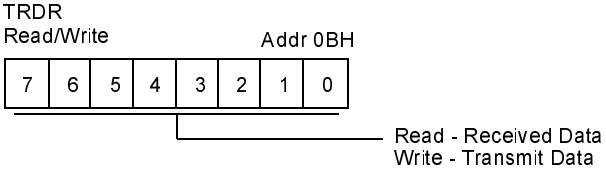


Figure 78. CSI/O Transmit/Receive Data Register

Timer Data Registers

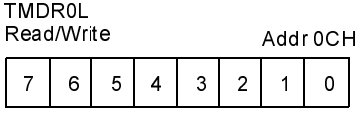


Figure 79. Timer 0 Data Register L

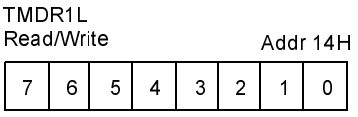


Figure 80. Timer 1 Data Register L

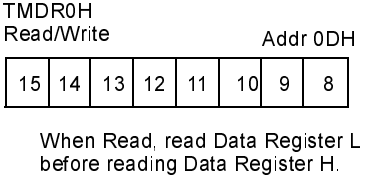


Figure 81. Timer 0 Data Register H

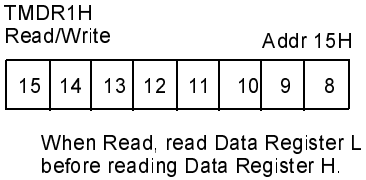


Figure 82. Timer 1 Data Register H

Timer Reload Registers

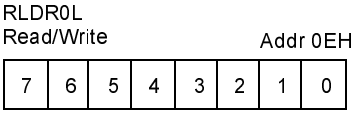


Figure 83. Timer 0 Reload Register L

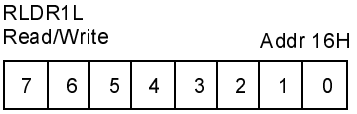


Figure 84. Timer 1 Reload Register L

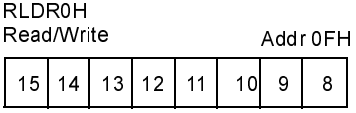


Figure 85. Timer 0 Reload Register H

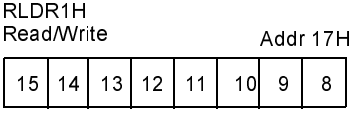


Figure 86. Timer 1 Reload Register H

Timer Control Register

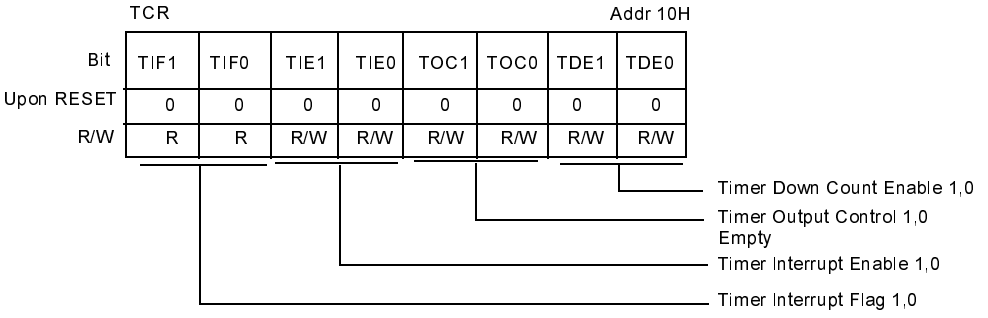


Figure 87. Timer Control Register

Table 34. Timer Control Register

TOC1,0	A15/TOUT
00	Inhibited
01	Toggle
10	0
11	1

Free-Running Counter

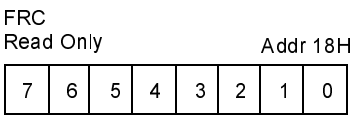


Figure 88. Free-Running Counter

CPU Control Register

CPU Control Register (CCR) Addr 1FH

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Figure 89. CPU

Note: See Figure 106 for full description.

DMA Registers

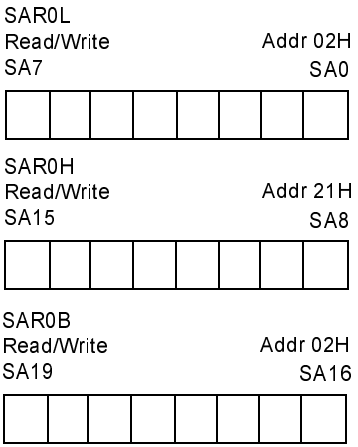


Figure 90. DMA 0 Source Address Registers

Table 35. DMA 0 Source Address Registers

Bits 0-2 (3) are used for SAROB				
A19,	**A18,**	**A17,**	**A16**	**DMA Transfer Request**
x	x	0	0	$\overline{\text{DREQ0}}$ (external)
x	x	0	1	RDR0 (ASCI0)
x	x	1	0	RDR1 (ASC 11)
x	x	1	1	Not Used

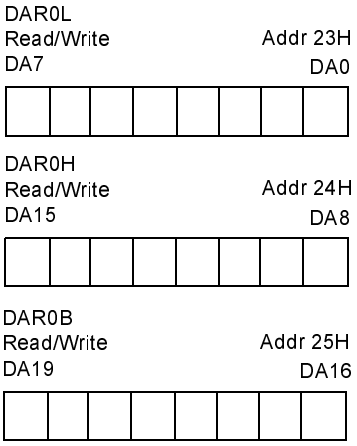


Figure 91. DMA 0 Destination Address Registers

Table 36. DMA 0 Destination Address Registers

Bits 0-2 (3) are used for DAROB				
A19,	**A18,**	**A17,**	**A16**	**DMA Transfer Request**
x	x	0	0	$\overline{\text{DREQ0}}$ (external)
x	x	0	1	TDR0 (ASCI0)
x	x	1	0	TDR1 (ASC 11)
x	x	1	1	Not Used

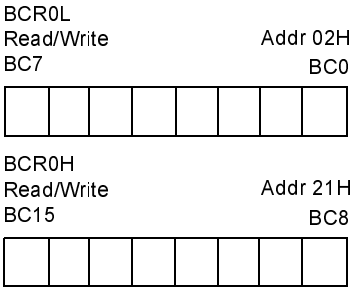


Figure 92. DMA 0 Byte Counter Registers

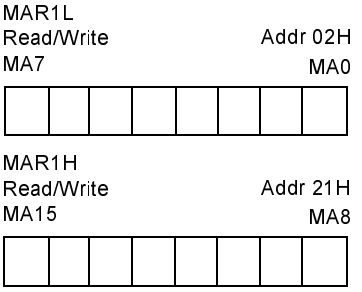


Figure 93. DMA I/O Address Registers

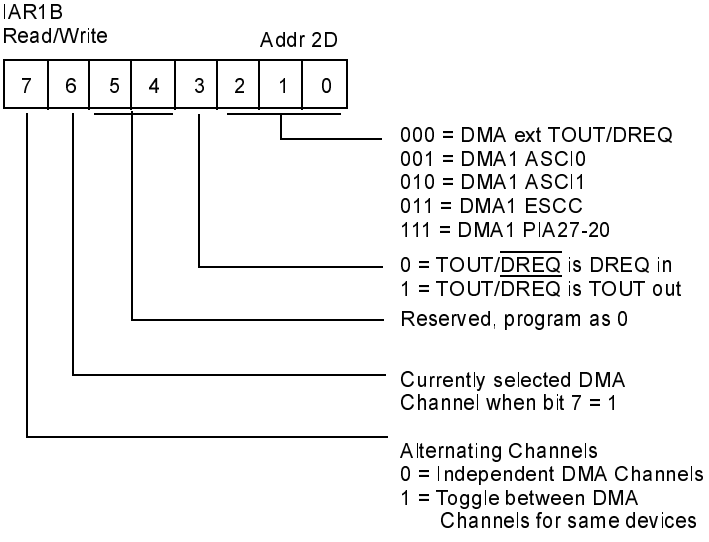


Figure 94. DMA I/O Register Ch. 1

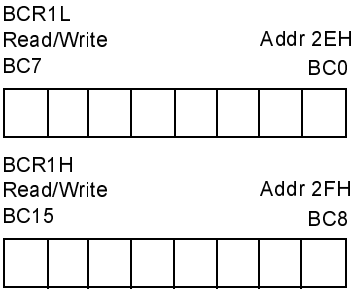


Figure 95. DMA 1 Byte Count Registers

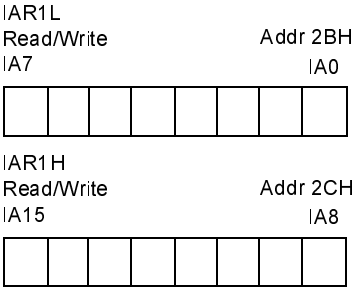


Figure 96. DMA 1 Memory Address Registers

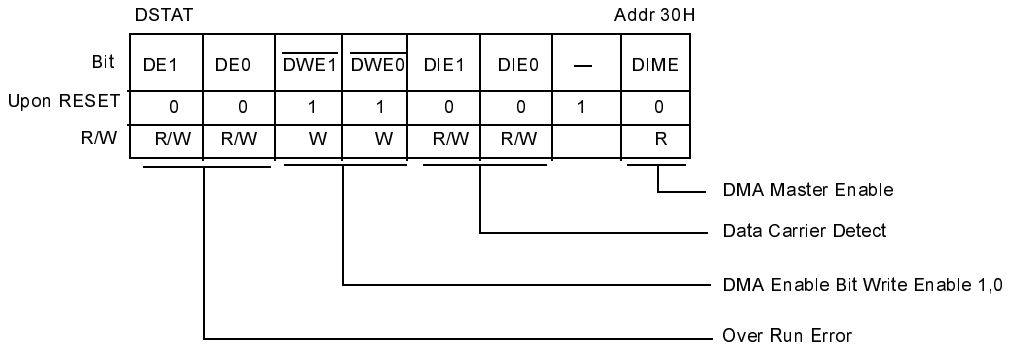


Figure 97. DMA Status Register

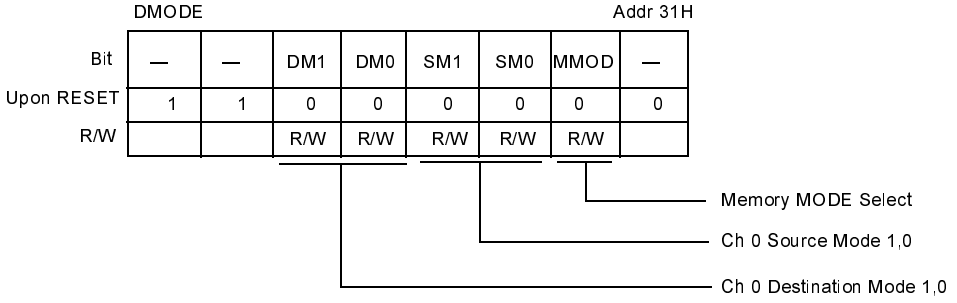


Figure 98. DMA Mode Select Register

Table 37. DMA Mode Select Register

DM1,0	Destination	Address	SM1,0	Source	Address
00	M	DAR0+1	00	M	SA0+1
01	M	DAR0-1	01	M	SAR0-1
10	M	DAR0 Fixed	10	M	SAR0 Fixed
11	I/O	DAR0 Fixed	11	I/O	SAR0 Fixed

Table 38. DMA Mode Register

MMOD	Mode
0	Cycle Steal Mode
1	Burst Mode

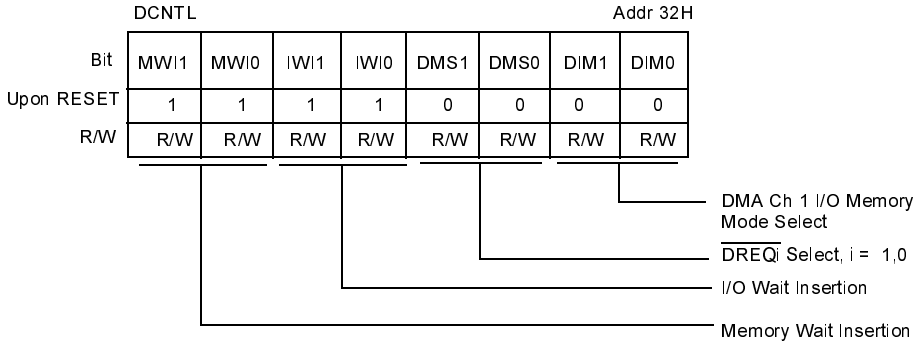


Figure 99. DMA Control Register

Table 39. DMA Control Register

MWI1,0[1]	No. of Wait States	IWI1,0	No. of Wait States
00	0	00	1
01	1	01	2
10	2	10	3
11	3	11	4

DMSi	Sense
1	Edge Sense
0	Level Sense

DM1,0	Transfer Mode	Address	Increment/ Decrement
00	M - I/O	MAR1+1	IAR1 Fixed
01	M - I/O	MAR1-1	IAR1 Fxed
10	I/O -M	IAR1 Fxed	MAR1+1
11	I/O -M	IAR1 Fxed	MA R1-1

NOTES:
1. If using ROM/RAM Chip Select wait state generators, the Z180 wait state generator must be set to 0.

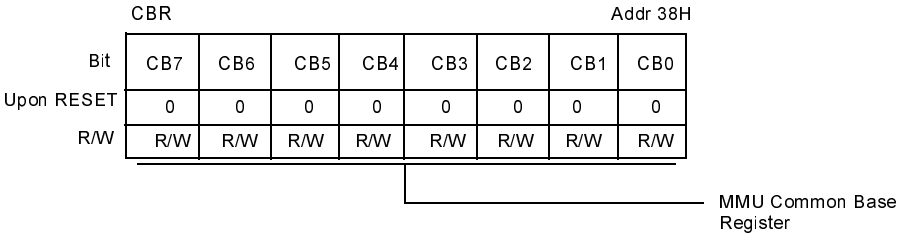


Figure 100. MMU Common Base Register

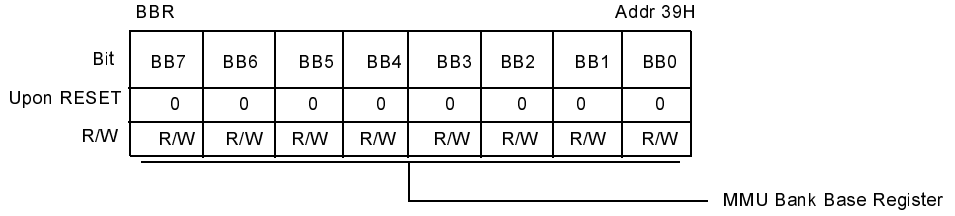


Figure 101. MMU Bank Base Register

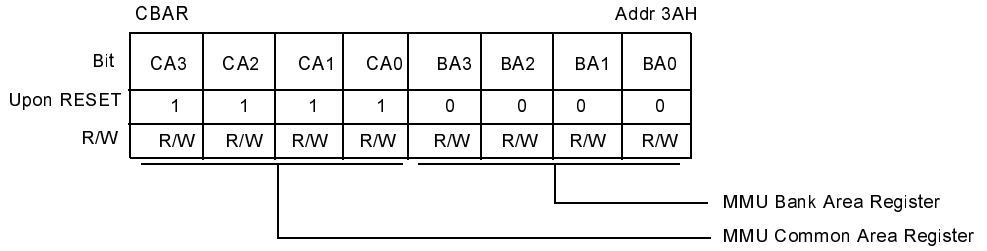


Figure 102. MMU Common/Bank Area Register

System Control Registers

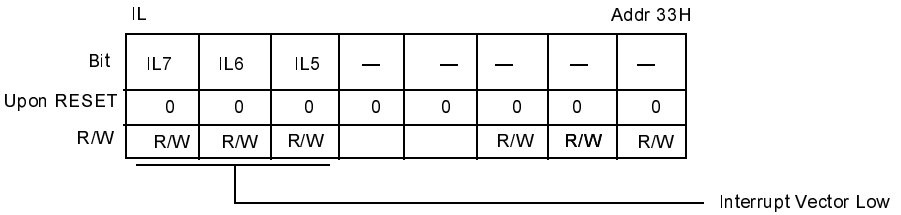


Figure 103. Interrupt Vector Low Register

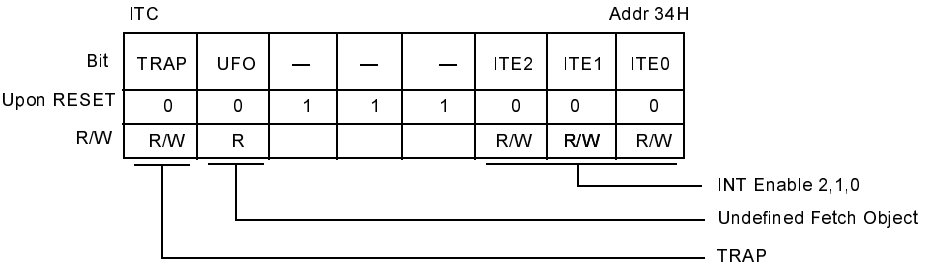


Figure 104. INT/TRAP Control Register

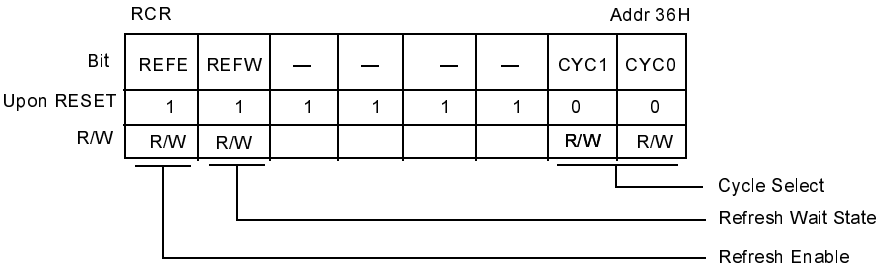


Figure 105. Refresh Control Register

Table 40. Refresh Control Register

CYC1,0	Interval of Refresh Cycle
00	10 states
01	20 states
10	40 states
11	80 states

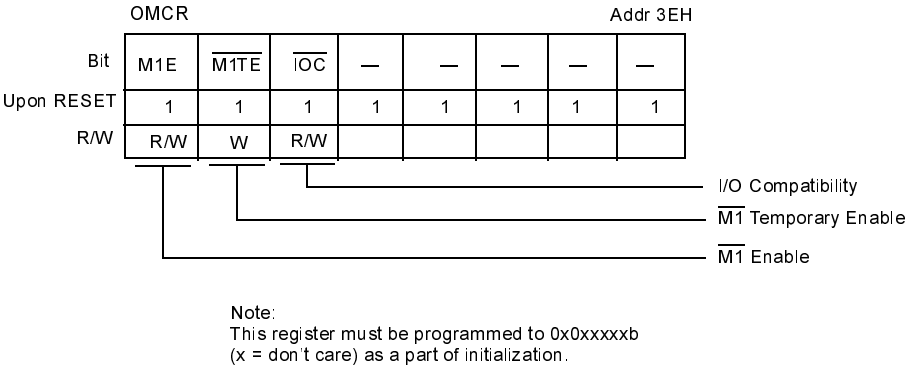


Figure 106. Operation Mode Control Register

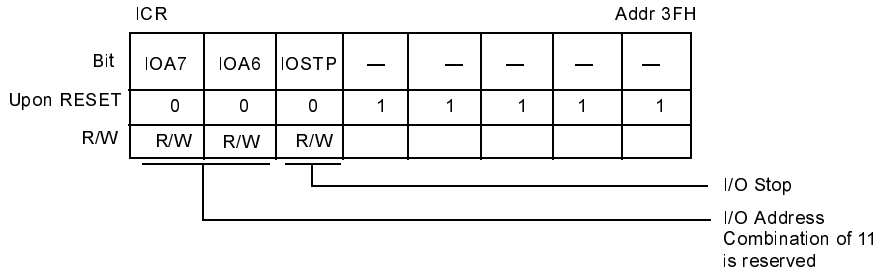


Figure 107. I/O Control Register

Additional Features on the Z182 MPU

The following is a detailed description of the enhancements to the Z8S180 from the standard Z80180 in the areas of STANDBY, IDLE, and STANDBY-QUICK RECOVERY modes.

ADD-ON FEATURES

There are five different power-down modes. SLEEP and SYSTEM STOP are inherited from the Z80180. In SLEEP mode, the CPU is in a stopped state while the on-chip I/Os are still operating. In I/O STOP mode, the on-chip I/Os are in a stopped state while leaving the CPU running. In SYSTEM STOP mode, both the CPU and the on-chip I/Os are in the stopped state to reduce the current consumption. The Z8S180 has added two additional power-down modes, STANDBY and IDLE, to reduce the current consumption even further. The differences among these power-down modes are summarized in Table 41.

Table 41. Power Down Modes

Power-Down Modes	CPU Core	On-Chip I/O	OSC.	CLKOUT	Recovery Source	Recovery Time (Minimum)
SLEEP	Stop	Running	Running	Running	RESET, Interrupts	1.5 Clock
I/O STOP	Running	Stop	Running	Running	By Programming	—
SYSTEM STOP	Stop	Stop	Running	Running	RESET, Interrupts	1.5 Clock

Table 41. Power Down Modes

Power-Down Modes	CPU Core	On-Chip I/O	OSC.	CLKOUT	Recovery Source	Recovery Time (Minimum)
IDLE[1]	Stop	Stop	Running	Stop	RESET, Interrupts, BUSREQ	8 +1.5 Clock
STANDBY[1]	Stop	Stop	Stop	Stop	RESET, Interrupts, BUSREQ	2^{17} +1.5 Clock (Normal Recovery)
						2^{6} +1.5 Clock (Quick Recovery)

NOTES:
1. IDLE and STANDBY modes are only offered in Z8S180. Note that the minimum recovery time can be achieved if INTERRUPT is used as the Recovery Source.

STANDBY Mode

The Z8S180 has been designed to save power. Two low-power programmable power-down modes have been added; STANDBY mode and IDLE mode. The STANDBY/IDLE mode is selected by multiplexing D6 and D3 of the CPU Control Register (CCR, I/O Address = 1 FH). To enter STANDBY mode:

1. Set D6 and D3 to 1 and 0, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY mode, it behaves similar to the SYSTEM STOP mode which currently exists on the Z80180, except that the STANDBY mode stops the external oscillator, internal clocks and reduces power consumption to typically 50 A.

Because the clock oscillator has been stopped, a restart of the oscillator requires a period of time for stabilization. An 18-bit counter in the

Z8S180 allowsfor oscillator stabilization. When the part receives an external IRQ or BUSREQ during STANDBY mode, the oscillator is restarted and the timer counts down 2^{17} counts before acknowledging the interrupt source.

The recovery source needs to remain asserted for duration of the 2^{17} count, otherwise standby is resumed.

The following section is a description of how the part exits STANDBY for different interrupts and modes of operation.

STANDBY Mode Exit With $\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ input must be asserted for a duration long enough for the crystal oscillator to stabilize and then exit from the STANDBY mode. When $\overline{\text{RESET}}$ is de-asserted, it performs the normal reset timing to start instruction execution at address (logical and physical) 0000H.

The clocking resumes within the Z8S180 and at the system clock output after $\overline{\text{RESET}}$ asserts when the crystal oscillator restarts, but not yet stabilized.

STANDBY Mode Exit with BUS REQUEST

Optionally, if the BREXT bit (D5 of CPU Control Register) is set to 1, the Z8S180 exits STANDBY mode when the $\overline{\text{BUSREQ}}$ input asserts; the crystal oscillator restarts. An internal counter automatically provides time for the oscillator to stabilize, before the internal clocking and the system clock output of the Z8S180 are resumed.

The Z8S180 relinquishes the system bus after the clocking is resumed by:

1. Tristating the address outputs A19 through A0.
2. Tristating the bus control outputs $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, RD and $\overline{\text{WR}}$.
3. Asserting $\overline{\text{BUSACK}}$

The Z8S180 regains the system bus when $\overline{\text{BUSREQ}}$ deactivates. The address outputs and the bus control outputs are driven High, and the STANDBY mode is exited.

If the BREXT bit of the CPU Control Register (CCR) is cleared, asserting the $\overline{\text{BUSREQ}}$ does not cause the Z8S180 to exit STANDBY mode.

If STANDBY mode is exited due to a reset or an external interrupt, the Z8S180 remains relinquished from the system bus as long as $\overline{\text{BUSREQ}}$ is active.

STANDBY Mode Exit with External Interrupts

Exit STANDBY mode by asserting input $\overline{\text{NMI}}$. The STANDBY mode may also exit by asserting $\overline{\text{INTO}}$, $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$, depending on the conditions specified in the following paragraphs.

$\overline{\text{INTO}}$ wake-up requires assertion throughout duration of clock stabilization time (2^{17} clocks).

If exit conditions are met, the internal counter provides time for the crystal oscillator to stabilize, before the internal clocking and the system clock output within the Z8S180 resume.

1. Exit with Non-Maskable Interrupts If $\overline{\text{NMI}}$ is asserted, the CPU begins a normal NMI interrupt acknowledge sequence after clocking resumes.
2. Exit with External Maskable Interrupts. If an External Maskable Interrupt input is asserted, the CPU responds according to the status of the Global Interrupt Enable Flag IEF1 (determined by the ITE1 bit) and the settings of the corresponding interrupt enable bit in the Interrupt/Trap Control Register (ITC: I/O Address = 34H):
    a. If an interrupt source is disabled in the ITC, asserting the corresponding interrupt input does not cause the Z8S180 to exit STANDBY mode. This condition is true regardless of the state of the Global Interrupt Enable Flag IEF1.

b. If the Global Interrupt Flag IEF1 is set to 1, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input causes the Z8S180 to exit STANDBY mode. The CPU performs an interrupt acknowledge sequence appropriate to the input currently asserted when clocking is resumed if:
   – The interrupt input follows the normal interrupt daisy chain protocol.
   – The interrupt source is active until the acknowledge cycle is completed.

c. If the Global Interrupt Flag IEF1 is disabled, that is, reset to 0, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input still causes the Z8S180 to exit STANDBY mode. The CPU fetches and executes instructions that follow the SLEEP instruction when clocking is resumed.

If the External Maskable Interrupt input is not active until clocking resumes, the Z8S180 does not exit STANDBY mode. If the Non-Maskable Interrupt ($\overline{\text{NMI}}$) is not active until clocking resumes, the Z8S180 still exits the STANDBY mode even if the interrupt sources go away before the timer times out, because $\overline{\text{NMI}}$ is edge-triggered. The condition is latched internally once $\overline{\text{NMI}}$ is asserted Low.

IDLE Mode

IDLE mode is another power-down mode offered by the Z8S180. To enter IDLE mode:

1. Set D6 and D3 to 0 and 1, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in IDLE mode, the clock oscillator is kept oscillating, but the clock to the rest of the internal circuit, including the CLKOUT, is

stopped completely. IDLE mode is exited in a similar way as STANDBY mode (that is, RESET, BUS REQUEST or EXTERNAL INTERRUPTS) except that the 217 bit wake-up timer is bypassed. All control signals are asserted eight clock cycles after the exit conditions are gathered.

STANDBY-QUICK RECOVERY Mode

STANDBY-QUICK RECOVERY mode is an option offered in STANDBY mode to reduce the clock recovery time in STANDBY mode from 2^{17} clock cycles (6.5 ms at 20 MHz) to 26 clock cycles (3.2 s at 20 MHz). This feature can only be used when providing an oscillator as the clock source.

To enter STANDBY-QUICK RECOVERY mode:

1. Set D6 and D3 to 1 and 1, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY-QUICK RECOVERY mode, the operation is identical to STANDBY mode except when exit conditions are gathered, (RESET, BUS REQUEST or EXTERNAL INTERRUPTS).the clock and other control signals are recovered sooner than the STANDBY mode.

Note: If STANDBY-QUICK RECOVERY is enabled, the user must make sure stable oscillation is obtained within 64 clock cycles.

CPU Control Register

The Z8S180 features an additional register which allows the programmer to select options that directly affect the CPU performance as well as controlling the STANDBY operating mode of the chip. The CPU Control Register (CC R) allows the programmer to change the divide-by-two internal clock to divide-by-one. In addition, applications where EMI noise is a problem, the Z8S180 reduces the output drivers on selected groups of

pins to 25% of normal pad driver capability which minimizes the EMI noise generated by the part.

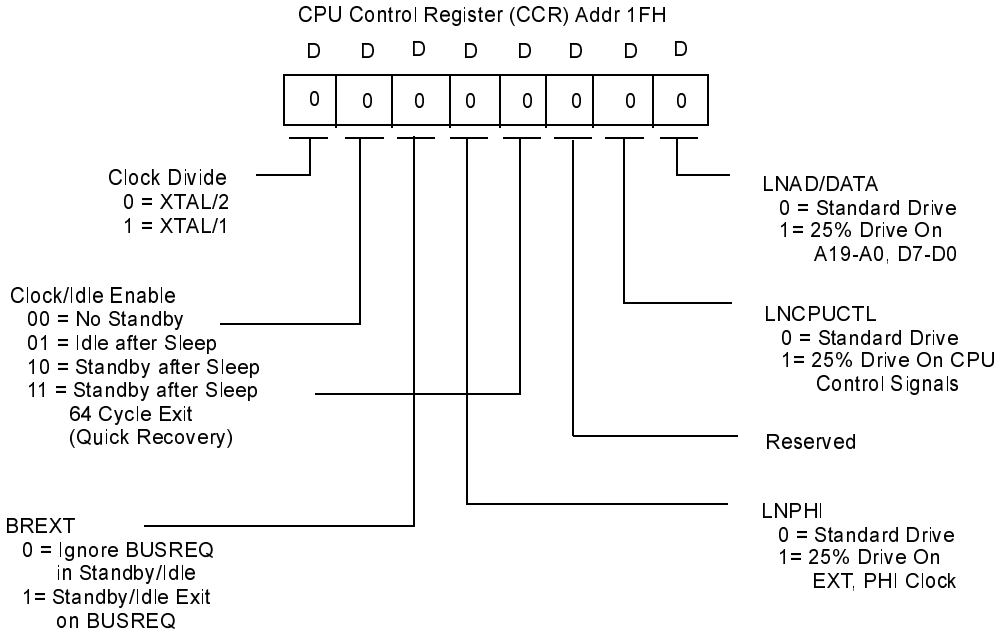


Figure 108. CPU Control Register

Bit 7. Clock Divide Select

Bit 7 of the CCR allows the programmer to set the internal clock to divide the external clock by 2 if the bit is 0 and divide-by-one if the bit is 1. Upon reset, this bit is set to 0 and the part is in divide-by-two mode. Since the on-board oscillator is not guaranteed to operate above 20 MHz, an external source must be used to achieve the maximum 33 MHz operation of the part,that is, an external clock at 66 MHz with 50% duty cycle.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement must be satisfied.

Bits 6 and 3. STANDBY/IDLE Enable

These two bits enable/disable the IDLE and STANDBY mode.

Setting D6, D3 to 0 and 1, respectively, enables the IDLE mode. In the IDLE mode, the clock oscillator remains oscillating but the clock to the rest of the internal circuit, including the CLKOUT, stops. The Z8S180 enters IDLE mode after fetching the second Op Code of a SLEEP instruction, if the I/O STOP bit is set.

Setting D6, D3 to 1 and 0, respectively, enables the STANDBY mode. In the STANDBY mode, the clock oscillator stops completely. The Z8S180 enters STANDBY after fetching the second Op Code of a SLEEP instruction, if the I/O STOP bit is set.

Setting D6, D3 to 1 and 1, respectively, enables the STANDBY-QUICK RECOVERY mode. In this mode, its operations are identical to STANDBY except that the clock recovery reduces to 64 clock cycles after the exit conditions are gathered. Similarly, in STANDBY mode, the Z8S180 enters STANDBY after fetching the second Op Code of a SLEEP instruction, if the I/O STOP bit is set.

Bit 5. BREXT

This bit controls the ability of the Z8S180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

Bit 4. LNPHI

This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output reduces to 25% of its drive capability.

Bit 2. Reserved

Bit 1. LNCPUCTL

This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins reduces to 25% of the original drive capability:

$\overline{\text{BUSACK}}$	$\overline{\text{MREQ}}$
$\overline{\text{RD}}$	$\overline{\text{IORQ}}$
$\overline{\text{WR}}$	$\overline{\text{RFSH}}$
$\overline{\text{M1}}$	$\overline{\text{HALT}}$
E	$\overline{\text{TEND1}}$

Bit 0. LNAD/DATA

This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus output reduces to 25% of its original drive capability.

Z85230 ESCC™ Control Registers

See Figure 109 through Figure 114 for the ESCC Control registers. For additional information, refer to the ESCC Product Specification / Technical Manual.

The Z80182/Z8L182 has two ESCC channels. They can be accessed in any page of I/O space since only the lowest eight address lines are decoded for access. Their Z180™ MPU Address locations are described in Table 29.

When the 16550 MIMIC interface is enabled, ESCC channel B is disconnected from the output pins. The channel B $\overline{\text{TRxCB}}$ clock connects to the Transmit and Receive timers of the 16550 MIMIC interface. **It is recommended that $\overline{\text{TRxCB}}$ be programmed as an output with proper**

baud rate values to timeout the transmitter and receiver of the 16550 MIMIC interface.

Table 42. ESCC Control and Data Map

ESCC Channel A	Control	Z180 MPU Address xxE0H
	Data	Z180 MPU Address xxE1H
ESCC Channel B	Control	Z180 MPU Address xxE2H
	Data	Z180 MPU Address xxE3H

Programming the ESCC™

The ESCC contains write registers in each channel that are programmed by the system separately to configure the functional uniqueness of the channels.

In the ESCC, the data registers are directly addressed by selecting a High on the D/$\overline{C}$ pin. With all other registers (with the exception of WRO and RRO), programming the write registers requires two write operations and reading the read registers, both a write and a read operation. The first write is to WRO and contains three bits that point to the selected register. The second write is the actual control word for the selected read register accessed. All of the ESCC registers, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WRO (or RRO) is addressed again.

With the Z80182/Z8L182, a new feature is implemented in the ESCC. The Transmitter and Receiver is now capable of sending and comparing a 32-bit CRC-32 (Ethernet Polynomial):

$X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$

This feature is enabled by access to WR7' Bit 7, which selects the 32-bit CRC polynomial for the transmitter and receiver and overrides any selection of SDLC/CRC-16 CRCs. When the 32-bit CRC override feature

is enabled, the transmitter only sends 32-bit CRC when CRC is to be sent. On the receive side, the CRC comparison/calculation isperformed only on 32-bit CRC values. The result of the 32-bit CRC comparison is maintained in RR1 bit D6 in place of the 16-bit CRC comparison result. The 32bit CRC compare result is also maintained in the 10 x19 FIFO for frames in which 32-bit CRC is enabled. The CRC still can be preset to all 0s or all 1 s. 32-bit CRC is disabled upon power-up or reset.

Note: The ESCC cannot do simultaneous calculation/ comparison using both 16-bit and 32-bit CRC.

Also, for the Z80182/Z8L182 only, the clock provided to the ESCC core is equal to the system clock divided by 1 or 2. The divider is programmed in the Z80182 Enhancement Register bit 3.

Divide-by-two must be programmed when running the Z182 beyond:

- 20 MHz, 5V
- 10 MHz, 3V

Note: Upon power-up or reset the system clock is equal to the ESCC clock.

Initialization

The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, in the Asynchronous mode, character length, clock rate, number of stop bits, and even or odd parity must be set first. Then the interrupt mode is set, and finally, the receiver and transmitter are enabled.

Write Registers

The ESCC contains 16 write registers (17 counting the transmit buffer) in each channel. These write registers are programmed separately to configure the functional “personality” of the channels. There are two

registers (WR2 and WR9) shared by the two channels that are accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits and reset commands. A new register, WR7', was added to the ESCC and may be written to if WR15, D0 is set. Figure 106 illustrates the format of each write register.

Read Registers.

The ESCC contains ten read registers (eleven, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RRO, RR1, RR10, and RR15). Two registers (RR12 and RR13) are read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (channel A) or the vector modified by status information (channel B). RR3 contains the Interrupt Pending (IP) bits (channel A only). RR6 and RR7 contain the information in the SDLC Frame Status FIFO, but is only read when WR15, D2 is set. If WR7' D6 is set, Write Registers WR3, WR4, WR5, WR7, and WR10 can be read as RR9, RR4, RR5, and RR14, respectively. Figure 107 shows the format of each Read register.

Control Registers

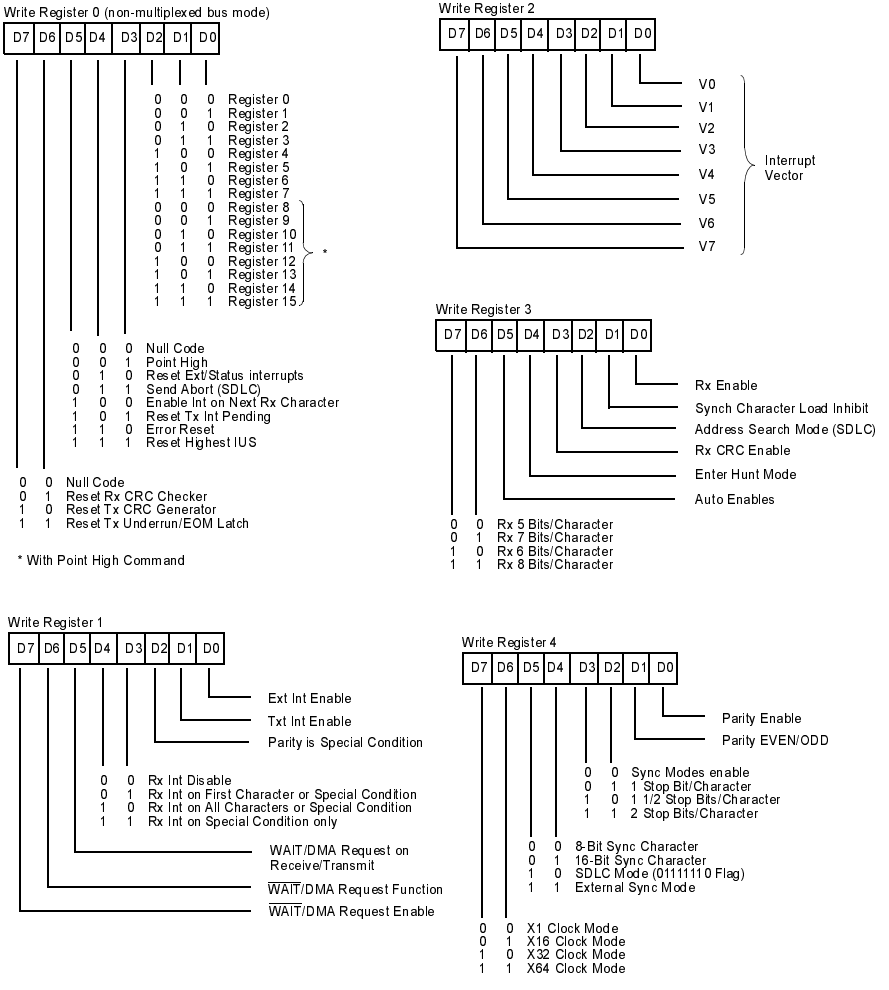


Figure 109. Write Register Bit Functions

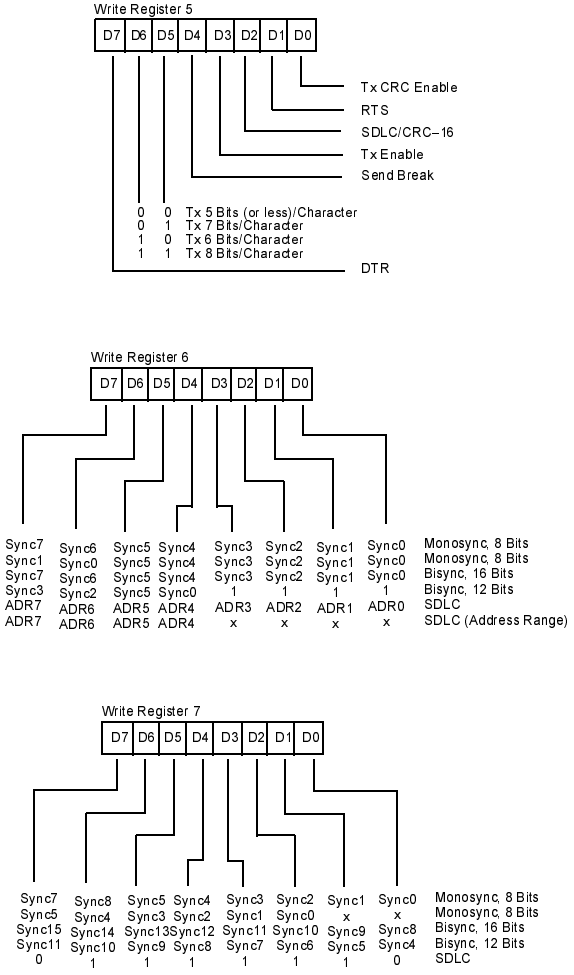


Figure 110. Write Register Bit Functions (Continued)

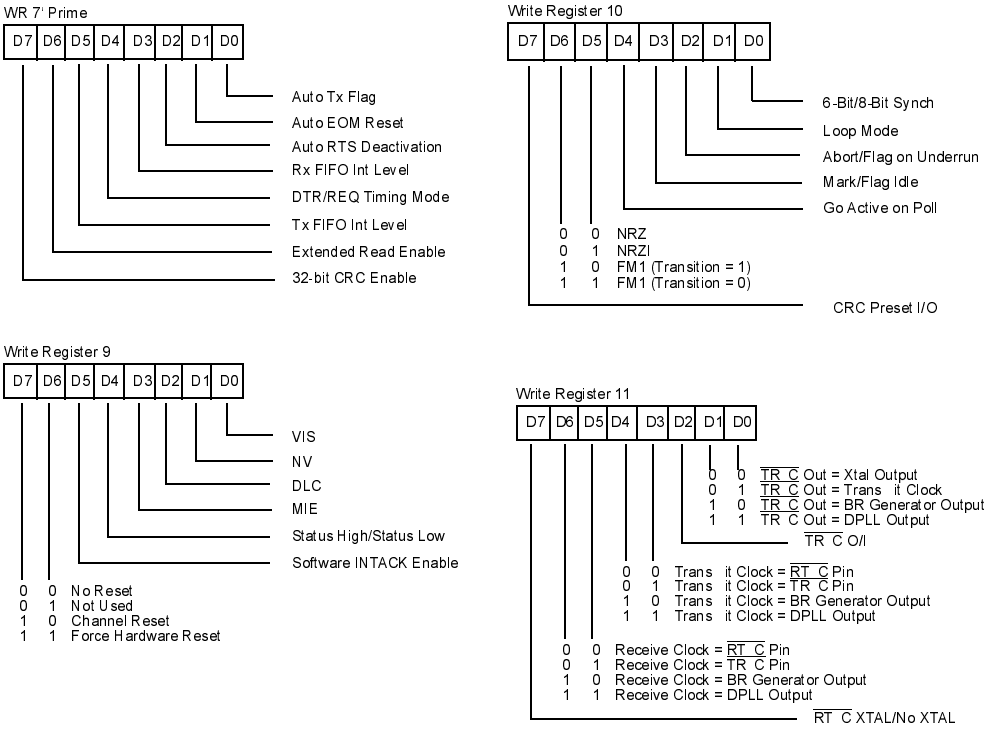


Figure 111. Write Register Bit Functions (Continued)

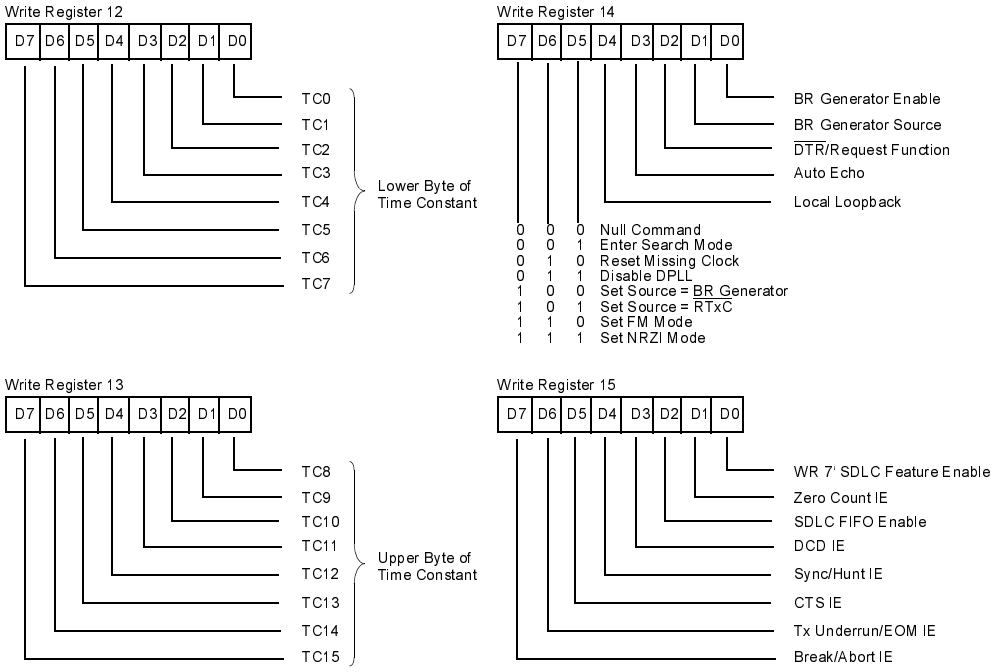


Figure 112. Write Register Bit Functions (Continued)

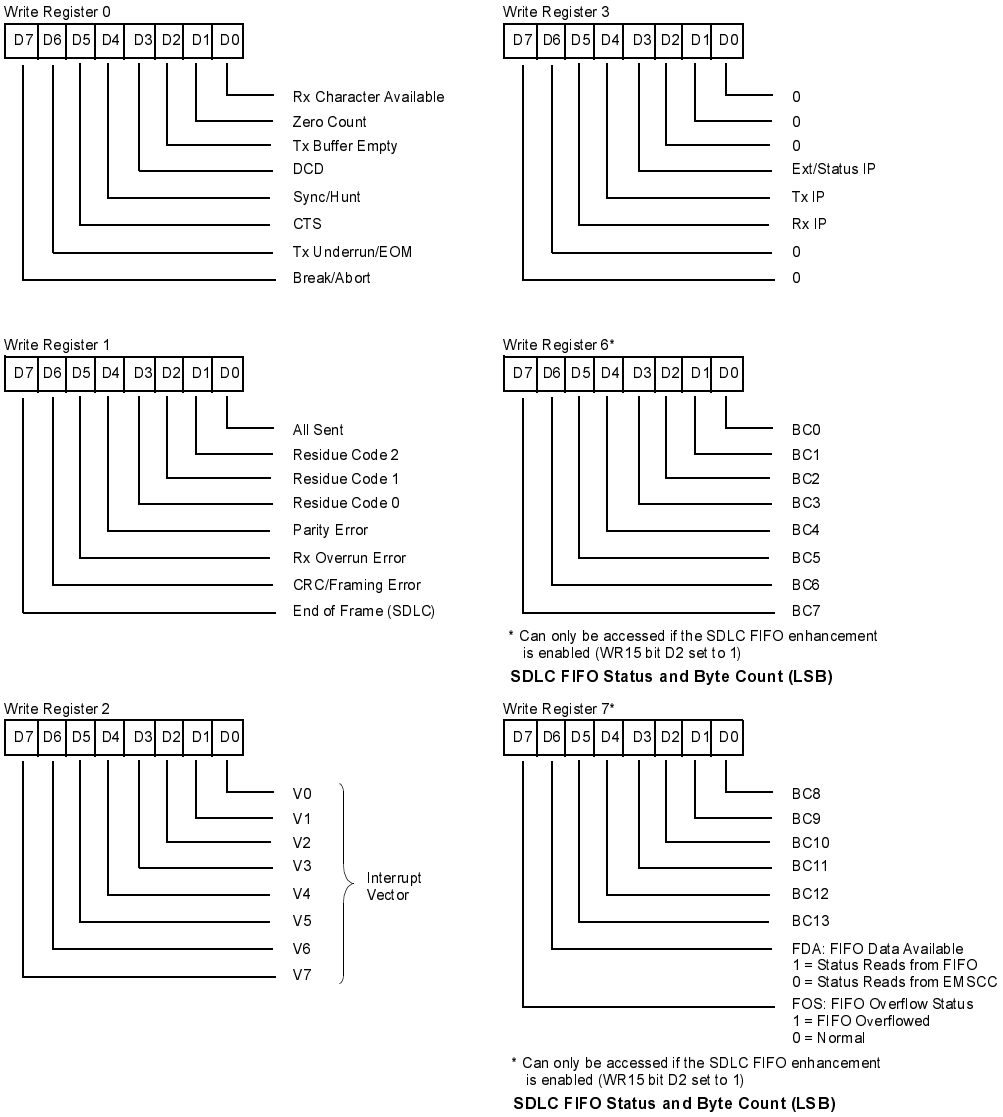


Figure 113. Read Register Bit Functions

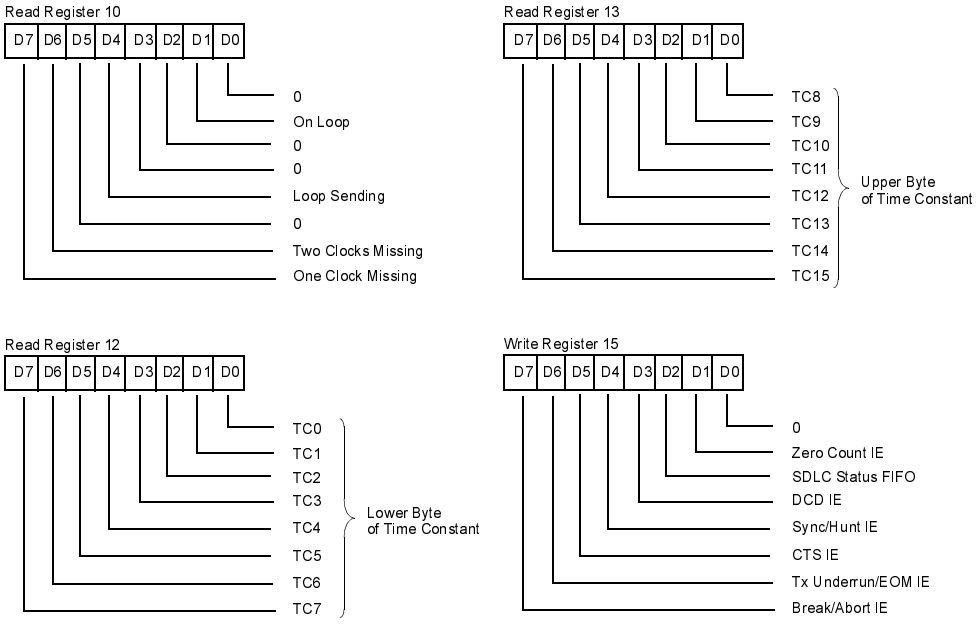


Figure 114. Read Register Bit Functions (Continued)

Other Control and Interface Registers

Figures 115 through Figure 128 describe miscellaneous registers that control the Z182 configuration, RAM/ROM chip select, interrupt and various status and timers.

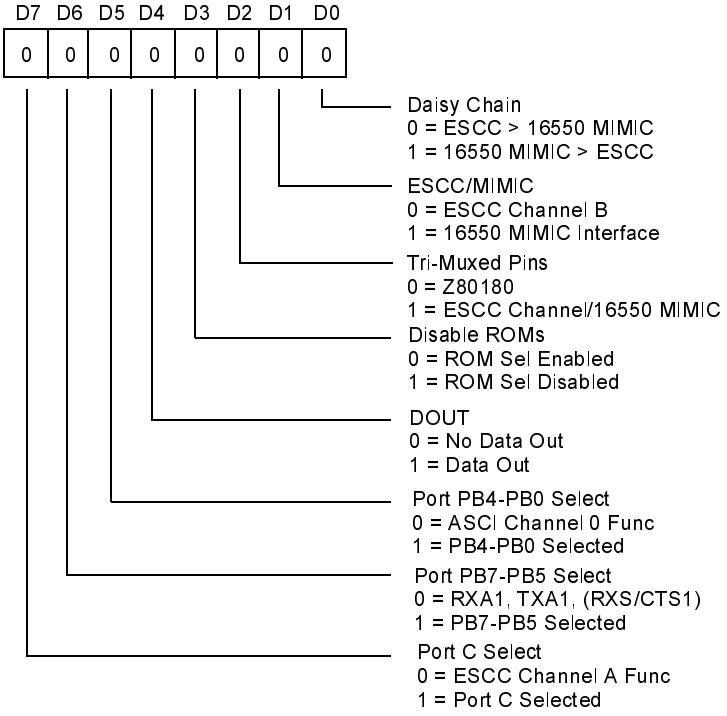


Figure 115. System Configuration Register Z180 MPU Read/Write, Address xxEFH)

System Configuration Register

Bit 7 Port C Select

When this bit is set to 1, bit 8 parallel Port C is selected on the multiplexed pins. When this bit is reset to 0 then these multiplexed pins take ESCC Channel A functions.

Bit 6 PB7-PB5 Select

When this bit is set to 1, parallel Port B bits 7 through 5 are selected on the multiplexed pins. When this bit is reset to 0, these multiplexed pins become RxA1, TxA1 and RxS/CTS1.

Bit 5 PB4-PB0 Select

When this bit is set to 1, parallel Port B bits 4 through 0 are selected on the multiplexed pins. When this bit is reset to 0, these multiplexed pins take ASCI channel 0 functions.

Bit 4 DD_{OUT} ROM Emulator Mode Enable

When this bit is set to 1, the Z182 is in ROM EMULATOR mode. In this mode, bus direction for certain transaction periods are set to the opposite direction to export internal bus transactions outside the Z80182/Z8L182. This allows the use of ROM emulators/logic analyzers for application development (see Table 43 and Table 44).

Note: The word “Out” means that the Z182 data bus direction is in output mode, “In” means input mode, and “Z” means high impedance. DD_{OUT} stands for Data Direction Out and is the status of the D4 bit in the System Configuration Register (SCR).

Table 43. Data Bus Direction (Z182 Bus Master)

I/O And Memory Transactions	I/O Write to On-Chip Peripherals	I/O Read From On-Chip Peripherals	I/O Write to Off-Chip Peripherals	I/O Read From Off-Chip Peripherals	Write To Memory	Read From Mode	Refresh	Z80182 Z8L182 Idle Mode
Z80182 Z8L182 Data Bus (DD_{OUT} = 0)	Out	Z	Out	In	Out	In	Z	Z
Z80182 /Z8L182 Data Bus (DD_{OUT} = 1)	Out	Out	Out	In	Out	In	Z	Z

Table 44. Data Bus Direction (Z182 Bus Master)

Interrupt Acknowledge Transaction	Intack For On-Chip Peripheral (IEI = 1)	Intack For Off-Chip Peripheral (IEI = 0)
Z80182/Z8L182 Data Bus (DD_{OUT} = 0)	Z	In
Z80182/Z8L182 Data Bus (DD_{OUT} = 1)	Out	In

Table 45. Data Bus Direction (Z80182/Z8L182 is not Bus Master)

I/O And Memory Transactions	I/O Write to On-Chip Peripherals	I/O Read From On-Chip Peripherals	I/O Write to Off-Chip Peripherals	I/O Read From Off-Chip Peripherals	Write To Memory	Read From Mode	Refresh	Z80182 Idle Mode
Z80182 Z8L182 Data Bus (DD_{OUT} = 0)	In	Out	Z	Z	Z	In	Z	Z
Z80182	In	Out	Z	Z	Z	In	Z	Z

Table 45. Data Bus Direction (Z80182/Z8L182 is not Bus Master) (Continued)

I/O And Memory Transactions	I/O Write to On-Chip Peripherals	I/O Read From On-Chip Peripherals	I/O Write to Off-Chip Peripherals	I/O Read From Off-Chip Peripherals	Write To Memory	Read From Mode	Refresh	Z80182 Idle Mode
/Z8L182 Data Bus (DD_{OUT} = 1)								

Table 46. Data Bus Direction (Z80182/Z8L182 is not Bus Master)

Interrupt Acknowledge Transaction		
	Intack For On-Chip Peripheral	**Intack For Off-Chip Peripheral**
Z80182JZ8L182 Data Bus (DD_{OUT} = 0)	Z	In
Z80182281_1 82 Data Bus (DD_{OUT} = 1)	Out	In

Bit 3 Disable ROMs

If this bit is 1, it disables the ROMCS pin. If it is 0, addresses below the ROM boundary set by the ROMBR register causes the ROMCS pin to go Low.

Bit 2 Tri-Muxed Pins Select

The Z80182/Z8L182 has three pins that are triple multiplexed and controlled by bit 2 and bit 1. Table 32 shows the different modes.

Table 47. SCR Control for Triple Multiplexed Pins

Bit 2	Bit 1	System Configuration Register
0	0	$\overline{\text{TEND1}}$,TxS,CKS
0	1	$\overline{\text{TEND1}}$,TxS,CKS
1	0	$\overline{\text{RTSB}}$,($\overline{\text{DTR}}$/$\overline{\text{REQB}}$),($\overline{\text{W}}$/$\overline{\text{REQB}}$)
1	1	$\overline{\text{HRxRDY}}$/$\overline{\text{HTxRDY}}$,HINTR

Bit 1 ESCC™ Channel B/MIMIC

- If this bit is 0, Mode 0 is selected.
- If this bit is 1, Mode 1 is selected.

Mode 0:

- Channel A ESCC Enabled
- Channel B ESCC Enabled
- PIA Port Enabled
- 16550 MIMIC Interface Disabled

Mode 1:

- Channel A ESCC enabled
- Channel B outputs disabled
- PIA disabled
- 16550 MIMIC Interface Enabled

Bit 0 Daisy Chain

This bit sets interrupt priority of the ESCC and 16550 MIMIC interface. If it is 0, the ESCC is higher up in the daisy chain than the 16550 MIMIC interface. If it is 1, the 16550 interface is higher up than the ESCC. $\overline{\text{INTO}}$ is used for both MIMIC and ESCC Interrupts.

$\overline{\text{RAMCS}}$ AND $\overline{\text{ROMCS}}$ REGISTERS

To assist decoding of ROM and RAM blocks of memory, three more registers and two pins are featured by the Z80182/Z8L182. The two pins are $\overline{\text{RAMCS}}$ and $\overline{\text{RAMCS}}$. The three registers are RAMUBR, RAMLBR and ROMBR.

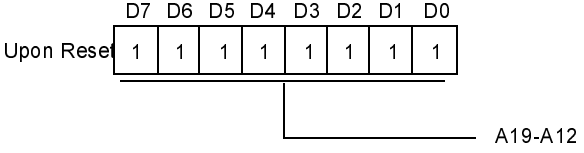


Figure 116. RAMUBR (Z180 MPU Read/Write, Address xxE6H)

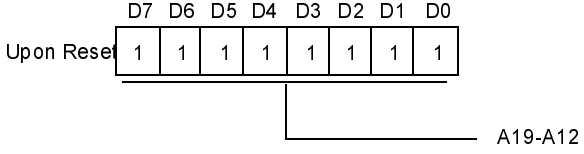


Figure 117. RAMLBR (Z180 MPU Read/Write, Address xxE7H)

RAMUBR, RAMLBR RAM Upper Boundary Range, RAM Lower Boundary Range

These two registers specify the address range for the $\overline{\text{RAMCS}}$ signal. When accessed memory addresses are less than or equal to the value programmed in the RAMUBR and greater than or equal to the value programmed in the RAMLBR, $\overline{\text{RAMCS}}$ is asserted. The A18 signal from the CPU is taken before it is multiplexed with T_{OUT}. If these registers are programmed to overlap, $\overline{\text{RAMCS}}$ takes priority over $\overline{\text{RAMCS}}$ ($\overline{\text{RAMCS}}$ is asserted and $\overline{\text{RAMCS}}$ is inactive).

Chip Select signals are going active for the address range:

- $\overline{\text{RAMCS}}$: (ROMBR) ≥ A19-A12 ≥ 0
- $\overline{\text{RAMCS}}$: (RAMUBR) ≥ A19-A12 ≥ (RAMLBR)

These registers are set to FFH at POR, and the boundary addresses of ROM and RAM are as follows:

- ROM lower boundary address (fixed) = 00000H
- ROM upper boundary address (ROMBR register) = 0FFFFFH
- RAM lower boundary address (RAMLBR register) = 0FFFFFH
- RAM upper boundary address (RAMUBR register) = 0FFFFFH

Because $\overline{\text{ROMCS}}$ takes priority over $\overline{\text{RAMCS}}$, the latter is never asserted until the value in the ROMBR and RAMLBR registers are re-initialized to lower values.

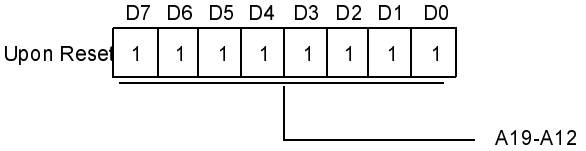


Figure 118. ROMBR (Z180 MPU Read/Write, Address xxE8H)

ROMBR ROM Address Boundary Register

This register specifies the address range for the $\overline{\text{ROMCS}}$ signal. When accessed, memory addresses are less than or equal to the value programmed in this register, the $\overline{\text{ROMCS}}$ signal is asserted.

The A18 signal from the CPU is obtained before it is multiplexed with TOUT. This signal can be forced to a "1" (inactive state) by setting bit 3 in the System Configuration Register, to allow the user to overlay the RAM area over the ROM area.

Z80182 Improvement to the Wait State Generator

A separate Wait State Generator is provided for access memory using $\overline{\text{RAMCS}}$ and $\overline{\text{RAMCS}}$. A single 8-bit register is added to enable/disable this feature as well as provide two 3-bit fields that provide 1 to 8 waits for each chip select.

WSG Chip Select Register (Z80182 address D8H)

Bit 7 $\overline{\text{RAMCS}}$ Wait State Generator Enable

Disable on power-up or reset.

Bits 6-4 $\overline{\text{RAMCS}}$ Wait States 1 to 8

Eight wait states on power-up or reset.

Bit 3 $\overline{\text{RAMCS}}$ Wait State Generator Enable

Disable on power-up or reset.

Bits 2-0 $\overline{\text{RAMCS}}$ Wait States 1 to 8.

Eight wait states on power-up or reset.

There are two wait state generators in the Z182. The actual number of wait states inserted is the greatest number of both the Z180 WSG and the chip select WSG.To use the Chip Select WSG, the Z180 WSG must be programmed to 0 wait states.

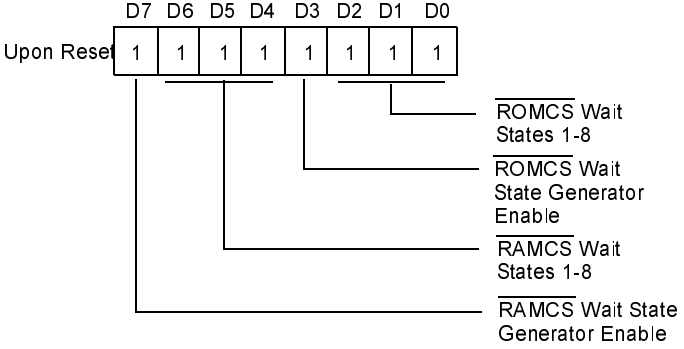


Figure 119. WSG Chip Select Register (Z180 MPU Read/Write, Address xxD8H)

Interrupt Edge/Pin MUX Register

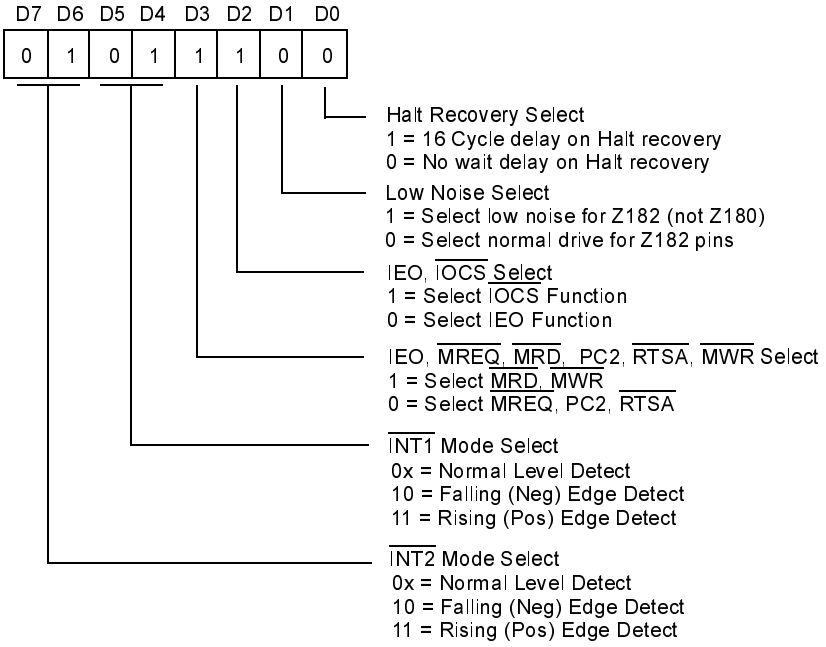


Figure 120. Interrupt Edge/Pin MUX Register (Z180 MPU Read/Write, Address xxDFH)

Bits 7-6

These bits control the interrupt capture logic for the external $\overline{INT2}$ PIN. When programmed as'0X', the $\overline{INT2}$ pin performs as the normal level detecting interrupt pin. When programmed as 10 the negative edge detection is enabled. Any falling edge latches an active Low on the internal $\overline{INT2}$ of the Z180. This interrupt must be cleared by writing a 1 to bit 7 of the Port C Data Register. Programming these control bits to 11

enables rising edge interrupts to be latched. The latch is cleared in the same fashion as the falling edge.

Bits 5-4

These bits control the interrupt capture logic for the external $\overline{\text{INT1}}$ PIN. When programmed as'0X', the $\overline{\text{INT1}}$ pin performs as the normal level detecting interrupt pin. When programmed as 10, the negative edge detection is enabled. Any falling edge latches an active Low on the internal $\overline{\text{INT1}}$ of the Z180. This interrupt must be cleared by writing a 1 to bit 6 of the Port C Data Register. Programming these control bits to 11 enables rising edge interrupts to be latched. The latch is cleared in the same fashion as the falling edge. Edge detect logic cannot be used in Emulation Adaptor EV mode 1.

Bit 3

Programming this bit to 1 selects the $\overline{\text{MRD}}$ and the $\overline{\text{MWR}}$ functions. The default for power up and $\overline{\text{RESET}}$ conditions is 1, i.e., the $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$. By programming this bit to 0 the $\overline{\text{MREQ}}$ Z180 function is enabled, as well as the PC2/$\overline{\text{RTSA}}$ function on the PC2/$\overline{\text{RTSA}}$/$\overline{\text{MWR}}$ pin. If the $\overline{\text{MREQ}}$ Z180 function is enabled, any external bus master must be prevented from asserting Z182's IRD signal unless accessing Z182's I/O.

Bit 2

This bit selects the $\overline{\text{IOCS}}$ function which is the default for power up and $\overline{\text{RESET}}$ conditions. By programming this bit to 0 the IEO function is enabled for this multiplexed pin.

Bit 1

This bit selects the low noise or normal drive feature for the Z182 pins. The default at power up is normal drive for Z182 pins. By programming this bit to 1, low noise for the Z182 pins is chosen and the output drive capability of the following pins is reduced to 25% of the original drive capability:

CKS	CKA/$\overline{\text{TEND0}}$	CKA0/$\overline{\text{DREQ0}}$
RxS/CTS1	TxA1	TxA0
TXS		

Programming this bit to 0 selects normal drive for the Z182 pins. Refer to the Z8S180 Product Specification for Low noise control of Z180 pins.

Bit 0

Programming this bit to 1 selects a 16 cycle wait delay on recovery from HALT. Halt Recovery is disabled if bit 5 of the enhancement register is set to 1. A 0 selects no wait delay on Haft recovery. If Haft Recovery is selected, the following pins assume the following states during halt and during the recovery, whether it is in HALT, SLP, IDLE or STBY Modes:

Address	=	Z
Data Bus	=	Z
RD	=	Z
WR	=	Z
MREQ/MRD	=	Z
M1	=	1
ST	=	1
IORQ	=	1
BUSACK[1]	=	1
RFSH[2]	=	1
E	=	Note[3]
IOCS	=	Z
MWR	=	1 (Note[4])

NOTES:
1. This assumes that BUSREQ is not activated during the halt.
2. This assumes that the refresh is not enabled. This would not be a logical case since the address bus is tristated during the Haft mode.
3. There is no control on the E line during the haft recovery so transitions on the pin are possible.
4. This is only true if MWR function is enabled.

The HALT RECOVERY mode is implemented by applying waft states to the next CPU operation following the exit from haft. All signals listed above are forced to their specified state (unless otherwise noted) during haft and also during the recovery state. Sixteen cycles after the $\overline{\text{HALT}}$ pin goes High the signals are released to their normal state, then eight wait states are inserted to allow proper access to accommodate slow memories.

After the first memory access, the wait states are inserted as programmed in the wait state generators.

In addition, if bit 4 of the Z80182 Enhancement Register is set, the TxDA pin is tristated during Halt and Recovery modes.

Bit <7-6> Reserved

Bit 5 Force Z180 Halt Mode

If this bit is set to 1, it disables the 16 cycle halt recovery and halt control over the busses and pins. This bit is used to allow DMA and Refresh Access to take place during halt (like Z180). This bit is set to 0 on reset.

Bit 4 TXDA tristate

The TxDA pin can be tristated on assertion of the $\overline{\text{HALT}}$ pin. This prevents the TxDA from driving and external device when $\overline{\text{HALT}}$ output is used to force other devices into power-down modes. This feature is

disabled on power-up or reset. It is also controlled by bit 5 in the enhancement register, this feature is disabled if bit 5 is set.

Bit 3 ESCC Clock Divider

The ESCC clock can be provided with the Z180 core's PHI clock or by a PHI clock divide by 2 circuit. When this bit is set, the ESCC's clock is the Z1 80's PHI clock divided by two. Upon power-up or reset, the ESCC clock frequency is equal to the Z180 core's PHI clock output.

Note: If operating above 20 MHz/5V or 10 MHz/3V, this bit must be set for ESCC divide-by-two mode.

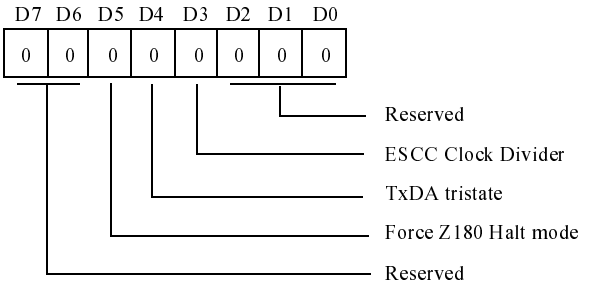


Figure 121. Z80182 Enhancements Register (Z180 MPU Read/Write, Address xxD9H)

Z80182 Enhancements Register

Bit <7-6> Reserved

Bit 5 Force Z180 Halt Mode

If this bit is set to 1, it disables the 16 cycle halt recovery and halt control over the busses and pins. This bit allows DMA and Refresh Access to take place during halt (like Z180). This bit is set to 0 on reset.

Bit 4 TxDA tristate

The TxDA pin can be tristated on assertion of the $\overline{\text{HALT}}$ pin. This prevents the TxDA from driving and external device when $\overline{\text{HALT}}$ output is used to force other devices into power-down modes. This feature is disabled on power-up or reset. It is also controlled by bit 5 in the enhancement register, this feature is disabled if bit 5 is set.

Bit 3 ESCC Clock Divider

The ESCC clock can be provided with the Z180 core's PHI clock or by a PHI clock divide by 2 circuit. When this bit is set, the ESCC's clock is the Z1 80's PHI clock divided by two. Upon power-up or reset, the ESCC clock frequency is equal to the Z180 core's PHI clock output.

Note: If operating above 20 MHz/5 V or 10 MHz/3 V, this bit must be set for ESCC divide-by-two mode.

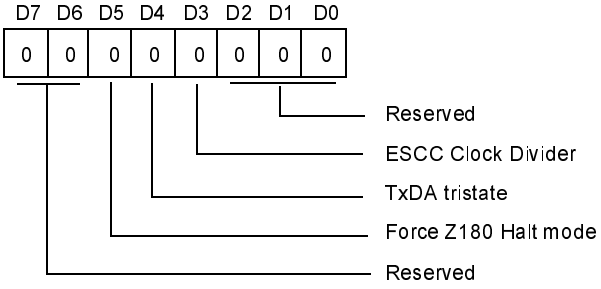


Figure 122. Z80182 Enhancements Register (Z180 MPU Read/Write, Address xxD9H)

Parallel Ports Registers

The Z80182/Z8L182 contains three 8-bit bi-directional Ports. Each bit is individually programmable for input or output. The Ports consist of two registers the Port Direction Control Register and the Port Data Register. The Port and direction register can be accessed in any page of I/O space because only the lowest eight address lines are decoded. Bits PC7 and PC6 are input only bits and have the special function of reading the external value of the $\overline{INT2}$ and $\overline{INT1}$ pins. Writing '1' to these bits clears the edge detect interrupt logic when operating $\overline{INT2}$ and/or $\overline{INT1}$ in edge detect mode.

When Port B and Port C bits 5-0 are deselected in the System Configuration Register, the Data and Data Direction Registers are still available as read/write scratch registers. If a Port is deselected and if the DDR bit is a '0', then the written value to that bit is latched and this value can be read back. If a Port is deselected and if the DDR bit is a '1', only the external pin value can be read. Any write to that bit is latched but can be read back only with DDR = 0.

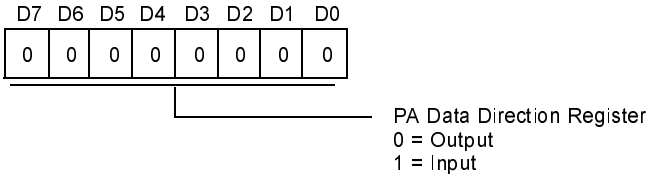


Figure 123. PA, Port A, Data Direction Register (Z180 MPU Read/Write, Address xxEDH)

The data direction register determines which are inputs and outputs in the PA Data Register. When a bit is set to 1 the corresponding bit in the PA Data Register is an input. If the bit is 0, then the corresponding bit is an output.

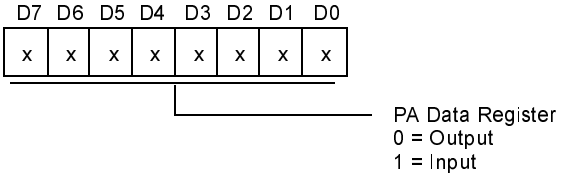


Figure 124. PA, Port A, Data Register (Z180 MPU Read/Write, Address xxEEH)

When the Z180 MPU writes to the PA Data Register the data is stored in the internal buffer. The values of the PA Data Register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PA Data Register the data on the external pins is returned.

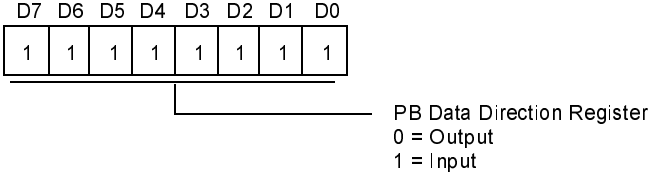


Figure 125. PB, Port B, Data Direction Register (Z180 MPU Read/Write, Address xxE4H)

The data direction register determines which are inputs and outputs in the PB Data Register. When a bit is set to 1 the corresponding bit in the PB Data Register is an input. If the bit is 0 then the corresponding bit is an output.

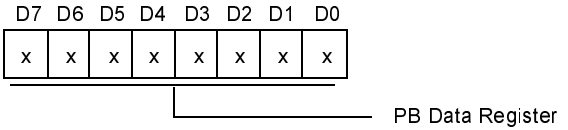


Figure 126. PB, Port B, Data Register (Z180 MPU, Address xxE5H)

When the Z180 MPU writes to the PB Data Register the data is stored in the internal buffer. The values of Port B data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PB Data Register, the data on the external pins is returned.

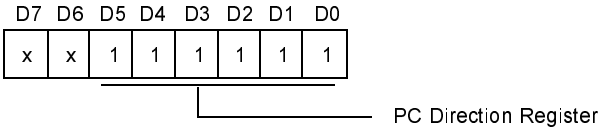


Figure 127. PC, Port C, Data Direction Register (Z180 MPU Read/Write, Address xxDDH)

The data direction register determines which are inputs and outputs in the PC Data Register. When a bit is set to 1 the corresponding bit in the PC Data Register is an input. If the bit is 0, then the corresponding bit is an output.

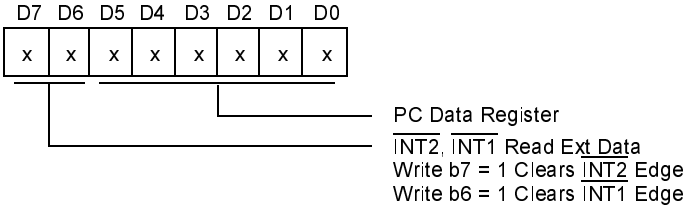


Figure 128. PC, Port C, Data Register (Z180 MPU Read/Write, Address xxDEH)

When the Z180 MPU writes to the PC Data Register, the data is stored in the internal buffer. The values of Port C data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PC Data Register, the data on the external pins is returned.

Bits 6 and 7 serve the special function of reading the value of the external $\overline{INT2}$ and $\overline{INT1}$ lines. When operating either $\overline{INT2}$ or $\overline{INT1}$ in edge detection mode, the edge detect latch is reset by writing a 1 to bit 6 or 7 respectively. Writing a 0 has no effect.

Note: These latches must be reset at the end of an INT2 or INT1 interrupt service routine when using edge-triggered interrupt modes.

16550 MIMIC INTERFACE DMA

The 16550 MIMIC is also able to do direct DMA with the PC/XT/AT. DMA is enabled by setting bits 3, 4 and 5 of the Master Control Register. DMA is accomplished by using the two DMA pins and the Transmitter Holding and Receive Data Registers.

If bit 5 is 1, the $\overline{HTxRDY}$ pin is equal to the complement of the Transmit Holding Register Empty bit. If bit 5 is 1 and bit 3 is 0 the external $\overline{DREQ1}$

pin of the Z180 MPU is disabled and the internal $\overline{\text{DREQ1}}$ is equal to the complement of the Transmit Holding Register Empty Shadow bit. If bit 5 is 1 and bit 3 is 1 the external $\overline{\text{DREQ0}}$ pin of the Z180 MPU is disabled and the internal $\overline{\text{DREQ0}}$ is equal to the complement of the Transmit Holding Register Empty Shadow bit.

If bit 4 is 1, then the $\overline{\text{HRxRDY}}$ pin is equal to the complement of the Data Ready bit. If bit 4 is 1 and bit 3 is 0 the external $\overline{\text{DREQ0}}$ pin of the Z180 MPU is disabled and the internal $\overline{\text{DREQ0}}$ is equal to the complement of the Data Ready Shadow bit. If bit 4 is 1 and bit 3 is 1 the external $\overline{\text{DREQ1}}$ pin of the Z180 MPU is disabled and the internal $\overline{\text{DREQ1}}$ is equal to the complement or the Data Ready Shadow bit.

Z80182/Z8L182 MIMIC DMA CONSIDERATIONS

For the PC Interface, the 16550 device has two modes of operation that need to be supported by the MIMIC. In single transfer mode, the DMA request line for the receiver goes active whenever there is at least one character in the RCVR FIFO. For the transmitter, the DMA request line is active on an empty XMIT FIFO and inactive on non-empty. In multi-transfer mode, the RCVR DMA goes active at the trigger level and inactive on RCVR FIFO empty. The XMIT DMA is active on non-full XMIT FIFO and inactive on a full XMIT FIFO.

Bit 3 in the FCR controls the DMA mode for the PC interface. If a 1 is programmed into this bit, multi-byte DMA is enabled. A 0 in this bit (default) enables single byte DMA. As specified, the 16550 does not have any means of handling the error status bits in the FIFO in this mufti-transfer mode. Such DMA transfers would require blocks with some checksum or other error checking scheme.

For the MPU interface, the DMA is controlled by a non-empty transmit FIFO and by a non-full receive FIFO conditions (THRE and the DR bits in the LSR). If the delay timers are enabled, the respective shadow bits are used for DMA control. The effect of the DMA logic is to request DMA

service when at least one byte of data is available to be read or written to the FIFO's by the Z180. The Z180's DMA channel can be programmed to trigger on edge or on level.

Emulation Modes

The Z80182/Z8L182 provides four modes of operation. The modes are selected by the EV1 and EV2 pins. These four modes allow the system development and commercial production to be done with the same device. The four emulation modes are shown in Table 33.

Table 48. EV2 and EV1, Emulation Mode Control

	EV2	EV1	EV Description
Mode 0	0	0	Normal Mode, on-chip Z180 bus master
Mode 1	0	1	Emulation Adapter Mode
Mode 2	1	0	Emulator Probe Mode
Mode 3	1	1	RESERVED, for Test Use Only

Mode 0 Normal Mode

This is the normal operating mode for the Z80182/Z8L182.

Mode 1 Emulation Adapter Mode

The Emulation Adaptor Mode enables system development for the Z182 with a readily available Z180 emulator. The Emulator provides the Z180MPU and Z180 peripheral functions to the target system, with their signals passing through the emulation adapter. In Emulation Adaptor Mode the Z1 82s, Z180 MPU and Z180 peripheral signals are tristate or physically disconnected. The Z182 continues to provide its ESCC, MIMIC, chip select, and Port functions and signals to the target system.

The Mode 1 effects on the Z182 are listed in Table 49. INT12 Edge Detect Logic cannot be used in Emulation Adaptor EV Mode 2.

Table 49. Emulation Mode 1

Signal	Normal Mode 0	Emulation Adaptor Mode 1
PHI	Output	Input
M1	Output	Input
$\overline{\text{MREQ}}$,$\overline{\text{MRD}}$	Output	Input
IORQ	Output	Input
RD	Output	Input
WR	Output	Input
RFSH	Output	Input
HALT	Output	Input
ST	Output	Input
E	Output	tristate
BUSACK	Output	Input
WAIT	Input	Output
A19,A18/T_{0UT}	Output	Input
A17-A0	Output	Input
D7-D0	Input/Output	Input/Output
TxA0	Output	tristate
RTS0	Output	tristate
TxA1	Output	tristate
INT0	Input	Output, Open-Drain

Mode 2 Emulation Probe Mode

In the Emulator Probe Mode all of the Z182 output signals are tristate. This scheme allows a Z182 emulator probe to grab on to the Z182 package leads on the target system.

Mode 3 RESERVED (for test purposes only)

This mode is reserved for test purpose only, do not use.

Note: Z182 has two branches of reset. $\overline{\text{RESET}}$ controls the Z182 overall configuration, RAM and ROM boundaries, plus the ESCC, Port and the 16550 MIMIC interface. In Normal Mode, a “one shot” circuit samples the input of the $\overline{\text{RESET}}$ pin to assert the internal reset to its proper duration. In Adapter Mode, this “one shot’ circuit is bypassed. Note also that the Z1 80’s crystal oscillator is disabled in Mode 1 and Mode 2.

In Mode 1 the emulator must provide $\overline{\text{MREQ}}$ on the ($\overline{\text{MREQ}}$, $\overline{\text{MRD}}$) Z80182281-1 82 pin (not $\overline{\text{MRD}}$); and A18 (not T_{OUT}) on the A18/T_{OUT} pin.

SLEEP, HALT Effect on MIMIC and 182 Signals

The following Z80182/Z8L182 signals are driven High when Z180™ MPU enters a SLEEP or HALT state:

- $\overline{\text{MRD}}$ when selected in the Interrupt Edge/Pin MUX Register.
- $\overline{\text{MWR}}$ when selected in the Interrupt Edge/Pin MUX Register.
- $\overline{\text{ROMCS}}$, $\overline{\text{RAMCS}}$ always High in SLEEP or HALT.
- The following signals are High-Z during SLEEP and HALT:
- $\overline{\text{IOCS}}$ when so selected in the Interrupt Edge/Pin MUX Register.
- $\overline{\text{RD}}$ and $\overline{\text{WR}}$.

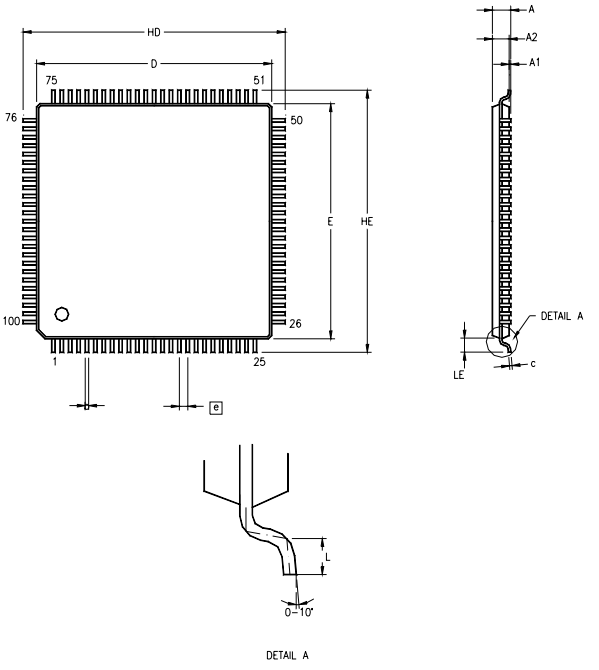
A0-A19 (A18 if selected) always High-Z in power down.

D0-D7 always High-Z in power down modes.

The MIMIC logic of the 182 is disabled during power down modes of the Z180.

Package and Ordering Information

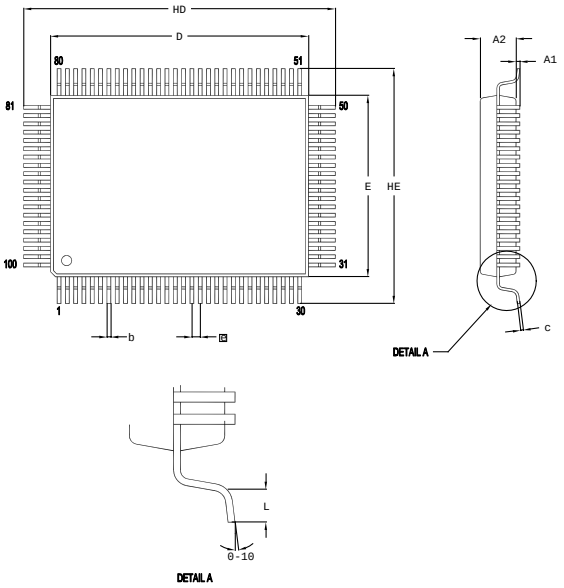
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.006	.010
c	0.10	0.20	.004	.008
HD	15.85	16.15	.624	.636
D	13.90	14.10	.547	.555
HE	15.85	16.15	.624	.636
E	13.90	14.10	.547	.555
e	0.50 BSC		.0197 BSC	
L	0.35	0.65	.014	.026
LE	0.90	1.10	.035	.043

1. CONTROLLING DIMENSIONS : MM
2. MAX COPLANARITY : .10mm / .004"

Figure 129. 100-Pin VQFP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.90	.102	.114
b	0.25	0.40	.010	.016
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.65 BSC		.0256 BSC	
L	0.70	1.10	.028	.043

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. MAX COPLANARITY : .10 / .004

Figure 130. 100-Pin QFP Package Diagram

ORDERING INFORMATION

Z8L182	**Z80182**
20 MHz	**33 MHz**
Z8L18220ASC	Z8018233ASC
ZSL18220FSC	Z8018233FSC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) desired.

Preferred Package	**Environmental**
A = VQFP (Very Small QFP) Quad Flatpack	C = Plastic Standard F = Plastic D = Plastic Stressed E = Hermetric Standard

Preferred Temperature
S = 0 °C to +70 °C

Speeds
20 = 20 MHz
33 = 33 MHZ

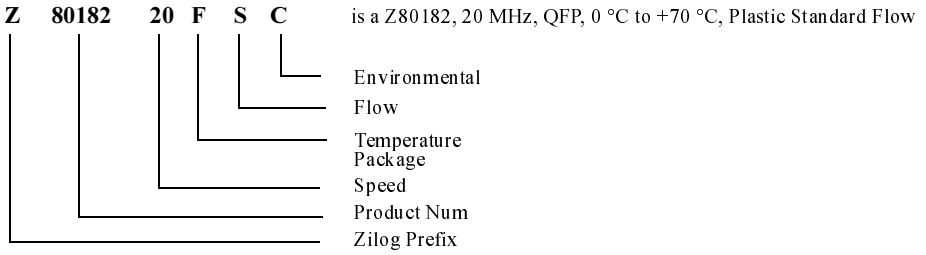


Figure 131. EXAMPLE

Z80182 PRECAUTIONS

1. Changing ESCC TRxCB prescaler to emulation timers may cause MIMIC FIFOs to lock up.

   Workaround: Avoid changing timer clocks “on the fly”. Timers must be disabled prior to any modification of timer registers.

2. When PC writes to the FIFO Control register and attempts to reset the RCVR or XMIT FIFO, the MPU shadow bits (RCVR and XMIT FIFO reset status) may clear before the status is read. This becomes more apparent when operating above 5.0 V.

   Workaround: During a FCR interrupt to MPU, read the FCR register. If the FCR does not indicate a Rx threshold change or FIFO enable bit change, then assume RCVR and XMIT FIFO reset.

Because the SMIT FIFO reset forces TEMT bit to zero, you may need to manually set this bit. Unless you are using the TEMT emulation feature, set the TEMT bit after reading a byte out of the THR register.

3. ESCC data transfers cannot be simultaneously set up for DMA and Interrupt mode on the Z182. For example, if DMA is configured to transfer data to ESCC when Tx buffer is empty, and interrupts are enabled to transfer data to ESCC when Tx buffer is empty, conflict can occur. It is possible for ESCC to export data instead of interrupt vector. Avoid simultaneous enabling of DMA and Interrupt mode data transfers to the ESCC.

4. When ESCC is used in divide-by-two mode, there is a possibility for ESCC Ch. B to cease requesting interrupts. Due to clocked signal paths that are doubled with respect to 2180 system clock, the following software workarounds are suggested:

   Workaround: If INT mode 2 is used for the ESCC, there is a possibility for lower priority interrupts to remain pending without asserting internal interrupt request. If ESCC clock divider is enabled, place ESCC reset highest IUS commands in the main loop of code to kick interrupts, if this condition occurs. When using WR1 to disable interrupts, place a NOP command immediately after disabling to allow for longer $\overline{\text{INT}}$ deassertion when using ESCC in divide-by-two mode.

5. $\overline{\text{HRxRDY}}$ Assertion. When using the MIMIC in conjunction with the Receive timers, $\overline{\text{HRxRDY}}$ may assert erroneously before the Receive timers elapse. This may result in multiple reads of the RBR FIFO when the Host DMA uses the $\overline{\text{HRxRDY}}$ signal for the DMA request.

6. $\overline{\text{IOCS}}$ Error on 16-Cycle Delay. $\overline{\text{IOCS}}$ may be asserted erroneously during interrupt acknowledge cycle following wakeup from sleepmodes.This error can occur when the 16-cycle delay on Halt Recovery feature is enabled (bit 0 if Int/EdgeMux register), $\overline{\text{IOCS}}$ is enabled, and sip address is within address bounder of $\overline{\text{IOCS}}$. Since the

$\overline{RD}$ or $\overline{WR}$ strobe does not go active during the interrupt acknowledge cycle, $\overline{IOCS}$ assertion does not cause problems under most circumstances.

7. The $\overline{HTxRDY}$ signal may have problems because of a possible glitch in the signal. The $\overline{HTxRDY}$ signal, known as the Host Transmit Ready signal is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. The glitch in the signal causes the $\overline{HTxRDY}$ signal to go active when there is still 1 byte of data left in the buffer, thus preventing data to be properly serviced.
8. The $\overline{INTO}$ Assertion on MIMIC Access Feature (Bit 2 of the Z80182 Enhancements Register) when enabled causes a low edge on the $\overline{INTO}$ pin during any HOST access to the MIMIC when the $\overline{HALT}$ is active (Power Down). Bit 2 is found to be the opposite as that defined in the technical specification of the Z182H. Instead of enabling this feature by setting bit 2 to a 1, this bit is enabled by resetting the bit to 0. In the previous 21 82 device, bit 2 of the Z80182 Enhancements Register was reserved at 0; therefore this feature becomes enabled.

   Workaround: If this feature is not desired, set Bit 2 of the Z80182 Enhancements Register to 1.

Z80182 Limitations

1. The Fast MIMIC Interrupt resolution is not functional. The MIMIC highest IUS bit may become set if ESCC and MIMIC requests interrupt service simultaneously and ESCC processes the Interrupt Acknowledge. Although interrupt priority selection arbitrates which device processes the Interrupt Acknowledge, the MIMIC IUS bit can become set while the ESCC exports an interrupt vector. All MIMIC and lower priority interrupts is disabled until the MIMIC highest IUS bit is cleared.

Workaround: Keep bit D0 of MIMIC Modification register (xE9h) disabled. Place a reset highest MIMIC IUS command in the root program, which ensures that the MIMIC IUS resets when this bit is set erroneously.

2. The RTO Time-Out Enhancement feature (Bit 1 in the FSCR register) is not functional.
3. Z180 DMA/MIMIC RBR.

   In the MIMIC Master Control register, RxDMA Enable (Bit D4) does not function. Program this bit as 0. While in 16450 non-FIFO Mode, the RBR DMA request to the Z180 DMA does not assert and causes RBR FIFO overrun.

   While in 16550 FIFO Mode, the RBR to Z180/DMA request de-assertion is delayed. The extent of deassertion delay deteriorates by operation at high speed, low-voltage, or high temperature. Using this DMA Request in level-triggered DMA Mode may cause RBR overruns. The effects of the delay are reduced by adding I/O Wait States in the DCNTL register, using the edge-triggered DMA Mode, or by ensuring 5.0 V operation.
4. MIMIC DMA on both MPU and PC Interface has timing problems or asserts DMA requests erroneously. MIMIC DMA is not usable.
5. In previous 182 versions when an ASCI overrun error occurs, the microprocessor would set the OVRN Error (bit 6 of STATO or STAT1). Once FIFO space became available, the receiver would automatically start putting data into the FIFO. Any character that is completed while the FIFO is full would naturally be lost. Since the data transfer was automatically restarted, it was impossible to determine what data is missed.

   For SL1932 and SL1933, once an overrun occurs, the receiver does not place any further data in the FIFO, until the “last good byte

received" has come to the top of the FIFO so that the Overrun latch is set and software then clears the Overrun latch. Assembly of bytes continues in the shift registers, but this data is ignored until the byte with the overrun error reaches the top of the FIFO and is cleared with a write of 0 to the EFR bit. This allows the user to determine exactly which data bytes were lost.

Workaround: To begin transmitting data in the FIFO, clear the overrun flag by resetting Error Flag Reset (bit 3 of CNTLA0 or CNTLA1)

6. When CTS1 E is set (bit 2 of Reg 05H), bit 5 of Reg 03H reflects the stat of the multiplexed rxs/cts1 pin. This bit always shows 0.
7. When the TE is set to 0 (Bit 4 of CSIO Control Register), the txs pin is held high. The txs therefore is high before a transmit starts and returns high on the rising CKS edge after the 8th bit has been transmitted.

   This may become an issue if the last bit send is a 0 and the data is being sampled on the rising edge of the cks clock, since an incorrect "high" states may be sampled rather than the actual correct 8th bit.

Z85230 ESCC Precautions

- IUS Condition Description.
  The fault occurs under the following conditions:
  - SDLC 10x19 Status FIFO is enabled
  - Interrupts on Rx Special conditions only

  This mode is intended for an application where received characters are read by a DMA controller. EOF (End Of Frame) is treated differently from other special conditions. For example: parity error, overrun error and CRC error in this mode.

When EOF is detected:

– Receive Character Available (RCA) interrupt is generated versus Special Conditions Interrupt in other operating mode.
– The data FIFO is not locked versus locking the data FIFO in other operating mode. This is known as “Anti-Lock” feature where:

  This allows the processor services the EOF interrupt with more latency. Immediate attention from the processor is not necessary because the data FIFO is not locked. incoming data can still be Securely delivered to the Receive FIFO and subsequent incoming data is not lost. It allows for an operation with no servicing at all of the interrupt.
– When the EOF interrupt (RCA interrupt) is serviced, the processor must use the Reset Highest IUS command to clear the EOF interrupt.
– If EOF interrupt happens when another lower priority interrupt is enabled. For example: ext/status interrupt is being serviced, the Reset Highest IUS command issued by the lower priority interrupt service routine (to clear out the pending interrupt) can also accidentally clear the pending EOF interrupt.
– The Reset Highest IUS command clears the IP bit related to the EOF (in this mode, RCA IP bit) regardless of the priorities of the pending interrupts. This causes a problem when the following circumstances are gathered:
  • Another ESCC interrupt is being serviced (For example: Ext/Status interrupt for Transmitter Underrun in Full Duplex operation).
  • The DMA reads a byte marked with the EOF. The corresponding IP bit is set and the $\overline{\text{INT}}$ line goes low/highest priority interrupt in the daisy chain).
  • The processor does not acknowledge this interrupt at that time, because it is servicing another interrupt.

The processor finishes servicing the other interrupt and uses the Reset Highest IUS command.

This resets the IP bit corresponding to the EOF, and the EOF interrupt is lost.

Workaround:

1. Alternate Operating Mode.

   A very similar operating mode can be used to achieve the same functionality with minimum code modifications. The ESCC operates in “receive interrupts on first character and special condition,” instead of “receive interrupt on special condition only.”

   In this made, the anti-lock feature is not enabled. The FIFO is locked after the last character of a frame has been transferred, and the interrupt condition does not disappear until after a “Error Reset” command is issued to the ESCC. No “Reset Highest IUS” command can clear any IP bit.

2. Use of the Daisy-Chain.

   This workaround uses the following two conditions:
   - If only one channel is used, the EOF interrupt is the highest priority interrupt. As soon as it occurs the $\overline{\text{INT}}$ pin goes Low, requesting an interrupt to the CPU.
   - Channel A is the only channel issuing interrupts.

     If both conditions are satisfied, allowing nested interrupts can solve the problem.

     The processor servicing an interrupt on the daisy chain must be interruptible again from another interrupt of higher priority on that same daisy-chain.

3. Use of RR7 Register.

   This workaround is applicable if EOF interrupt is only used to notify another part of the software that there has been another frame received:

   – After issuing the Reset IUS command, read RR7.
   – Check bit 6 of RR7. This bit indicates that the SDLC frame FIFO contains a valid frame. Although one interrupt may have been lost (IP reset) by the Reset IUS command, bit 6 of RR7 always indicates that at least one frame is available in the frame FIFO.
   – If bit 6 of RR7 equals 1, notify the concerned part of the software that at least one frame is available in the frame FIFO.

4. Conclusion.

   When the SDLC FIFO is enabled and “Receive Interrupts on Special Conditions Only” is selected, software needs to check whether there is a Receive Character Available Interrupt, which is generated by DMA reading an EOF character, before issuing the “Reset Highest IUS” command. Otherwise, the EOF interrupt conditions were cleared out by the command (Figure 32).

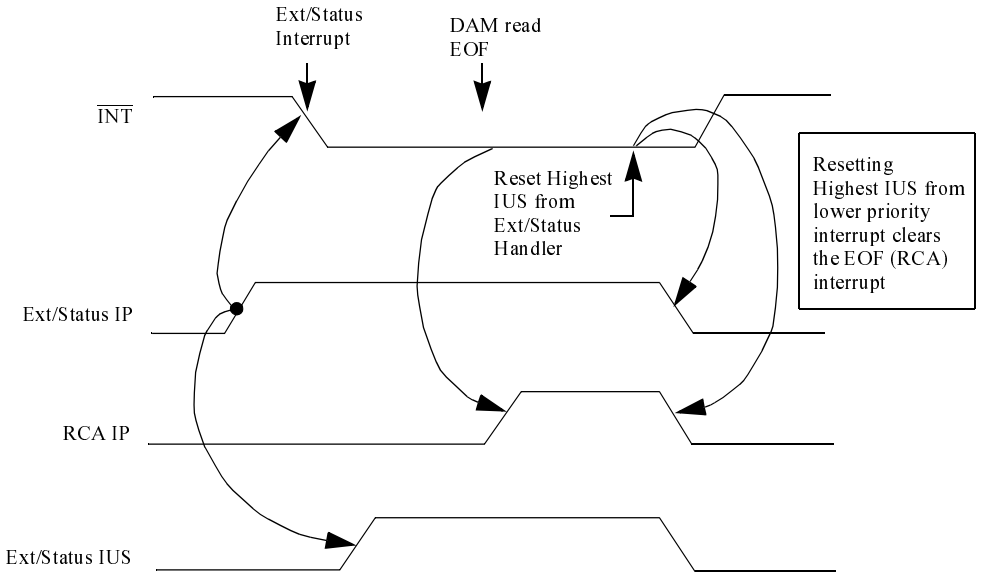


Figure 132. Resetting Highest IUS From Lower Priority

RTS Condition Description

The Z85230 has identified a functional problem in “Automatic RTS De-activation”.

This mode is intended for SDLC applications where the $\overline{RTS}$ signal from the ESCC is used to enable a line driver in multi-drop line communications.

Before the frame transmission, $\overline{RTS}$ is asserted by “Activate RTS” command (WR5 D1 = 0). After the last data bit of a frame is sent, transmit underrun interrupt is generated. “De-activate RTS” command is issued (WR5 D1 =1) to de-activate the $\overline{RTS}$ signal for turning off the line driver after the multiple-frame packet is completely sent.

In SCC, the processor needs to monitor the data line to make sure that the frame is completely gone before the “De-activate RTS” command is issued.

In ESCC, $\overline{RTS}$ can be programmed to de-activate automatically after the frame is completely sent without requiring additional monitoring if the following sequence is followed:

- Automatic $\overline{RTS}$ De-activation is enabled (WR7‘ D2 = 1)
- CRC/Flagon Underrun is enabled (WR10 D2 = 0)
- At transmit underrun interrupt service routine, issue ’Deactivate RTS’ command.

  Consequently, the $\overline{RTS}$ signal de-activates automatically after the closing flag is gone.

The “Automatic RTS Deactivation” is working properly in single frame and two consecutive frames in back-to-back, but not in multiple back-to-back frames where more than two frames are in back-to-back.

In multiple back-to-back frames transmission, if the ’Deactivate RTS’ command is issued at the beginning of the transmit underrun interrupt service routine, /RTS is de-activated after the CRC has gone, but before the closing flag is sent. Because the last frame is not correctly concluded, the frame becomes corrupt.

Workaround:

A workaround to the “RTS Bug” is not to send back-to-back frames. Idle time is inserted in between frames. Workaround Limitations:

The system throughput is reduced by the idle time inserted between frames.

Automatic TO Forced High in SDLC, NRZI, Mark Idle Condition Description

If WR10 is programmed with D6, D5 = 01 (NRZI), D3 = 1 (Mark Idle) and WR4 D5,D4 = 10 (SDLC), TxD pin is forced high after detecting the last bit of the closing flag at the falling edge of the TxC. This feature does not work properly if back-to-back frame is sent. The TxD output is automatically forced high for the duration of eight bit times and the first byte of the second frame is corrupted. In a multiple frame transmission, a zero bit was inserted before the opening flag of the second frame.

Workaround:

Send back-to-back frames in Flag Idle: Since the “Automatic TxD forced high” feature is having problems only if all the following conditions are gathered:

- Back-to-back frame transmission
- NRZI
- Mark Idle

Setting the system in Flag Idle mode (WR10 D3=0) in frame transmission allows back-to-back frames to be correctly sent without any data corruption.

SDLC FIFO Overflow Condition Description.

In SDLC mode, D7 of RR7 (FIFO Overflow status bit) is set if the 11th frame is written to the 10X19 SDLC status FIFO while the FIFO is full, (that is, 10 frames have been accumulated in the Status FIFO and have not yet been read by the Processor). Under this circumstance, the status FIFO is locked and no data can be written to the Status FIFO until D7 of RR7 is reset.

1. If the ESCC is set up in Anti-Lock mode, that is, the SDLC FIFO is used when “Receive Interrupts on Special condition only” is enabled, the only way to reset D7 of RR7 (the FIFO Overflow bit), is to reset

and set D2 (SDLC FIFO Enable Bit) of WR15. This causes the SDLC FIFO to be reset and all the SDLC frame information to be lost.

2. With no Anti-Lock feature, the FIFO Overflow status bit is reset if SDLC FIFO is read.
3. If the ESCC is setup in NRZI and Mark Idle in back-to-back frame transmission, once the FIFO Overflow bit (D7 of RR7) is set, the only way to reset the status is to reset and set D2 (SDLC FIFO Enable Bit) of WR15. This causes the SDLC FIFO to be reset and the unprocessed frame information stored in the SDLC FIFO to be lost.

Workaround:

Do not use “Receive Interrupts on Special Conditions Only” and Mark Idle if there is a possibility of Status FIFO Overflow.

Default RR0 Value Condition Description.

D7 of RR0, Break/Abort status bit, is not consistently cleared after reset.

Default RR10 Value Condition Description.

D6 of RR10, Two Clock Missing bit, is sometimes erroneously set to indicate that the DPLL detects a clock edge in two successive tries after hardware reset.

Workaround:

Ignore the first D6 value read from RR10 after hardware reset.

CRC Condition Description.

The CRC cannot be interpreted correctly from the Receive FIFO when one or two residue bits are sent. The CRC value is correctly received and checked but is not loaded to the Receive FIFO properly.

Two Residue Bits

(Residue code =’000’)

The last three bytes of the Receive FIFO read:

Bit 6 and 7 of the CRC are lost.:

D7	D6	D5	D4	D3	D2	D1	D0
C6	C5	C4	C3	C2	C1	CO	D8
C15	C14	C13	C12	C11	C10	C9	C8

One Residue Bit

(Residue code =’111’)

The last 3 bytes of the Receive FIFO read:

D7	D6	D5	D4	D3	D2	D1	D0
C6	C5	C4	C3	C2	C1	C0	D8
C15	C14	C13	C12	C11	C10	C9	C8

Bit 7 of the CRC is lost.

The CRC is received and loaded properly into the Receive FIFO in other situations, i.e., 0,3,4,5,6,7 residue bits.

The Residue Code (bit 3,2,1 of RR1) is reported correctly independent of the number of residue bits sent.

Workaround:

Ignore the CRC value read from the Receive FIFO if one or two residue bits are sent. 1.

1. In the Z80182 Product Specification, DC-832201 for Write Register 9 of the ESCC Control Registers, there is a documentation error. For bits D7 and D6, it reads:

D7	D6	
0	0	No Reset
0	1	Channel Reset B
1	0	Channel Reset A
1	1	Force Hardware Reset

2. In the Z80180 User's Manual, there is a documentation error regarding the description of the ASCIO $\overline{DCD0}$ function on the Z182. On page 33 of the Z80180 Users Manual, DC-8276-04 it reads, "Even after the $\overline{DCD0}$ input goes LOW, these bits do not resume normal operation until the status register (STATO) is read." This is incorrect. It should read, The RDRF and Error Flags become functional again once the $\overline{DCD0}$ is asserted, regardless of reading the STATO register."

Note: The Z80182 SL1932/SL1933 has a Revision Register (Z182 MPU Address %DA, Value = 0x9F) which allows for software to differentiate (if needed) between Z80182 revision K and older Z80182 devices. A value of 60 hex is used for this revision. Previous revisions of the Z182 did not have Revision Register feature.

3. Mode 0 Interrupts require PHI/2
4. Mode 0 interrupts from the ESCC pass the correct vector/opcode only if bit 3 of the Z80182 Enhancement Register (I/O address xxH9H) is 1 to select "ESCC clock is PHI/2"

5. Mode 1 Rx interrupts read Rx FIFO
6. If, at the time of a Mode 1 Rx data interrupt from an ESCC channel, the Program Counter address on the A7-1 lines matches the I/O address of that channel, and A0 is 1 to select Data rather than Control, the interrupt acknowledge cycle (which is performed even though there is no opcode nor vector to be communicated) removes the oldest received character from the Rx FIFO.