High Power Two-Phase Digital Power Factor Correction

Reference Design
IXRD100401-0916

Overview

This reference design builds upon IXYS Corporation's Digital Power Control technology and extends it to high power levels in the area of Power Factor Correction (PFC). It introduces fast switching, high current, high voltage X2-class MOSFETs and incorporates Digital Inrush Current Control concepts (IXYS reference designs IXRD1001 and IXRD1002). Functional control is based upon Zilog's 8-bit Z8F6481 microcontroller, a member of the Z8 Encore! XP F6482 Series of MCUs.

High power (1 kW and above) AC to DC converters with active PFC are designed to solve specific issues arising at high power, including the following:

- Decrease high current ripples at PFC switching frequency in the input power line
- Maintain fast low-loss transfer of high inductor's current from the switching device to the load
- Provide efficient conversion in a wide load range
- Decrease high frequency electromagnetic interference (EMI) caused by PFC switching devices operating at high current and voltage
- Decrease EMI caused by oscillations in the inductor during discontinuous mode at low load that are a result of transforming energy stored in stray capacitance/inductance
- Design a low loss high frequency inductor to store and efficiently pump energy into the output bulk capacitor
- Develop a robust current-balancing technology for polyphase PFC topology to reduce current ripples in the input power line
- Create overload and overvoltage protections to ensure reliable performance in unexpected situations for the end-user

In this reference design, input AC power line current ripples are reduced by using two-phase interleaved conversion with pulse density modulation at low power. After the power drops below 50% of maximum rated power, the second phase is disabled to reduce switching losses, while the microcontroller adjusts appropriate parameters to continue an uninterrupted conversion.

The quasi-resonant mode is used to reduce EMI during high power conversion, while the device operates in discontinuous mode with an active snubber at lower power. The selected conversion frequency is in the 100 kHz range, which allows for a decrease in component size yet provides high enough wattage for power range devices.

The inductor current switching time is reduced to 10–15 ns depending on current value, which is in the range of 12–18 A at 140 V–105 V AC input power line voltage respectively. Fast switching is achieved by using fast X2-class MOSFETs and appropriate decoupling and layout (For more information, refer to the device documentation). The inductor is built with high frequency E-core and Litz wire coil to obtain high efficiency at high switching frequency.

The two-phase interleaving architecture used in this reference design requires thorough current balancing to avoid high frequency modulation in the AC input power line current. To solve this problem, the MCU controls the position of the peak current for each phase and centers the secondary phase peak in between the primary (master) phase peaks.

Additionally, the MCU-based digital control optimizes the converter's overall performance including limiting inrush current, programmable overload protection schemes, and high power factor of conversion, which gives this device a competitive advantage in high power applications.

Features

The High Power Two-Phase Digital Power Factor Correction reference design offers the following features:

- Conversion power, maximum: 1.06 kW @120V power line
- Input Voltage: 105 –140 V AC 50/60 Hz
- Output Voltage: 400 V ± 2%, programmable
- Output Current: 2.65A @400V
- Output Voltage Ripples: <6% at full load
- Input Current Ripples: <2%
- Load Variation Range: >8x
- Device Conversion Frequency : 100–120 kHz at high power
- Programmable Overload, Overvoltage, and Brownout Protection
- Digital Inrush Current Control
- Soft Start mode
- Power Good status

Potential Applications

This reference design provides a platform for developing a variety of power management applications using AC–DC converters with IXYS power devices and an MCU, including the following applications:

- Medical equipment
- Battery charging
- Air conditioning systems
- High power LED lighting
- Welding equipment

This design may be used at input voltages 220V/240V with minor modifications to the input voltage sensing schematic providing reference voltages to DAC and MCU measurements. Depending on customer requirements, MOSFET current sensor gain may also be changed.

Note: The source code file associated with this reference design, IXRD1004-SC01.zip, is available for download for free from the IXYS Power and Zilog websites (www.ixyspower.com and www.zilog.com). This source code is tested with ZDS II–Z8 Encore! version 5.2.0. Subsequent releases of ZDS II may require you to modify the code supplied with this reference design.

Description

Power factor correction is implemented using two-phase interleaved boost type conversion architecture, as shown in Figure 1. For Phase 1, it is executed with inductor *L1*, switching device *T1*, and diode *D1*. For Phase 2, boost conversion is accomplished with *L2*, *T2*, and *D2*. High Power factor is achieved by adjusting a peak current value with respect to rectified input voltage, which is used as a reference V_{IN}. Peak currents are captured with sense resistors *Rs1* and *Rs2* and amplified to a range of 2 V.

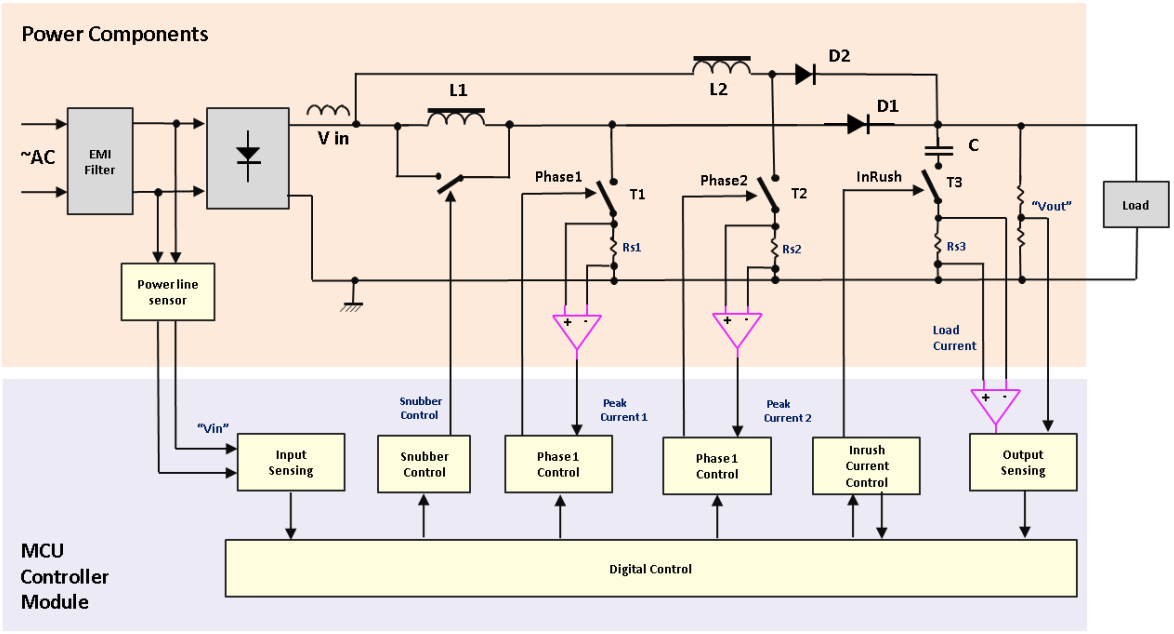


Figure 1. Block Diagram of the Digitally Controlled Power Factor Corrector

Due to high current values, the inrush current at start-up is digitally controlled and the bulk capacitor's C pre-charge is performed in switching mode by switching device T3, along with inductors L1 and L2. The digital inrush current control concept utilized here is published in IXRD1001.

Current sense resistor Rs3 is used to monitor bulk capacitor's C current and the load current. It is also responsible for the overload protection functionality. Load current is sensed during zero crossing of the input AC voltage, when the inductor is discharged and capacitor C is the only source of energy provided to the load. At this moment, the capacitor's current is equal to the load current. This allows connecting the load to the rectifier's ground directly and eliminating the current sensing resistor in between.

The overload protection is continuously active with the comparator set to monitor the load current. In an event of overload, the comparator shuts down conversion. The MCU can be programmed to wait for a predetermined period of time and attempts to restart the converter. Additional programmable features include the number of restarts and the period between attempts.

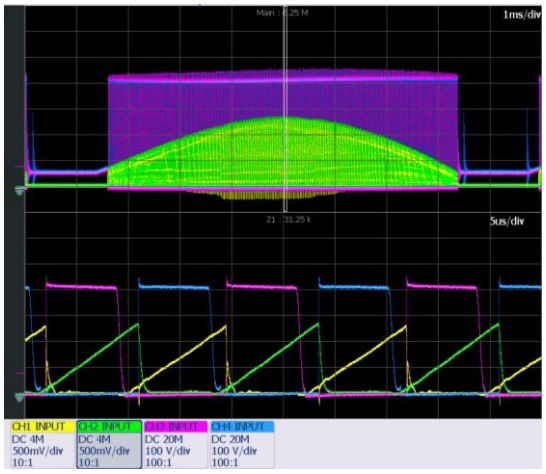
Overvoltage protection is based on measuring output voltage during the zero crossing time frame and comparing it to the programmable overvoltage reference. If overvoltage occurs, the device is shut down to prevent high output voltage in case of low load.

Principles of Operation

The following operational principles are considered for high power two-phase PFC:

- Peak inductor current modulation was chosen over other PFC topologies aiming at high power conversion.
- Quasi-resonant mode is used as a version of critical conduction mode, allowing inductor voltage to drop to its lowest value in resonant process with strain capacitance after the inductor is discharged into a load.
- The second conversion phase is set as slave with respect to the first "master" phase.
- The balance of the second phase current with respect to the master phase is performed using hardware and software.
- Low power consumption (less than half of peak power) forces the second phase into sleep mode.
- Pulse density modulation is used in addition to amplitude modulation to maintain efficiency of conversion.
- An active snubber is used to reduce stray oscillation after the inductor is discharged into a load
- A Look-Up Table (LUT) is used to simplify calculations performed by the 8-bit MCU.
- Prediction control is performed with LUT assistance. Prediction is set to about 90% of expected output parameters.
- Digital feedback is used to keep output parameters in the predetermined range.

Peak Inductor Current Modulation – Peak inductor current modulation allows the average line current to copy a form of the AC line input voltage, which is used as a reference. In this design, DAC is used to provide reference voltage for peak current modulation. A rectified and scaled input sine wave is applied to analog DAC input, while digital DAC input is used to control amplitude of DAC output in accordance with prediction and feedback control. See Figure 2 for reference.



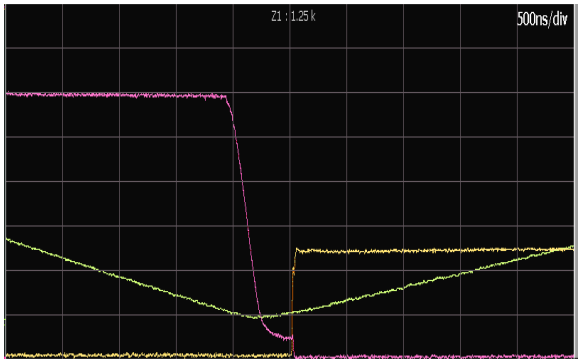
Legend:
Blue and Magenta – First and second inductor voltages
Green and Yellow – First and second inductor charging currents

Figure 2. General Waveforms of Two-phase MCU-controlled PFC Converter

In Figure 2, the peak inductor current amplitude is 12 A at AC input of 120 V, and voltage on the inductor is 400 V. The bottom of the scope snapshot is a zoom-in of the top portion of the area between two white lines.

Switching operations are disabled near the zero crossing area of the AC input voltage to improve efficiency by avoiding switching at low input voltages, when the voltage cannot be boosted to the required output level.

Quasi-resonant Mode – The MCU maintains quasi-resonant mode by tracking the point of the inductor's discharge and providing the necessary delay before turning the inductor's current on again. The delay value may have some variance because the inductor voltage has a dull bottom plateau. The inductor current changes smoothly as shown in Figure 3.



Legend:
Magenta – First inductor voltage
Green – First inductor charging current
Yellow – Gate voltage for first phase MOSFET

Figure 3. Quasi-resonant Mode Waveforms

Quasi-resonant mode of operation is maintained at high power until power consumption approaches half of peak power, after which pulse density modulation is applied to keep up with efficiency of conversion.

Second Conversion Phase – This phase is synchronized with the master phase. Synchronization is implemented through delay of the beginning of the second phase conversion cycle with respect to the first phase timing.

Balance of Second Phase Current – This is required for reduction of ripples in the input power line. This reference design allows the following phase synchronization options for current balancing:

- The second phase conversion starts after the master inductor's current falls to zero
- The second phase conversion starts when the master inductor's current falls to the predetermined level
- The second phase conversion starts after a delay time that is required to keep both phases' currents balanced, based on previous conversion cycle values.

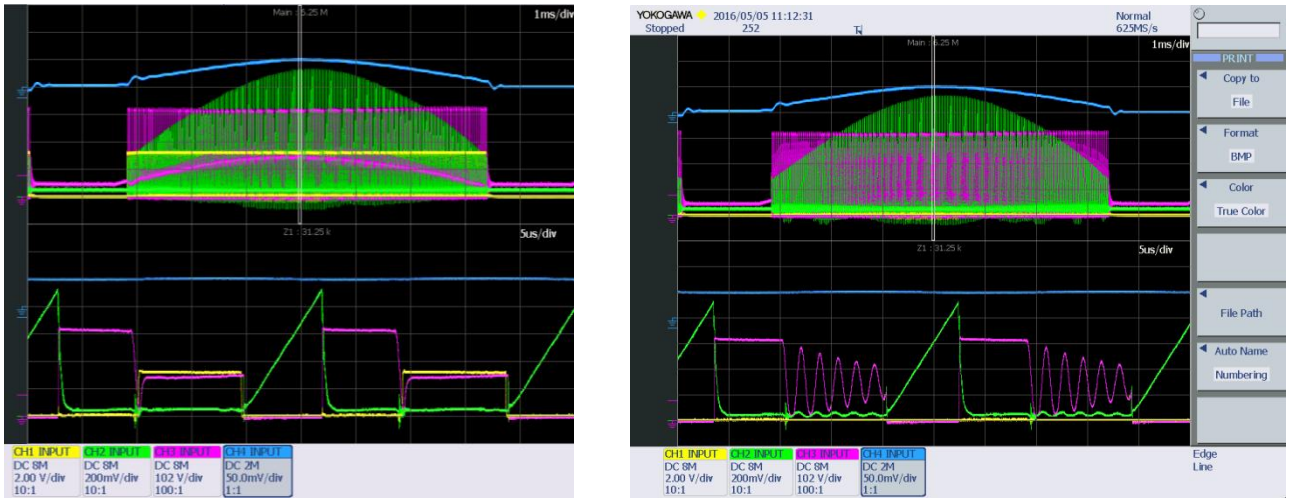
The selection is implemented by setting appropriate zero Ohm resistors on the MCU controller board. The resistors corresponding to the options listed above are *R15*, *R18*, and *R8* respectively (see schematic in Figure 14).

Low Power Consumption – This state is detected by measuring load current while output voltage V_{OUT} is maintained in the specified range. Load current is measured during AC input voltage zero crossing, where conversion is halted, thereby allowing for improved accuracy. Voltage drop on the current sensing

resistor is amplified with inversion into positive voltage domain. If load current drops below half of the maximum rated value, the second phase conversion is halted.

Pulse Density Modulation – This is used to further reduce generated power, if power consumption falls more than half of the rated power.

Active Snubber – This is activated at low power consumption during the time frame from inductor discharge to the start of the next conversion cycle. Snubber timing is generated by the MCU. An illustration of active snubber performance is shown in Figure 4.



Legend:
Magenta – First inductor voltage
Green – First inductor charging current
Yellow – Gate voltage for first phase MOSFET

Figure 4. Inductor Voltage with Snubber Active (left) and Snubber Disabled (right)

Look-Up-Table (LUT) – The LUT simplifies MCU operations to speed up the algorithm. The data for LUT is converted to an 8-bit representation. The main LUT data contains load impedance, which is estimated by measuring output V_{OUT} and load current *iLoad*. Load impedance is more informative because it is estimated not only in steady state, but also in transition modes, when V_{OUT} is not settled yet. For simplicity of MCU operation, the load impedance is calculated as *R_Load*. The $R\_Load = f(iLoad, V_{OUT})$ equation is represented in Figure 5, where *iLoad* is the horizontal axis. The axis values are scaled to an 8-bit representation. The LUT base algorithm is also used in prediction control.

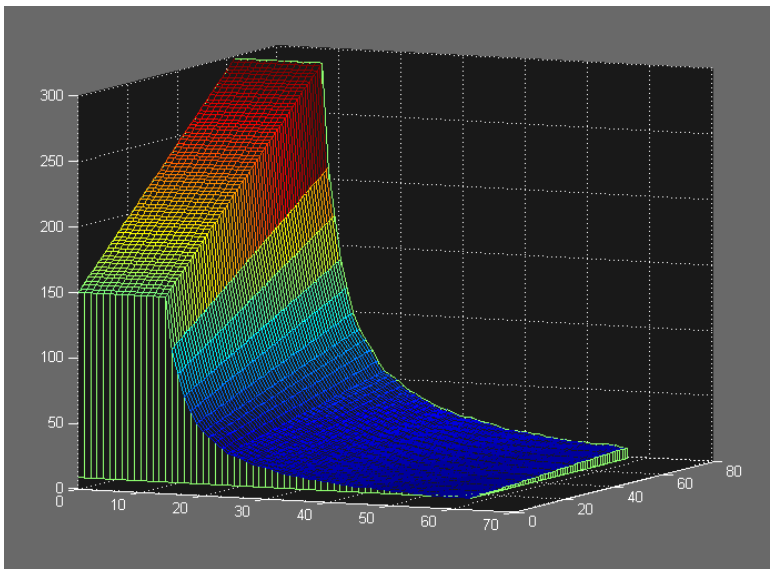


Figure 5. Two-dimensional Representation of *R_Load* in LUT

Prediction Control – This sets the initial values for peak value of inductor current *DACdata* supplied to DAC digital input and for delay of the next conversion pulse (indicated as *Delay)* to modulate pulse density.

Empirically obtained *DACdata* is a convoluted result of the influence of input voltage V_{IN} and load power consumption P_{OUT}. V_{IN} influences on converted power in inverse square dependence as $1/V_{IN}\hat{}2$. The input voltage range is from 105 V to 140 V, which is scaled to ADC input for measurement from 1.72 V to 2.4 V as shown in Figure 6. The power load is set from 60 W to 1070 W. The actual power values used are shown in the colored legends in the top right corner of Figure 6.

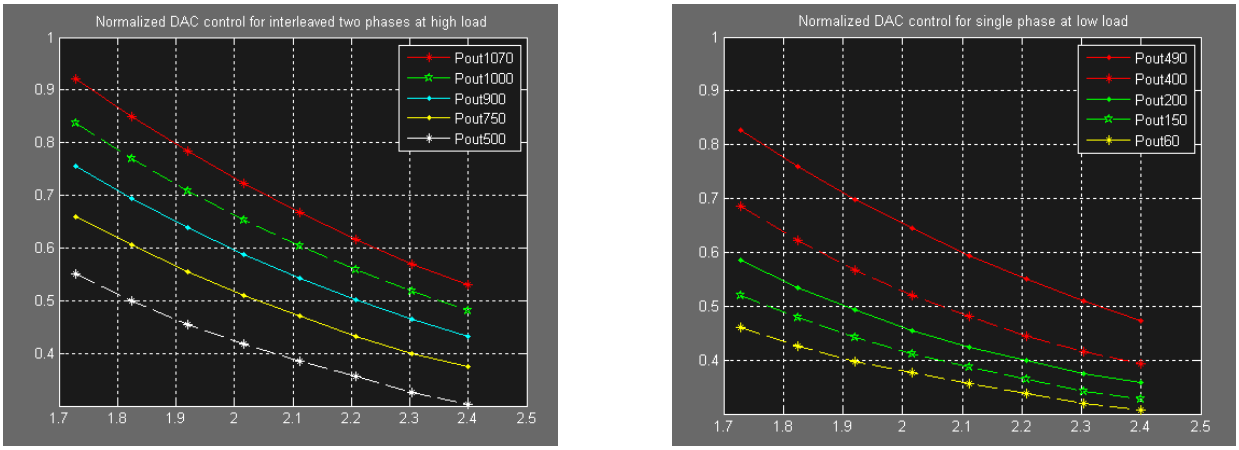


Figure 6. DACdata Sets for Two-phase (left) and Single-phase (right) Conversion Modes

The prediction LUT is constructed as a 2D LUT representing *DACdata = f(V_{IN}, R_Load)*. Prediction LUT is shown in Figure 7 in actual 8-bit data values along the X axis for V_{IN} and Y axis for *R_Load*.

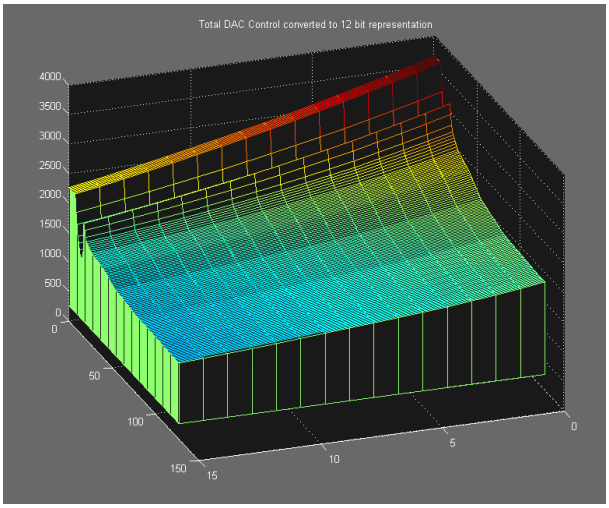


Figure 7. Prediction of *DACdata* as a Function of V_{IN} and *R_Load*

Another prediction LUT used is for delay prediction as a function of R_Load, Delay = f(R_Load). The Delay is zero at low R_Load (high power), then there is a little peak of delay at two-phase conversion because the *DACdata* drop was not enough for steady performance, after which *Delay* steadily increases with reduction of power (increase of *R_Load*), as shown in Figure 8.

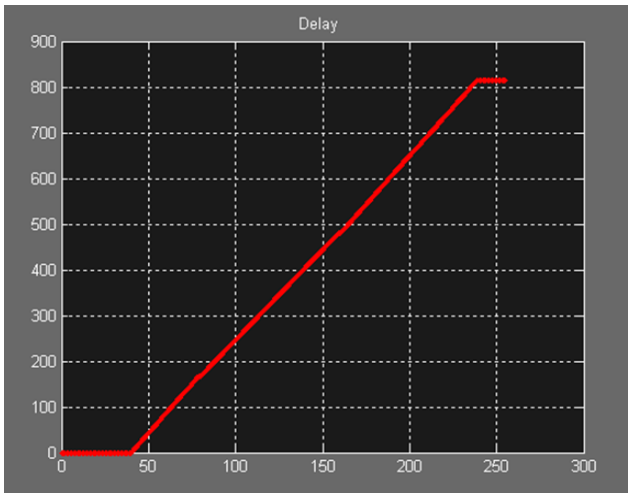


Figure 8. Prediction of *Delay* as a Function of *R_Load*

Digital Feedback – Digital feedback finalizes the conversion algorithm as it modifies *DACdata* loaded as prediction value with feedback control value. The overall algorithm of feedback and its addition to *DACprediction* value is shown in Figure 9. The feedback control value is calculated once per half period at zero crossing, to be loaded into registers as a conversion time for following half of the sine wave period. The calculations are performed at 16-bit resolution in order to have smooth DAC control, which is of 12-bit resolution. The feedback data consist of two terms: integral term *iTerm* and differential term *dTerm*. The differential term functions as lead control to increase the stability of the control loop while reducing the settle time. *KD* and *KI* constants are used to balance the ratio between terms, while *KE* sets the feedback gain.

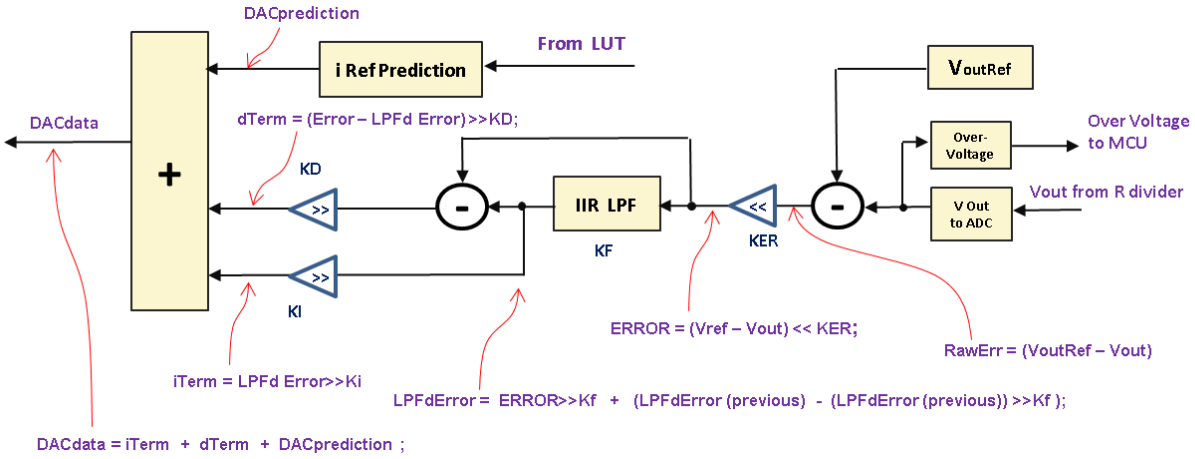


Figure 9. Feedback and Prediction Control Algorithm

Hardware Implementation

IXYS' MCU-controlled PFC, which consists of an MCU Module and a Main Power Board, is shown in Figure 10. The detailed circuit schematics are shown in Appendix A . The MCU Module is implemented as an add-on device powered by an auxiliary +3.3 V power supply. It contains a connector for MCU programming because the MCU is required to be programmed before powering the entire system.

The Main Power Board is a two-layer surface-mount board that provides easy access to test points. Diode bridge *BR1* (see Appendix A for schematic diagrams), MOSFETs *Q1*–*Q3*, and boost diodes *D3* are mounted on heat sinks. Power dissipated on the MOSFETs is less than 16 W at a 1000 W output power. This board may be powered from a 50 Hz or a 60 Hz 105 V to 140 V AC source. The connector *J1* is used to provide auxiliary power supply +3.3 V for the MCU and 12 V for the gate drivers on the Main Power Board.

Figure 10. MCU Module (left) and Main Power Board with MCU Module (right)

Setup and Test Results

This reference design has been tested and its performance verified on a test bench as shown in Figure 11.

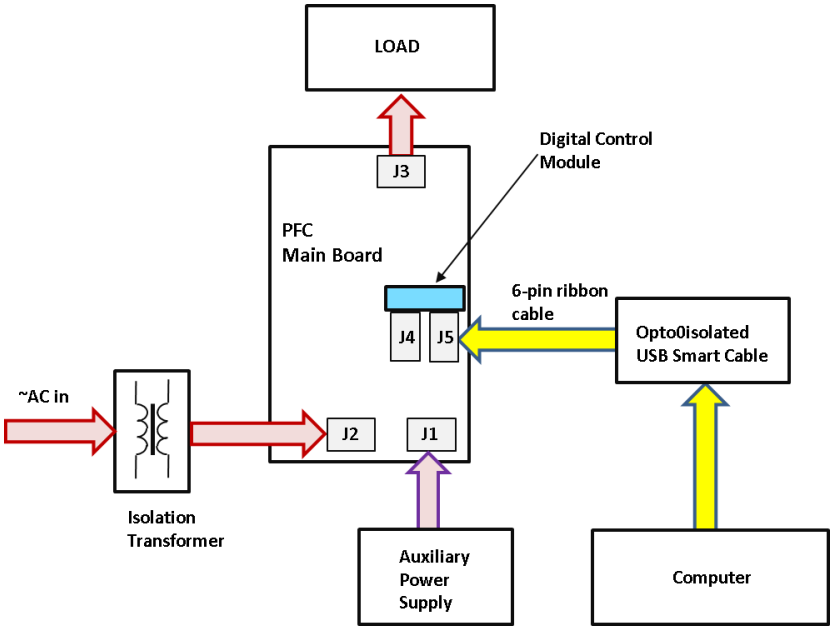
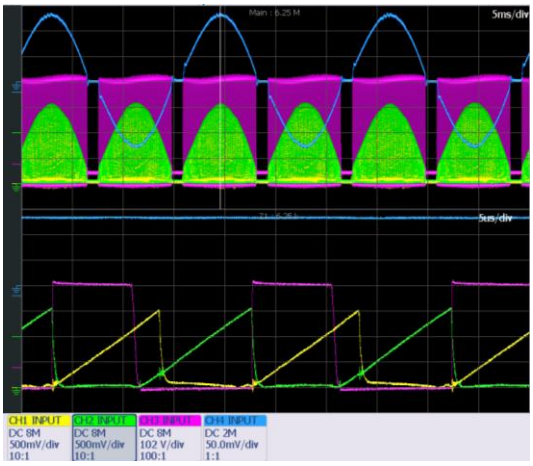


Figure 11. Reference Design Test Setup

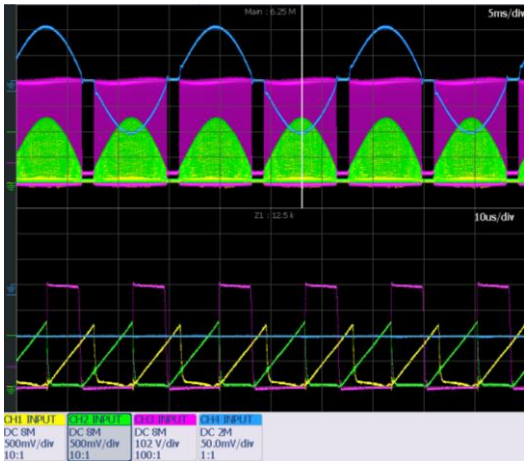
The AC line input was fed through a 2 kW isolation transformer to protect the operator and test equipment. The load was set to consume 2.5 A during normal operation. To test overload conditions, an additional load was used to add .25 A current. An instantaneous connection of additional load was enough to trigger the overload protection functionality.

The auxiliary power supply should be turned ON after the AC power is ON. After a power-on reset and initialization, the MCU analyzes the power line, sets an appropriate timing, and begins pre-charging the bulk capacitor and then goes to normal operation mode. Performance of MCU-controlled PFC was tested at AC line voltage of 105 V, 120 V, and 140 V. Actual waveforms taken from a scope at the normal operation are depicted in Figure 12.

Figure 12(a) shows scope waveforms at V_{IN} = 105 V and power = 750 W. Figure 12(b) shows scope waveforms for V_{IN} = 120 V at the same power. The inductor current (green line) dropped from 16 A to 12 A.



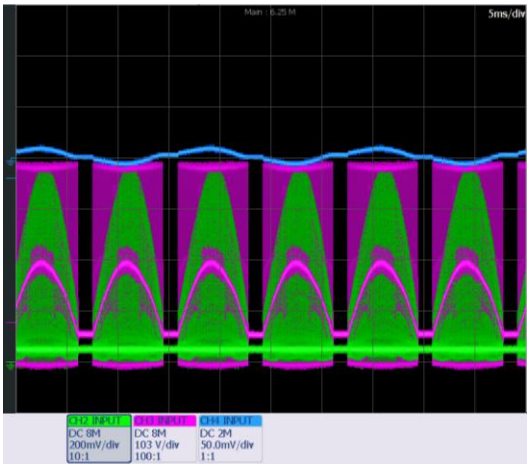
(a)



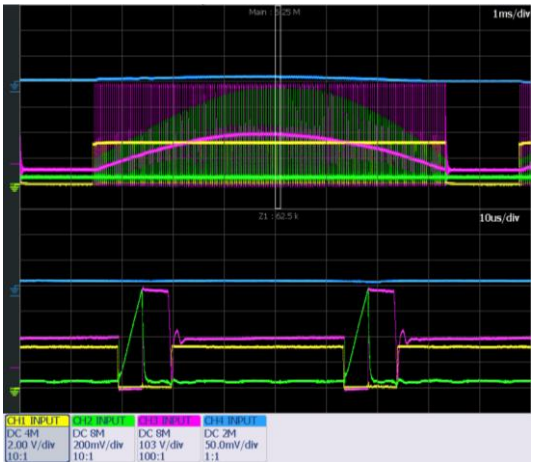
(b)

Legend:
Magenta – First inductor voltage
Green – First inductor charging current
Yellow – Second inductor charging current
Blue – Power line current

Figure 12(c) shows scope waveforms for V_{IN} = 140 V under conditions of low power of 100 W when peak current is reduced to 8 A while pulse density is also reduced as shown in Figure 12(d).



(c)



(d)

Legend:
Magenta – First inductor voltage
Green – First inductor charging current
Yellow – Snubber control signal
Blue – Power line current

Figure 12. Scope Waveforms under Different Conditions

Device Configuration and Control Setup

This reference design can be configured for different parameters such as output voltage, input voltage and frequency range, overload and overvoltage threshold, overload recovery time, and time position for Power Good status signal.

Development of the firmware that controls the operations of this MCU-controlled PFC reference design was completed using Zilog's Development Studio II (ZDS II – Z8 Encore! version 5.2.0). The following hardware components were used during the development of this reference design:

- USB SmartCable provides communication with ZDS II – Z8 Encore! version 5.2.0, debugging and downloading code into the F6281 Series of MCUs
- Connectors J4, J5 are 2x3, straight male header

Note: When connecting either device to the Reference Design Board, always ensure that pin 1 of the programming cable and pin 1of the connector on Digital control module are lined up.

Software Implementation

The source code for this design, IXRD1004-SC01.zip, is available free for download from the Zilog and IXYS websites.

Two Z8F6481 MCUs are used on the controller board. Therefore, the software is implemented as two projects, one for each MCU:

1) Main Processor
2) Mcu1Pfc – second processor

Main Processor Project

Source files

main.c - Main application file
initialization.c - Clock, pins, timers, ADC, DAC, OpAmp, and Comparator initialization \
isr.asm - Timer 2 interrupt to start ADC in a middle of Half-wave
vectors.c - Pins, timers0, 1, 2, ADC, DAC, OpAmp, and Comparator data

Header files, function prototypes

main.h
initialization.h
vectors.h

main.h – describes all hardware definitions

```
#define MAX_VOUT                    190     // max Vout before overvoltage in 8 bit scale
```

```
#define OVERVOLTAGE                 190
#define OVERLOAD                    240    // max current in 8 bit scale
#define MIN_INPUT_VOLTAGE           96     // min input voltage which initiate work.
#define MIN_VOUT_2_START_NORMAL 128        // minimal output voltage to start normal mode
```

The main.h file also defines the structures/unions used in the application.

UnInteger union – Used to access to word and MSB/LSB bytes of 16-bit unsigned word
enum BOARD_MODE – Used to define and switch between board modes:

```
typedef enum
{
        WAIT4SETTLE_MODE,           wait input voltage stabilization-
        MEASURE_PERIOD_MODE,        measure half-wave period
        MEASURE_IN_VLTAGE_MODE, measure initial input voltage
        INRUSH_MODE,                in-rush mode
        NORMAL_WORK_MODE,           normal work mode has two parts: soft start and normal work
        IDLE__MODE,                         reserved
        OVERLOAD_MODE,              reserved
        PROBLEM_MODE                reserved

} BOARD_MODE;
```

SETTLE_PERIODS = 10 - half-wave periods before start

Structure below is used to collect ADC readings:

```
typedef struct
{
        union unInteger  Vout;   - hold output voltage value
        union unInteger  i_ld;      - hold load current value
        union unInteger  Vin;       - hold input voltage value
        char Index;
        char ReadIndex;
} ADC_BLOCK;
```

main.c – Contents reference information about SVN version and compilation date for particular version. This information is stored with the code in a ROM and can also be accessed in the loaded application.

```
#define LOWEST_ADC_4_DELAY      3500  // max ADC value to use with ADC
```

rom unsigned int InrushCurrentOffTime[IN_RUSH_TABLE_SIZE] - holds delay for in-rush before turn on charging transistor.

R_LD_vs_Vout_32x128[][] - holds load resistance equivalent, defined as load current in horizontal axis and output voltage as vertical axis.
Load resistance limited at level 14 – as lowest and 240 as highest.

DelayTicksVsRload[] - defines delay in ticks for charging transistor.

TwoPhaseTable[] - defines when to start second processor .

Logic Flow

Disable interrupts,
Initialize all pins,
Configure Clock at 24MHz,
Initialize variables,
Configure Op amp,
Configure Timer 0,
Configure Comparator 1,
Configure Comparator 0,
Initialize DAC,
Configure Multi-Capture timer,
Configure ADC to measure input voltage,
Enable interrupt,
measure Wave half-period,
Configure Multi-capture timer for in-rush,
Start in-rush,
if in-rush succeed – start soft start.

Configure ADC for normal work,
Configure Timer 0 to use with output pulse,
Configure Timer 1 to use with output pulse,
Configure Timer 2 to start ADC to measure input Voltage in a middle of half-wave,
Configure start pin (event for pulses).

Soft Sart:
- Read and convert Input voltage, Load current and output voltage to use with tables,
- uses constant load resistance,
- load DAC and timer 1 with calculated values during inactive HALT,
- starts ADC to read load current and output voltage,
- starts timer 2 to read ADC at half-wave,
if soft start completed –normal operation starts.

Normal operation logic flow:
- Read and convert Input voltage, Load current and output voltage to use with Look Up Tables,
- Calculate load resistance to use with calculations,
- Correct error for DAC,
- load DAC and timer 1 with calculated values during inactive HALT
- starts ADC to read load current and output voltage,
- starts timer 2 to read ADC at half-wave,

Vectors.c:

ComparatorInt1():
- generates all board statuses,
- generates HALT signal and defines,

- defines when start timer to measure period,
- defines in-rush end status and switch to normal mode,
- manage enable/disable pulses generation by timer 1,
- manage event system activity.

MCU1Pfc – Second Processor

Source files:

initialization.c	- clock, pin, timers, ADC, DAC, OpAmp, Comparator initialization,
isr.asm	- timer 1,2 interrupt,
Mcu1.c	- main application part,
vectors.c	- pin interrupts.

Disables interrupts,
configure clock at 24MHz external quartz oscillator,
Configure comparator 0,
Configure Op amp,
Configure Timer0,
Configure Timer1,
Configure Timer2.
Configure Halt Pin,
Configure Multi capture Timer to measure half-wave Period,
Configure Start Pin.

Enable interrupt:
skips several pulses until stable,
during active halt – measure pulse length,
and generate if enabled by Two Phase high.

Isr.asm

timer2 - generates pulses
timer1 - measure pulse length
timer 0 – measure time between pulses

Equipment Used

The following equipment was used to build and test this reference design:

- Laboratory DC Power Supply GPS-4303
- Scope Yokogawa DL9140
- Multimeter FLUKE-179
- Isolation Transformer 2000W

See Appendix C for a list of materials used to build this reference design.

Kit Contents

The MCU-controlled PFC Reference Design Kit contains the following items:

- MCU Controlled Reference Design PFC device
- Opto-isolated USB SmartCable
- MCU Controlled PFC Reference Design Kit Insert

Ordering Information

This MCU-controlled Power Factor Correction Reference Design can be ordered from the IXYS Store or the Zilog Store using the part number listed below.

Part Number	Description	Store Product ID
IXRD1004	High Power Two-Phase Digital PFC Reference Design	RD10044

Results

Testing of this device was done at input line voltages ranging from 105 V to 140 V and loads ranging from 1060 W to 100 W. The device is capable of functioning at input voltages below 105 V with increasing peak currents over 18 A and up.

Summary

This High Power Two-Phase Digital Power Factor Correction reference design is a continuation of the digital power control design based on Zilog's F6481 series of MCUs, which offers flexibility in implementing a unique control algorithm that aids in maintaining efficient power systems. This reference design achieves a high level of efficiency, increased stability, and reliable performance across a wide range of input voltages and loads. Because of an innovative current measurement algorithm, this controller allows common input and load grounds. Users can optimize the device for a wide range of input voltages and power consumption. This design provides instant overcurrent protection, followed by an intervention by the MCU for corrective action.

This reference design can be modified for use at input power lines 220 V/240 V for a variety of power loads. Digital control can be used to build a user interface that would allow users to change device parameters, gather statistics, add a communication interface, remotely monitor performance, or change parameters.

Related Documentation

Documents associated with this reference design are listed below. Each of the linked documents in this table can be obtained from the IXYS or Zilog websites by clicking the link associated with its Document Number.

Document Number	Document Description
IXRD1004	This High Power Two-Phase Digital PFC reference design document
IXRD1004-SC01	Source code for this High Power Two-Phase Digital PFC reference design
PS0294	F6482 Series General-Purpose Flash Microcontroller Product Specification
UM0263	F6482 Series Development Kit User Manual
UM0181	USB SmartCable User Manual
RM0064	F6482 Series API Programmer's Reference Manual

Appendix A. Schematic Diagrams

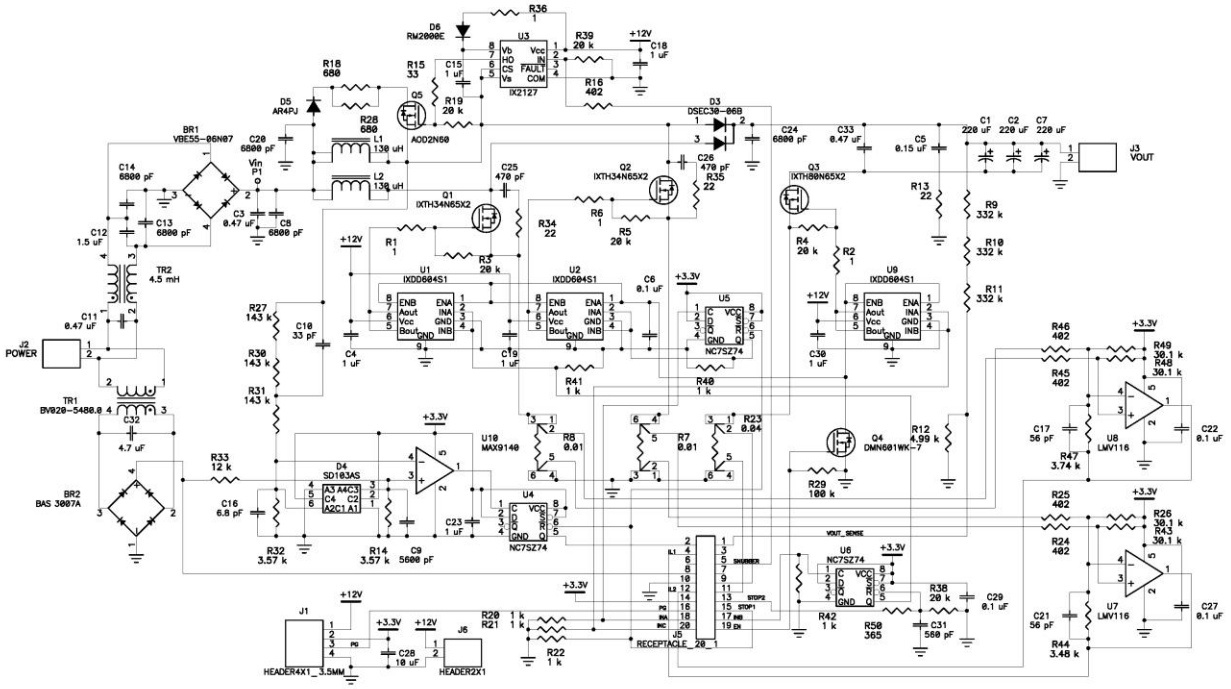


Figure 13. MCU-controlled PFC Main Board Schematic Diagram

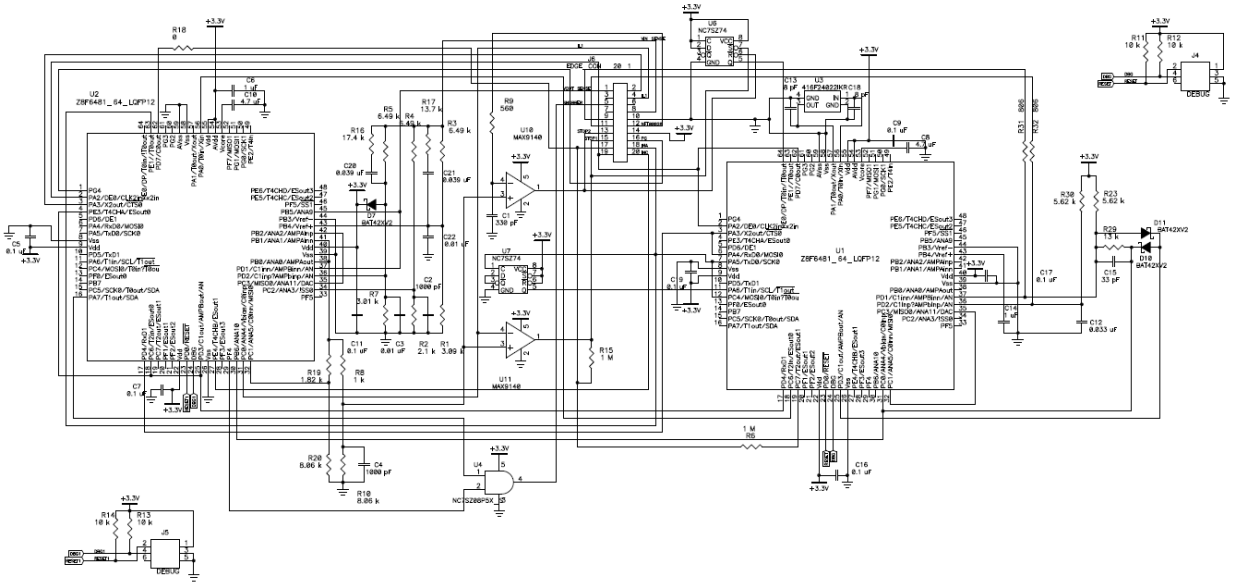


Figure 14. Digital Control Module Schematic Diagram

Appendix B. Board Components

Figures 15 and 16 display the location of the components on the High Power Two-Phase Digital Power Factor Correction Reference Design Board.

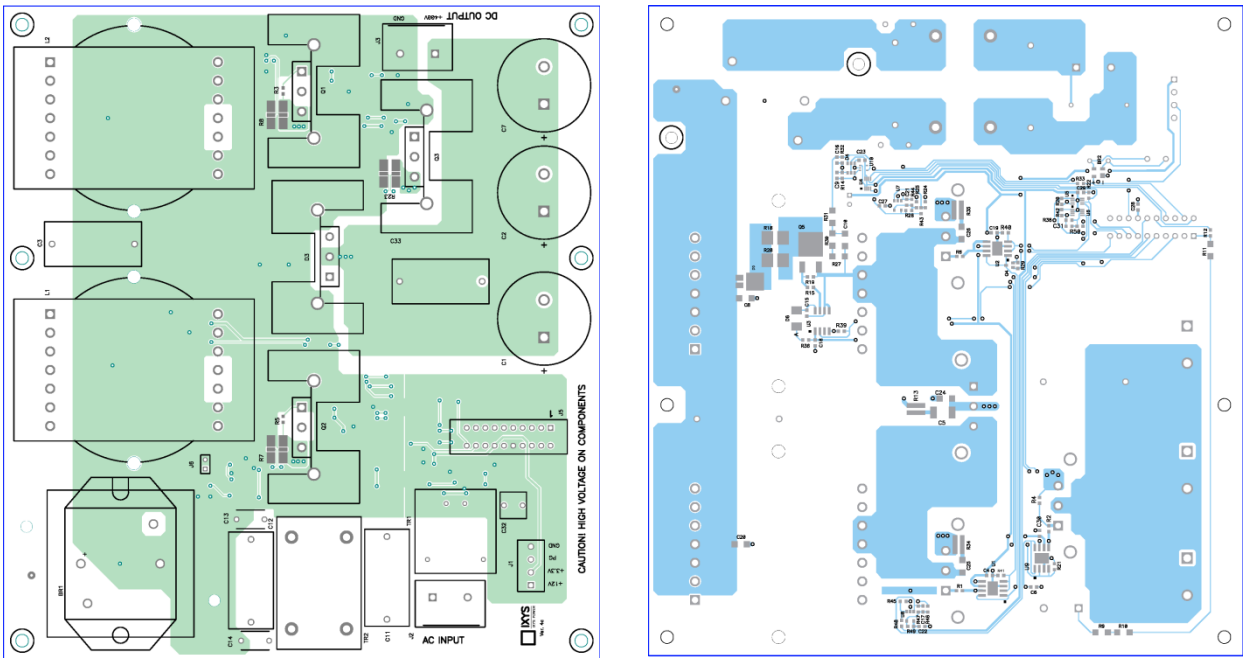


Figure 15. Main Board Layout (Top and Bottom Layers)

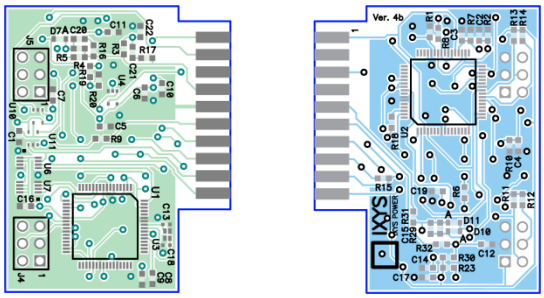


Figure 16. Layout of Digital Control Module (Top and Bottom Layers)

Appendix C. Bill of Materials

Table 1. Main Board Components

Count	Reference Designator	Value	Description	Manufacturer
1	BR1	VBE55-06N07	VBE55-06N07	IXYS Corp.
1	BR2	BAS 3007A	BAS 3007A-RPP E6327	Infineon Technologies
3	C1, C2, C7	220 uF	B43501A5227M	EPCOS (TDK)
1	C10	33 pF	CL31C330JHFNFNE	Samsung
1	C12	1.5 uF	ECW-FA2J155J	Panasonic Electronic Components
2	C13, C14	6800 pF	C967U682MYVDBA7317	Kemet
1	C16	6.8 pF	CL10C6R8DB8NNNC	Samsung
1	C17	56 pF	C1608C0G1H560J080AA	TDK Corporation
1	C21	56 pF	C1608C0G1H560J080AA	TDK Corporation
2	C25, C26	470 pF	CL31B471KHFNNNE	Samsung
1	C28	10 uF	CL10A106MA8NRNC	Samsung
3	C3, C11, C33	0.47 uF	B32653A6474K	EPCOS Inc
1	C31	560 pF	GRM1885C1H561JA01D	Murata
1	C32	4.7 uF	R82CC4470AA30J	Kemet
6	C4, C15, C18, C19, C23, C30	1 uF	TMK107B7105KA-T	Taiyo Yuden
1	C5	0.15 uF	C1812C154KBRACTU	Kemet
4	C6, C22, C27, C29	0.1 uF	CL10B104KA8NNNC	Samsung
3	C8, C20, C24	6800 pF	CC1206KKX7RZBB682	Yageo
1	C9	5600 pF	CL10B183JB8NNNC	Samsung
1	D3	DSEC30-06B	DSEC30-06B	IXYS Corp.
1	D4		SD103ASDM-7-F	Diodes Incorporated
1	D5	AR4PJ	AR4PJ	Vishay
1	D6	RM2000E	RM2000E	Micro Commercial Components
1	J1		39357-0004	Molex
2	J2, J3		1714971	Phoenix Contact
1	J5		5-5530843-0 TE	Connectivity
1	J6		BBL-102-GE	Samtec
2	L1, L2	130 uH	B65646	TDK
1	P1	Vin	1001-0-15-01-30-02-04-0	Mill-Max
2	Q1, Q2	IXTH34N65X2	IXTH34N65X2	IXYS Corp.
1	Q3	IXTH80N65X2	IXTH80N65X2	IXYS Corp.
1	Q4	DMN601WK-7	DMN601WK-7	Diodes Inc.
1	Q5	AOD2N60	AOD2N60	Alpha & Omega Semiconductor Inc.
4	R1, R2, R6, R36	1	RMCF0603FT1R00	Stackpole Electronics Inc
1	R12	4.99 k	RMCF0603FT4K99	Stackpole Electronics Inc
3	R13, R34, R35	22	LTR50UZPF22R0	Rohm Semiconductor
2	R14, R32	3.57 k	RMCF0603FT3K57	Stackpole Electronics Inc
1	R15	33	RMCF0603FT33R0	Stackpole Electronics Inc
5	R16, R24, R25, R45, R46	402	RMCF0603FT402R	Stackpole Electronics Inc
2	R18, R28	680	3522680RJT TE	Connectivity
6	R20, R21, R22, R40, R41, R42	1 k	RMCF0603FT1K00	Stackpole Electronics Inc
1	R23	0.04	LRF3WLF-01-R040F	TT Electronics/IRC
4	R26, R43, R48, R49	30.1 k	RMCF0603FT30K1	Stackpole Electronics Inc
3	R27, R30, R31	143 k	RMCF1206FT143K	Stackpole Electronics Inc
1	R29	100 k	RMCF0603FT100K	Stackpole Electronics Inc
6	R3, R4, R5, R19, R38, R39	20 k	RMCF0603FT20K0	Stackpole Electronics Inc
1	R33	12 k	RMCF0603FT12K0	Stackpole Electronics Inc
1	R44	3.48 k	RMCF0603FT3K48	Stackpole Electronics Inc
1	R47	3.74 k	RMCF0603FT3K74	Stackpole Electronics Inc
1	R50	365	RMCF0603FT365R	Stackpole Electronics Inc
2	R7, R8	0.01	LRF3WLF-01-R010F	TT Electronics/IRC
3	R9, R10, R11	332 k	RMCF1206FT332K	Stackpole Electronics Inc
1	TR1	BV020-5480.0	BV020-5480.0	Pulse
1	TR2	4.5 mH	7448051804	Wurth Electronics Inc
3	U1, U2, U9		IXDD604S1	IXYS Corp.
1	U10		MAX9140EXK-T	Maxim
1	U3		IX2127	IXYS Corp.
3	U4, U5, U6		NC7SZ74K8X	Fairchild Semic.
2	U7, U8		LMV116MF/NOPB	Texas Instruments

Table 2. Components of Digital Control Module

Count	Reference Designator	Value	Description	Manufacturer
1	C1	330 pF	GRM1885C1H331JA01D	Murata
1	C12	0.033 uF	C0603C333K4RACTU	Kemet
2	C13, C13	8 pF	GRM1555C1H8R0DA01D	Murata
1	C15	33 pF	CL10C330KB8NNNC	Samsung
1	C2	1000 pF	GRM188R71H102KA01D	Murata
1	C20, C21	0.039 uF	GRM188R71H393KA61D	Murata
2	C3, C22	0.01 uF	GRM188R71H103KA01D	Murata
1	C4	1000 pF	GRM188R71H102KA01D	Murata
7	C5, C7, C9, C11, C16, C17, C19	0.1 uF	CL10B104KA8NNNC	Samsung
2	C6, C14	1 uF	TMK107B7105KA-T	Taiyo Yuden
2	C8, C10	4.7 uF	GRM188R61E475KE11D	Murata
3	D7, D10, D11	BAT42XV2	BAT42XV2	Diodes Inc.
2	J4, J5	DEBUG	Header 67996-406HLF	FCI
1	J6		Board layout	
1	R1	3.09 k	RMCF0603FT3K09	Stackpole Electronics Inc
2	R10, R20	8.06 k	RMCF0603FT8K06	Stackpole Electronics Inc
4	R11, R12, R13, R14	10 k	RMCF0603FT10K0	Stackpole Electronics Inc
1	R16	17.4 k	RMCF0603FT17K8	Stackpole Electronics Inc
1	R17	13.7 k	RMCF0603FT13K7	Stackpole Electronics Inc
1	R18	0	HCJ0603ZT0R00	Stackpole Electronics Inc
1	R19	1.82 k	RMCF0603FT1K82	Stackpole Electronics Inc
1	R2	2.1 k	RMCF0603FT2K10	Stackpole Electronics Inc
2	R23, R30	5.62 k	RMCF0603FT5K62	Stackpole Electronics Inc
1	R29	13 k	RMCF0603FT13K0	Stackpole Electronics Inc
3	R3, R4, R5	6.49 k	RMCF0603FT6K49	Stackpole Electronics Inc
2	R31, R32	806	RMCF0603FT806R	Stackpole Electronics Inc
2	R6, R15	1 M	RMCF0603FT1M00	Stackpole Electronics Inc
1	R7	3.01 k	RMCF0603FT3K01	Stackpole Electronics Inc
1	R8	1 k	RMCF0603FT1K00	Stackpole Electronics Inc
1	R9	560	RMCF0603FT560R	Stackpole Electronics Inc
2	U1, U2		Z8F6481AR024XK	Zilog
2	U10, U11		MAX9140EXK-T	Maxim
1	U3	416F24022IKR	416F24022IKR	TS-Frequency Controls
1	U4		NC7SZ08P5X	Fairchild Semic.
2	U6, U7		NC7SZ74K8X	Fairchild Semic.

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