Digital Inrush Current Controller

Reference Design
IXRD100101-0515

Overview

The Digital Inrush Current Controller reference design combines IXYS' Digital Power Control technology with the capabilities of Zilog's 8-bit Z8F3281 microcontroller, a member of the Z8 Encore! XP F6482 Series of MCUs, to display a unique approach to control inrush current in AC–DC rectifiers or AC–DC converters. The objective of this reference design is twofold – to highlight the advantages of digital control that overcome many of the shortcomings of current technology, and to enhance interest in digital control of high power converters, potentially stimulating the development of next generation converters.

Digital control allows for distinctive solutions to control inrush current in a typical AC–DC rectifier with capacitive load by limiting the capacitor pre-charge current to a predetermined value at each half sine-wave cycle. This capacitor charge is spread over a number of cycles until the capacitor is charged to a peak value of AC voltage source. The capacitor is charged according to a time-dependent pulse train. Pulses are designed to provide substantially equal voltage increment applied to the capacitor to maintain peak charging current at approximately the same value at each cycle. The number of cycles depends on capacitor value and charge current. For a given capacitor value which is selected based on the desired amplitude of ripples, the charge current is a function of the number of pulses and their timing position with respect to the rectified sine wave. A comprehensive algorithm of creating a pulse train for Digital Inrush Control is described in Principles of Operation.

This reference design features programmable overload protection and the Power Good status signal. It is not sensitive to power outages, brownouts, and ambient temperature variations. This reference design has the ability to operate within an input voltage range of 80V–240V AC and load current up to 3A. The entire operating process and essential values are fully programmable. The controller may be programmed to 50 Hz, 60 Hz, or any other line input frequency operation.

This Digital Inrush Current Controller reference design is valuable for high power loads with tens of amperes of current in Normal Mode of operation. It allows users to optimize performance, maximize efficiency across the load range, and reduce the design time to market. IXYS power components handle the pre-charge of load capacitors at these values while limiting inrush current to controlled values.

Note: The source code file associated with this reference design, IXRD1001-SC01.zip, is available free for download from the IXYS Power and Zilog websites (www.ixyspower.com and www.zilog.com). This source code is tested with ZDS II – Z8 Encore! version 5.2.0. Subsequent releases of ZDS II may require you to modify the code supplied with this reference design.

Features

The Digital Inrush Current Controller reference design offers the following features:

- Input voltage range from 80V to 240V RMS
- Steady load current up to 3A
- Programmable overload protection

- Power Good status signal
- High endurance
- Not sensitive to power outage or brownout
- Not sensitive to ambient temperature variations
- Voltage ripples 15% at 2.5A load and output capacitance of 720µF
- Option to expand bulk capacitor value using external capacitors

Potential Applications

This reference design provides a basis for developing a variety of power management applications using IXYS power devices and an MCU, including the following applications:

- High Power AC– DC Rectifier
- High Power AC– DC PFC Converter

Principles of Operation

This section describes a basic example of operating the Digital Inrush Current Controller. This device comprises the following components:

- Typical power components of an AC–DC rectifier (diode bridge, inductor, and bulk capacitor)
- Switch Sw1 to commutate capacitor pre-charging current
- Switch Sw2 to connect/disconnect load
- Digital control module based on Zilog's Z8F3281 MCU, as shown in Figure 1.

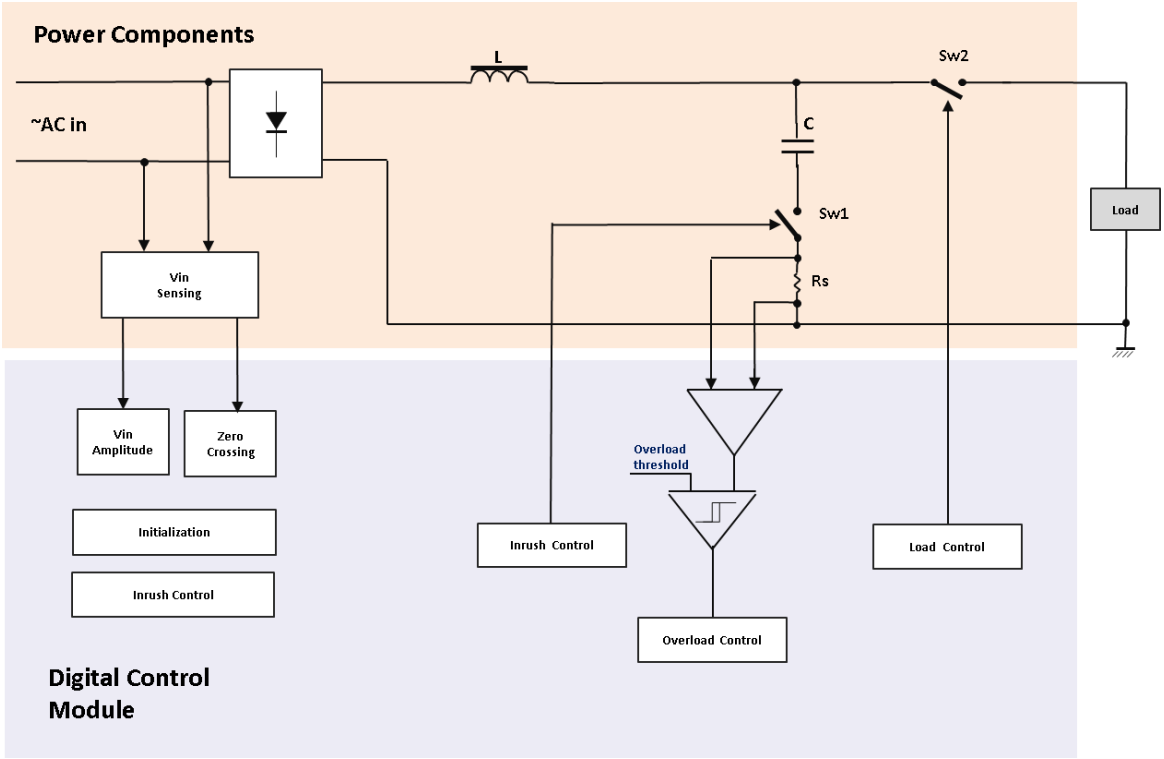

Figure 1. Functional Block Diagram of the Digital Inrush Controller

Theory of Digital Inrush Control

The Digital Inrush Control approach aims to provide charge to the bulk capacitor in substantially equal increments. This is accomplished by providing control pulses to Sw1, as shown in Figure 1, resulting in equal increments of a voltage applied to the bulk capacitor. It is possible to apply this charge on a cycle by cycle basis considering a cycle is half of sine wave of line voltage. For example, we can assign N cycles for the inrush control operation, and then split the normalized amplitude of the sine wave cycle to N segments with increment of 1/N, as shown in Figure 2.

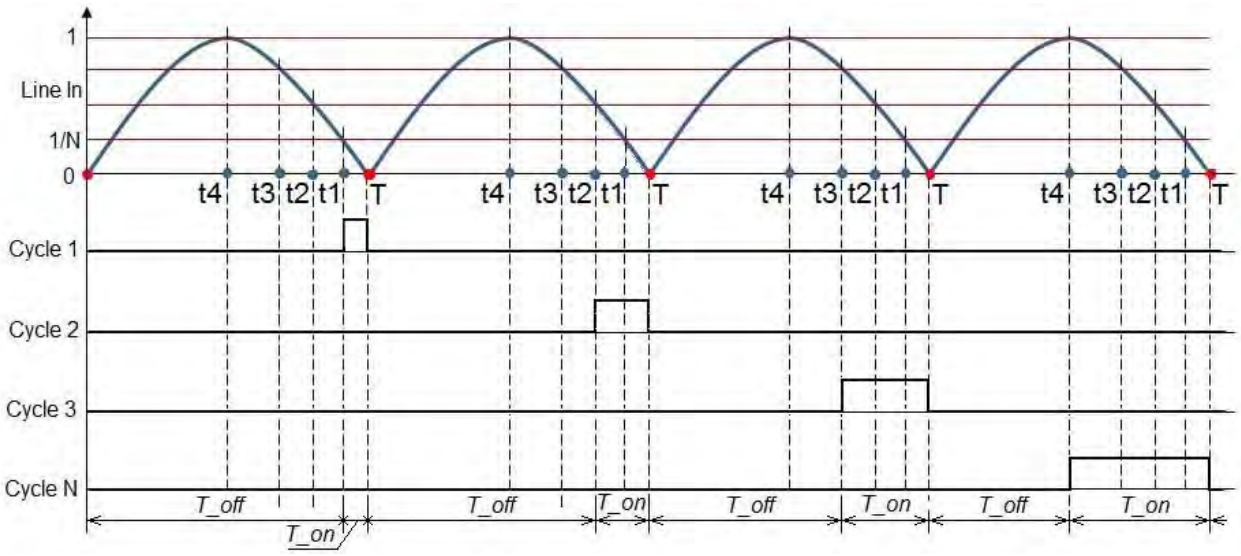

Figure 2. Digital Inrush Control Timing

During Cycle 1, Sw1 is in the ON state (conducting) from time t1 to T, as shown in Figure 2. The voltage across the capacitor increases to a voltage proportional to normalized value 1/N. During this period, the charging current rising follows the LC resonant behavior, as shown in Figure 3 (green line). The current rises until the capacitor voltage reaches the input voltage, excluding voltage dropouts. The current continues its resonant behavior as long as Sw1 is ON. No further oscillation occurs because the input voltage drops below the voltage on the capacitor, switching Sw1 to the OFF position (not conducting). The capacitor remains pre-charged to the voltage proportional to 1/N.

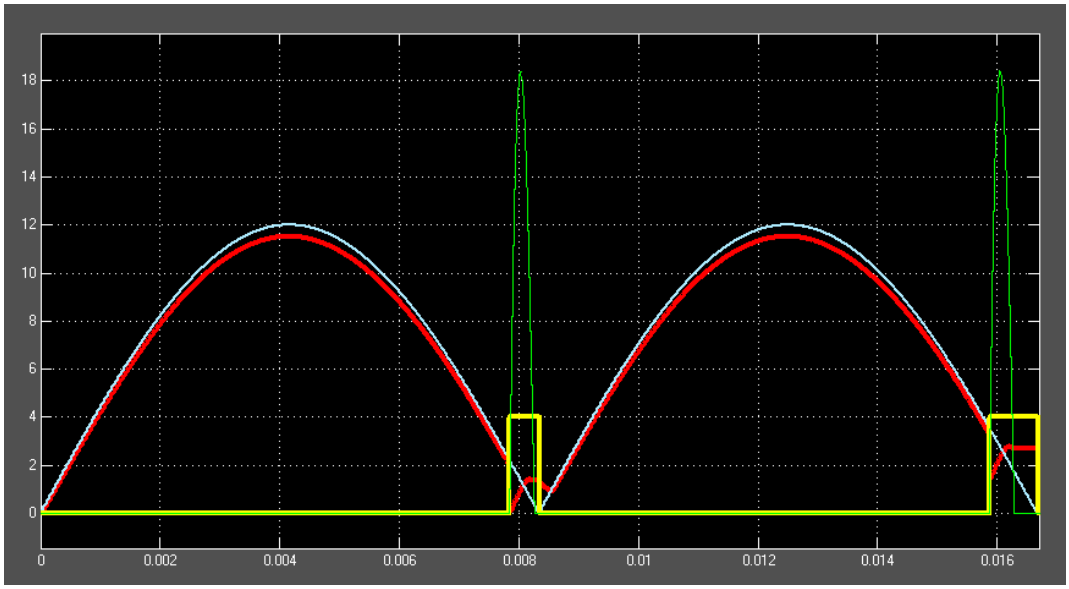

Figure 3. Capacitor C Pre-charging During First 2 Cycles

Legend (Not to scale):

Blue – power line voltage
Red – voltage on Capacitor C in respect to common Ground
Yellow – driver to Sw1
Green – Capacitor current

In Cycle 2, Capacitor C is pre-charged by another voltage increment 1/N, in a process similar to Cycle 1. Capacitor C is charged during N cycles to a voltage value proportional to the peak voltage value of the input power line.

Composing Timing for Digital Inrush Control

A simplified timing diagram for inrush control is shown in Figure 2 in which the voltage increment for each cycle is defined by the number of cycles (N). The capacitor's charging current is proportional to voltage increment, 1/N. Therefore, the number of cycles (N) is the variable used to control peak inrush current.

Another variable to control inrush current is LC time constant. The value of Capacitor C depends on the desired ripple value. After selecting the capacitor (C) value, the designer can decrease peak inrush current by increasing inductance (L). If there are physical limits to the L value, the number of cycles (N) should be used to set the required peak current.

Turn ON time for Switch Sw1 should be defined for each active cycle. Assuming that delay from zero crossing (point 0 in Figure 2Figure 2) to the beginning of turning Sw1 ON, t4, is ***T_off***, an active time to keep Sw1 ON is ***T_on***, and cycle duration is ***T.***

T_on for each occurrence ***i*** is defined as geometrical transform

$$T_{on(i)} = \frac{T}{\pi/2}\,\mathbf{asin}\,(i/N), \quad where\ i = 1 \ldots N \qquad (1)$$

The period (***T)*** is measured by MCU at initialization. Values ***T_on*** are determined by (1) and stored in memory. Values for ***T_off*** are derived by firmware according to following expression

$$T\_off = T - T\_on; \qquad (2)$$

Figure 4 illustrates how *T_on* values are defined for 16 cycles used in this reference design for 120V@60Hz.

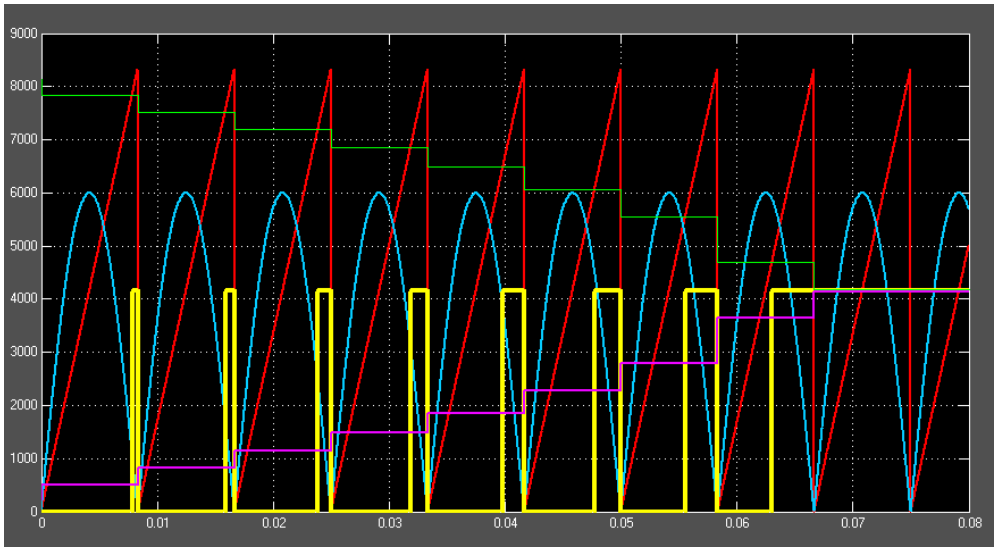

Figure 4. T_on Timing Generation

Legend (Not to scale):

Blue – rectified power line voltage
Red – full cycle period timing counter
Yellow – driver to Sw1
Green – time OFF to Sw1
Magenta – Time ON to Sw1
White – period T

In Figure 4, the blue line (rectified power line voltage) is shown for reference. The magenta line represents actual ***T_on*** time value in µs for each cycle, and the yellow line indicates ***T_on*** pulse positioned relatively to rectified power line voltage.

Figure 4 conceptually illustrates the algorithm functionality as executed by the Z8F3281 MCU. The timing counter (red line) corresponds to time at any given moment of discrete time base provided by the internal clock. The counter first counts until the ***T_off*** value, represented by the green line. When the counter reaches ***T_off*** value, it initiates the ***T_on*** pulse (yellow line) which continues until the counter reaches ***T_on*** value (magenta line).

Figure 5 displays the timing position and amplitude of the capacitor (C) current (green line) with respect to **T_on** pulses. A single current pulse is produced by the Inrush Controller during a cycle because the input voltage drops below the capacitor voltage and the input power line is isolated from the rest of the circuitry through the diode bridge after the capacitor charge is completed. The inductor discharges into the capacitor, and Sw1 switch is turned off (not conducting) at the end of the cycle.

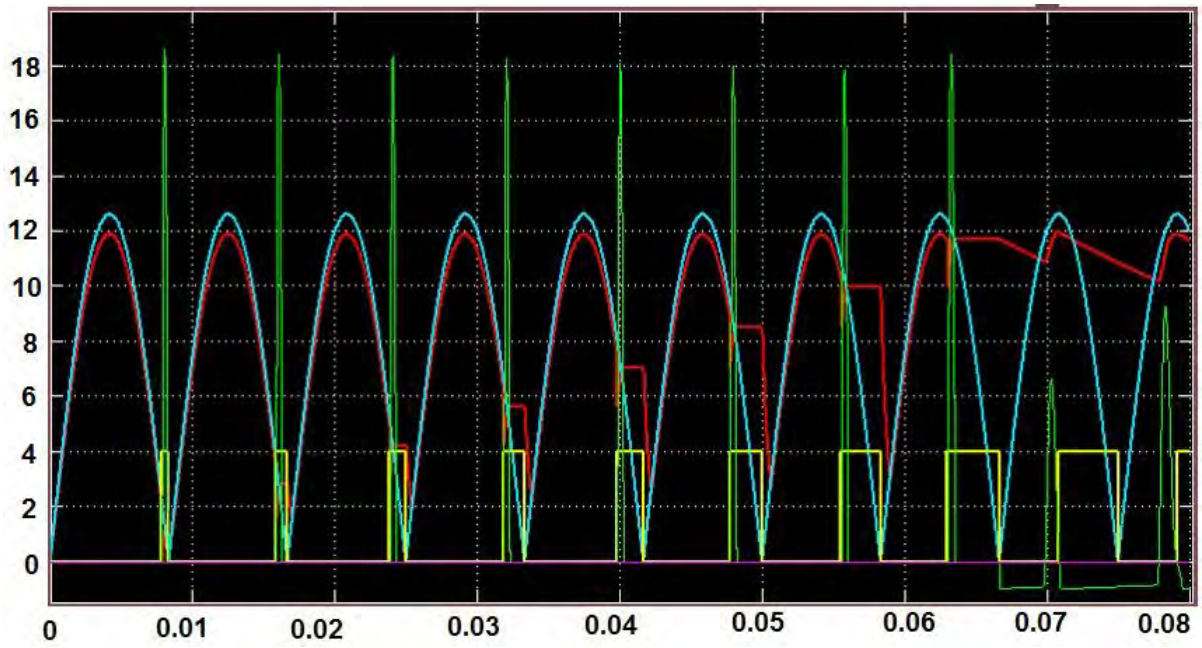

Figure 5. Capacitor C Pre-charging

Legend (Not to scale):

Blue – rectified power line voltage
Red – voltage on Capacitor C with respect to common Ground
Yellow – driver to Sw1
Green – Capacitor current

Service Functions

This reference design also includes a Load ON/OFF switch, Sw2, Overload Protection functionality, and Power Good status output to display the capability of IXYS power components. Sw2 activation is programmable, and is enabled after the capacitor C pre-charge is completed. In the current reference design, the Sw2 switch is activated at zero crossing on the next cycle after the capacitor is pre-charged. In the simulation shown in Figure 5, the Sw2 switch is activated at time stamp 0.066ms, when the capacitor current shows up as negative, because the current is sourced from the capacitor. Sw2 switch activation can be programmed to any time stamp point, depending on customer requirements.

The Overload Protection feature protects a device from damage in case of current overload. The overload threshold is programmable, and is set to 3.5A in this reference design.

If overload is detected by a comparator, the MCU disconnects the load by turning the Sw2 and Sw1 switches off, preventing extra current from going into the load

Overload protection can be programmed for the following two modes of operation:

- Immediately shut down the device and wait for user input
- Allow the device to restart after the short circuit is removed, and allow the device to restart for a predetermined number of short circuit occurrences if the short circuit occurrences repeat

In the second mode of operation, the delay between restarts and the number of restarts is programmable. In this reference design, the delay time is set to 1.5 seconds and the number of restarts is set to 4.

Power Good status activation is programmable. For this Digital Inrush Controller reference design, activation is delayed by 2 cycles after the capacitor's pre-charge is completed. The Power Good status is not set if overload is detected.

An example of the actual Power Good status signal can be in the following section.

Hardware Implementation

The IXYS Digital Inrush Current Controller, which consists of an MCU module and a main Power Board, is shown in Figure 6 (a) and (b). The detailed circuit schematics are included in Appendix A. Schematic Diagrams. The MCU module is implemented as an add-on device. The module consists of a connector for programming the microcontroller. The MCU module is powered by an auxiliary power supply of +3.3V for the MCU and 12V for the gate driver applied to the J4 connector on the main Power Board.

Note: The MCU should be programmed before powering the entire system.

The main Power Board is a two-layer surface-mount device that provides easy access to test points. Diode Bridge BR1 (refer to Appendix A. Schematic Diagrams) and MOSFETs Q1 and Q2 are mounted on small heat sinks. Power dissipated on these heat sinks is less than 5W at a 375W power output. This board may be powered from a 50 Hz or 60 Hz AC source.

Figure 6: (a) MCU Module and (b) Main Power Board with MCU Module

Setup and Test Results

This reference design was programmed and its performance verified on a test bench as shown in Figure 7. The AC line input is fed through 0.5 kW isolation transformers. The load is designed to consume 2.5A during normal operation. To test overload conditions, an additional load was used to provide 3.5A. An instantaneous connection of additional load was enough to trigger overload protection. Continuous overload results in multiple attempts to restart the device with immediate interruption.

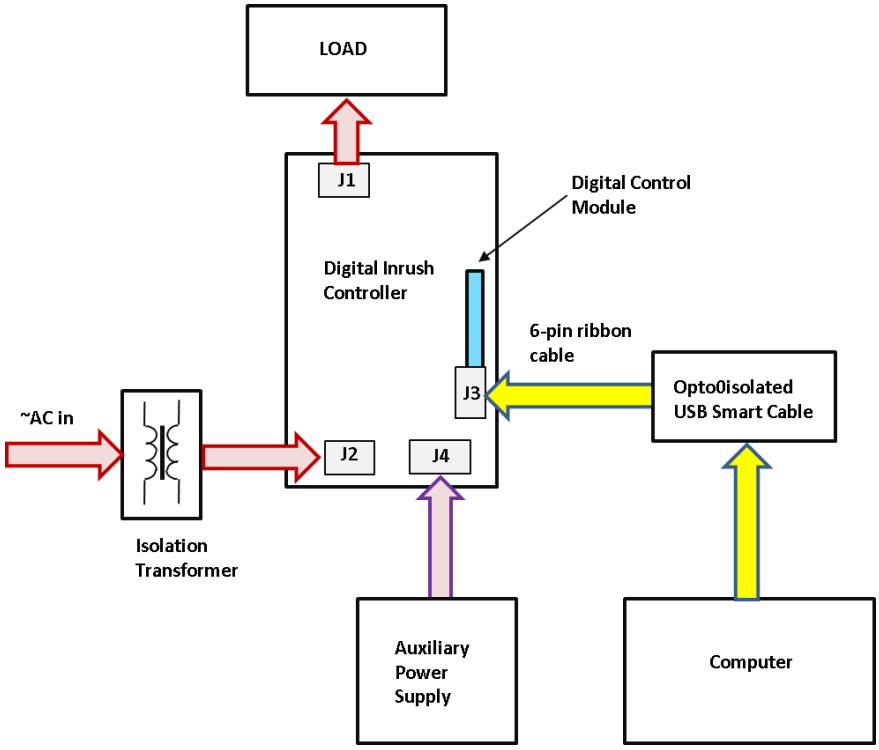

Figure 7. Digital Inrush Controller Setup

Auxiliary power supply should be turned ON only after the AC power is ON. Following a power-on reset and initialization, the MCU analyzes the power line, sets an appropriate timing, and begins pre-charging the bulk capacitor. Actual waveforms taken from a scope at normal operation are shown in Figure 8.

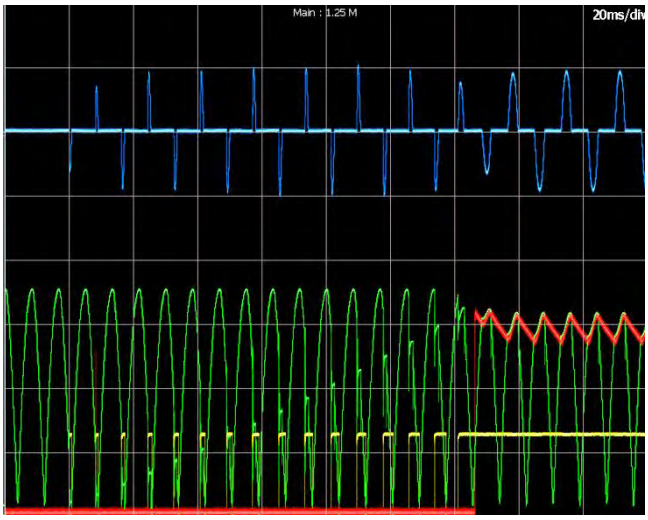

Figure 8. Scope Snapshot of Digital Inrush Current Control

Legend:

Blue – power line current (10A/div)
Red – Load voltage (50V/div)
Green – rectified input voltage (50V/div)
Yellow –Sw1 commutation signal

The Inrush current (top blue line) is limited to 10A. The yellow line shows the signal at the Sw1 gate. After the inrush procedure is completed, the gate is set to a high level to allow Sw1 to continue conducting. One cycle later, the load is connected and load voltage rises from zero to the level on the pre-charged capacitor. After the load is connected, a slight drop in the rectified voltage occurs due to the limited power capability of the isolation transformer.

To highlight the performance of increasing number of inrush control cycles at the same power conditions, inrush current measurements were taken with the controller reprogrammed to 16 cycles instead of the original 8 cycles. As a result, the inrush current dropped 2 times, as shown in Figure 9.

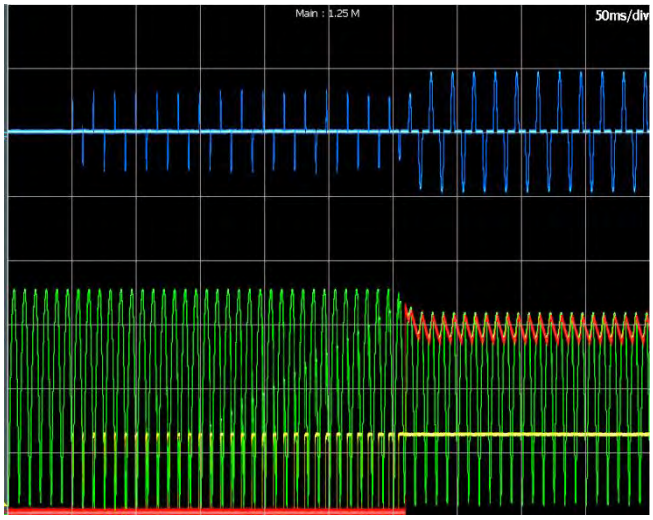

Figure 9. Scope Snapshot of Inrush Pulses with N Increased to 16

Legend:

Blue – power line current (10A/div)
Red – Load voltage (50V/div)
Green – rectified input voltage (50V/div)
Yellow – driver to Sw1

Performance During Overload Conditions

Normal operation starts with pre-charging the bulk capacitor. A scope snapshot of the startup is shown in Figure 10 with a horizontal scale of 1s. The yellow line indicates that the gate driver state is wide because of the low graphic resolution for 12 cycles of pre-charge. After the inrush control sequence is completed, the load is connected, which is indicated by the red line going upwards. The Power Good status (blue line) goes up as well.

Continuous overload is applied at 2.3 seconds. The load is disconnected and the Power Good status goes low. An attempt to restart the device initiated in 1.5 second intervals. The inrush sequence is performed again, and the load is connected. However, the overload is sensed right away, the load is disconnected, and the Power Good status continues to stay low. Another attempt to restart is repeated after 1.5 seconds and the load stays connected for about 1 second while there is no overload condition.

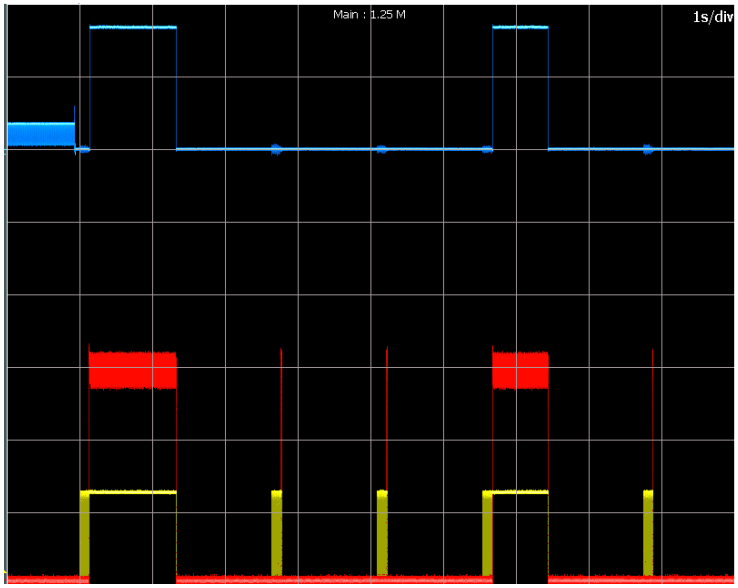

Figure 10. Scope Snapshot to Show Performance During Overload and Restart

Legend:

Blue – Power Good status
Red – Load voltage (50V/div)
Yellow – driver to Sw1

Efficiency of Digital Inrush Controller

The efficiency of the Digital Inrush Controller is estimated, starting after the diode rectifier to the load. At a load power of 375 W, the power loss is 2.1 W, which equates to an efficiency of 99.47%.

Device Configuration and Control Setup

This reference design can be configured for different parameters such as input voltage and frequency range, overload threshold, overload recovery time, number of overload events before shutdown, time position for Power Good status, and time position to turn ON the Load.

The firmware that controls the operations of this Digital Inrush Controller reference design was developed using Zilog's Development Studio II (ZDS II – Z8 Encore! version 5.2.0). The following hardware components were used during the development of this reference design:

- USB SmartCable – provides communication with ZDS II – Z8 Encore! version 5.2.0, debugging and downloading code into the F3281 MCU
- Connector J5 2x3, straight male header

Note: When connecting either device to the Reference Design Board, always ensure that pin 1 of the programming cable and pin 1of the connector on the digital control module are lined up.

Software Implementation

The source code for this application, IXRD1001-SC01.zip is available free for download from the Zilog website. This section describes the programs included in the source code.

Main.c file

To limit the inrush current upon system power up, this program utilizes Look-up Tables (LUT) containing values based on characterization from a simulation model to charge the buffer capacitors which are connected to the load after the capacitor charging process has completed. If a fatal overcurrent event occurs, the comparator will shut down the system and restart the inrush current control for a user defined amount of time. After the allowed restart attempts, the system remains OFF.

The program implements a comparator and three timers to generate the current limiting pulse trains, which consist of on and off times that are based on these LUT values. Effectively, this constitutes a pulse width modulated signal. Each of these on/off pulses is applied to the input switch PD6 of the inrush current limit circuit, therefore limiting the current of the circuit. Three look-up tables contain values that are characterized for the capacitors to be charged at 220V/60Hz, 120V/60Hz, and 220V/50Hz and can be selected in the main.h header files.

The main purpose of the comparators and timers is to place the current limiting pulse train so that the pulses are aligned to a certain position of the rectified power input sine wave. This pulse train alignment, or synchronization, is achieved by the use of a comparator and a timer which measures the zero crossing events of the input power sine wave. The pulse train is then synchronized with the zero crossing events and is located toward the falling slope of the rectified sine wave.

Upon power up, the first user-definable sine wave cycles are ignored to let the system stabilize before measuring the sine wave periods and zero-crossings. The next two sine wave periods are measured using the comparator's falling edge and multichannel timer 1 and stored as variable T_period. However, this variable is not implemented; instead, a macro containing the ideal value for either 50Hz or 60Hz is used. The macro can be changed so that the measured values can be implemented, if required. The next four input power sine cycles are used to determine the zero crossing events by measuring the time period from the sine's falling slope to the sine's rising slope at a 0.7V comparator interrupt threshold. Multichannel timer1 is used to measure the lapsed time between the two comparator interrupt events. When the measurement is completed, the zero crossing is determined to be half of the measured time.

After the above information is collected, general timer1 and timer2 are configured in triggered one-shot mode. Timer-2 is loaded with the power input sine period value minus the *inrushCurrentOffTime* value from the LUT, minus the measured zero-cross time and a zero-cross compensation value. The result of this operation becomes the on-time. The zero-cross compensation value is used to fine-tune the pulse train alignment with the power input sine wave. Timer2 is triggered upon the comparator's rising edge interrupt. Upon expiring of timer2, the gate of the input switch MOSFET is enabled and timer1 is triggered. Upon expiring of timer1, the input switch MOSFET is disabled again.

This process repeats until all the values from the LUT have been used. Up to this point, only the capacitors have been charged, not the actual load. Upon finishing of the inrush current procedure for the

capacitors and one input power sine cycle later, the actual load is activated. After the load is connected, a *Power Good Signal* is generated at a user-defined delay.

Note: To enable further customization, the Analog-to-Digital converter (ADC) peripherals have been configured and functions have been written for the implementation of load current and voltage readings. This has not been implemented.

Main.h file

This file contains the function prototypes, structures, and macro definitions. The inrush current limit can be selected for 120V/60Hz, 240V/60Hz, and 220/50Hz systems.

Power is selected by commenting and un-commenting macros in the following manner:

- If the ONEHUNDRED_TWENTY macro is uncommented, then 120V/60 is selected.
- If the ONEHUNDRED_TWENTY and TWOHUNDRED_TWENTY_VOLT_50HZ macros are commented out, then 240V/60 Hz is selected, otherwise 220V/60 Hz is selected.

Depending on the load capacitor values, the amount and durations of the LUT values may have to change. In this situation, the user is provided with a formula to calculate the new LUT values which can then be loaded into the look-up tables. However, the amount of these values can be more or less and the INDEX macro must be adjusted to the amount of LUT values.

The RC_DLY_OFFSET_50HZ macro is used to fine-tune the pulse train to the left on the x-axis of the input power sine wave to achieve a more linear charging characteristic.

Initialization.c file

This file contains the peripheral setup for:

- System clock
- Operational amplifier
- ADC
- Multichannel timers
- General purpose timers
- Comparators

Software setup procedure

The code for this reference design was created on ZDS II – Z8 Encore! version 5.2.0, which can be downloaded from the Zilog website. To make changes to the code, perform the following steps to setup the software:

1. Install ZDS II – Z8 Encore! version 5.2.0 or newer software to your PC.
2. Connect the Opto-isolated USB Smart Cable (debugger) to the PC. Connect the included ribbon cable to the J3 connector on the main Power Board.
3. Download the source code file for the Digital Inrush Current Controller reference design (IXRD1001-SC01) from the Zilog or IXYS website and open this project file in the ZDSII IDE.

4. To make changes to the code operation such as voltage outlet (220V/50Hz, 120V/60Hz, or 240/60Hz), refer to the instructions in the main.h header files.
5. Compile the program and download it to the Z8F3281 MCU.

Equipment Used

The following equipment was used to build and test this reference design:

- Laboratory DC Power Supply – GPS-4303
- Scope – Yokogawa DL9140
- Multimeter – FLUKE-179
- Isolation Transformer – 500W

See Appendix C. Bill of Materials for a list of materials used to build this reference design.

Kit Contents

This Digital Inrush Controller Reference Design Kit contains the following items:

- Digital Inrush Controller Reference Design Block
- Opto-isolated USB SmartCable
- Digital Inrush Controller Reference Design Kit Insert (FL0177)

Ordering Information

The products associated with this Digital Inrush Controller Reference Design can be ordered from the IXYS Store or the Zilog Store using the part number listed below.

Part Number	Description	Store Product ID
IXRD1001	Digital Inrush Controller Reference Design Kit	RD10040

Results

Testing of this design confirmed that the inrush current is limited to a predefined value and the performance of the limiter is quite close to the simulation results. The measured efficiency of the inrush control path is 99.5%. This device is capable of working with a wide range of input voltages from 80V to 240V. The tested power line frequency range was 50 Hz–60 Hz. A dedicated control pulse train was developed for each power line frequency. To work with higher power line voltage, a longer control pulse train needs to be programmed. For instance, raising line voltage from 110 V to 220 V required twice as much pre-charging time to have the same peak inrush current.

Overload protection is based on continuous monitoring of dynamic current from bulk capacitor. In case of overload, the current drawn from the capacitor instantly increases and triples the comparator, thereby initiating system overload mode. Overload current threshold, number of overload instances, and period between overload events are programmable. The option to turn the load ON/OFF aids the overload mode of operation by disconnecting the load. Power Good status is not available in overload conditions. The Digital Overload Protection device is not sensitive to power interruptions, brownouts, and temperature variations.

The primary features of the system include:

- Inrush current is limited to predefined value
- High efficiency in the range of 99.5%
- Wide input voltage range – 80V to 240V
- Wide input frequency range – 50/60/400Hz
- Option to turn Load ON/OFF
- Programmable Overload protection – number of overload instances, period between overload event, continuous overload or instant
- Power Good status, which is not available during overload conditions
- Not sensitive to power interruptions or brownouts
- Not sensitive to temperature variations
- High endurance

Summary

This Digital Inrush Controller is the first digital power device based on Zilog's Z8 Encore! XP F6482 Series of MCUs, which offers flexibility in implementing a unique control algorithm that aids in developing efficient power systems. This reference design achieves a high level of efficiency, improved stability, and reliable performance across a wide range of loads. Because of an innovative current measurement algorithm, this Controller allows common input and load grounds. Users can optimize the device for a wide range of input voltages and frequencies. This design provides instant over-current protection, followed by an intervention by the MCU for corrective actions.

The Digital Inrush Controller can be used as part of an AC-DC rectifier or can be expanded to higher-level devices such as a PFC converter.

Digital control can be used to build a user interface that would allow users to change device parameters, gather statistics, add a communication interface, remotely monitor performance, or change parameters.

Related Documentation

Documents associated with this reference design are listed below. Each of the linked documents in this table can be obtained from the IXYS or Zilog websites by clicking the link associated with its Document Number.

Document Number	Document Description
IXRD1001	This Digital Inrush Controller Reference Design document
IXRD1001-SC01	Source code for this Digital Inrush Controller Reference Design
PS0294	F6482 Series General-Purpose Flash Microcontroller Product Specification
UM0263	F6482 Series Development Kit User Manual
RM0064	F6482 Series API Programmer's Reference Manual

Appendix A. Schematic Diagrams

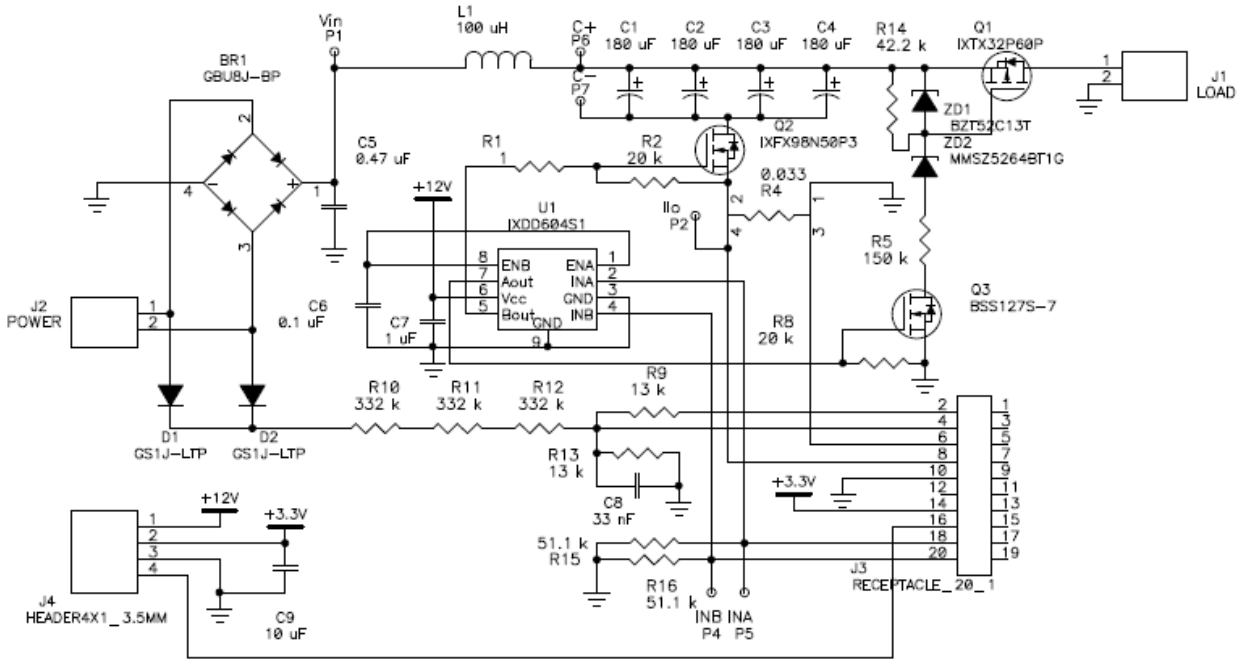

Figure 11. Schematic Diagram of Digital Inrush Controller Main Board

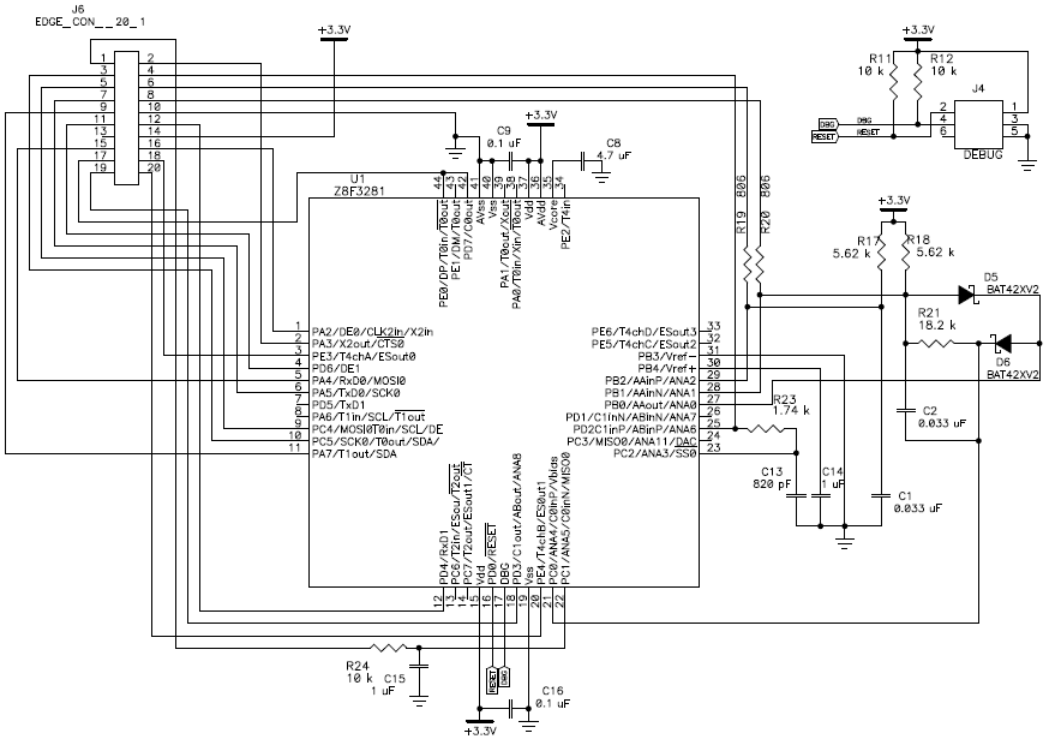

Figure 12. Schematic Diagram of Digital Control Module

Appendix B. Board Components

Figure 13 displays the location of the components on the Digital Inrush Controller Reference Design Board. Figure 14. Layout of Digital Control Module (Top and Bottom Layers)Figure 14 indicates the location of power components and the MCU on the Board.

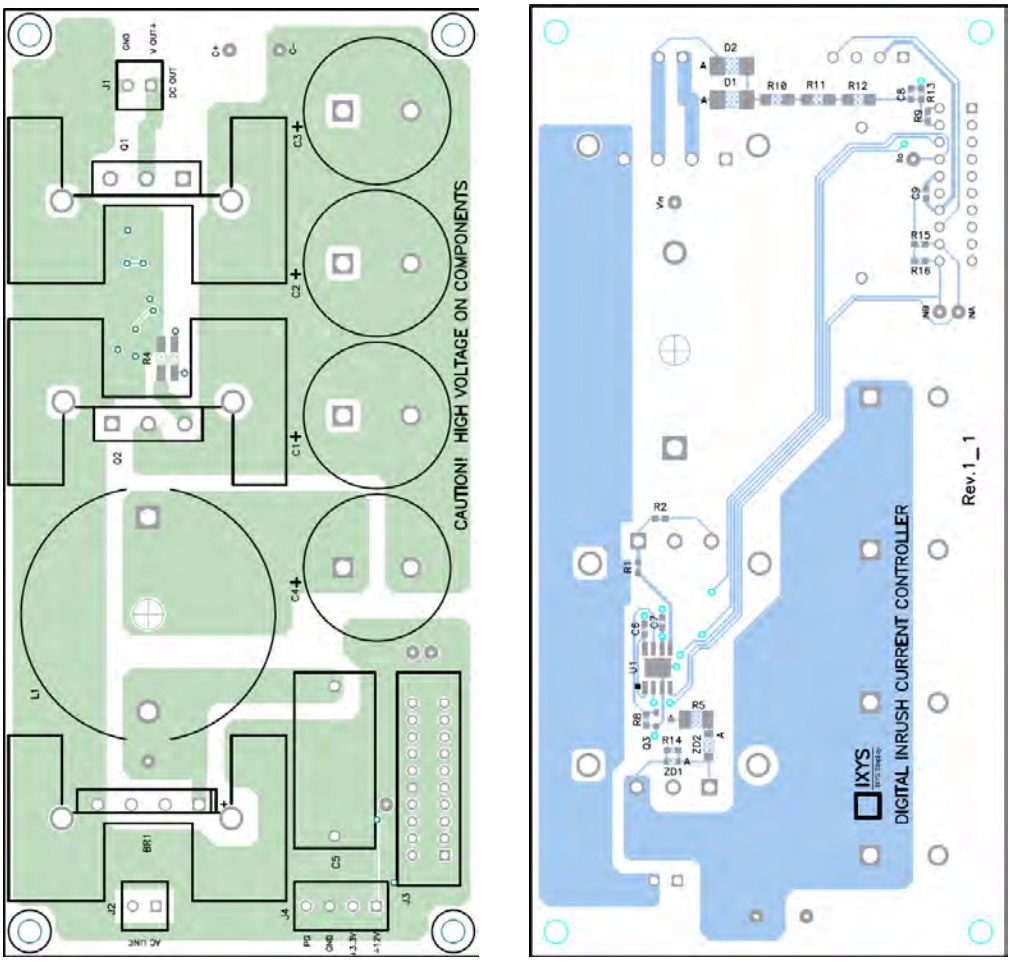

Figure 13: Main Board Layout (Top and Bottom Layers)

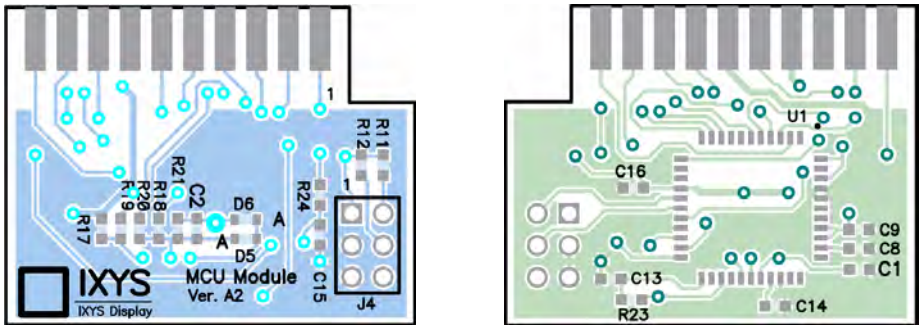

Figure 14. Layout of Digital Control Module (Top and Bottom Layers)

Appendix C. Bill of Materials

Table 1 and Table 2 list the components used to build this reference design.

Table 1. Main Board Components

Count	Reference Designator	Value	Description	Manufacturer
1	BR1	GBU8J-BP	GBU8J-BP	Micro Commercial Co with HS
3	BR1, Q1, Q2	6398BG	Heat Sink	Aavid Thermalloy
4	C1, C2, C3, C4	180 µF	ESMQ451VSN181MP40S	United Chemi-Con
1	C5	0.47 µF	B32653A6474K	EPCOS Inc
1	C6	0.1 µF	C0603C104K3RACTU	Kemet
1	C7	1 µF	TMK107B7105KA-T	Taiyo Yuden
1	C8	33 nF	C0603C333K3RACTU	Kemet
1	C9	10 µF	CL10A106MA8NRNC	Samsung
2	D1, D2	GS1J-LTP	GS1J-LTP	Micro Commercial Co
2	J1, J2		Terminal Block 39357-0002	Molex
1	J3		5-5530843-0	TE Connectivity
1	J4		Terminal Block 39357-0004	Molex
1	L1	100 µH	1140-101K-RC	Bourns Inc.
7	P1 –P7		1001-0-15-01-30-02-04-0	Mill-Max
1	Q1	IXTX32P60P	IXTX32P60P	IXYS Corp. with HS
1	Q2	IXFX98N50P3	IXFX98N50P3	IXYS Corp. with HS
1	Q3	BSS127S-7	BSS127S-7	Diodes Incorporated
1	R1	1	CRCW06031R00FSTA	Vishay
3	R10, R11, R12	332 k	RMCF1206FT332K	Stackpole Electronics Inc
1	R14	42.2 k	RMCF0603FT42K2	Stackpole Electronics Inc
2	R15, R16	51.1 k	RMCF0603FT51K1	Stackpole Electronics Inc
2	R2, R8	20 k	RMCF0603FT20K0	Stackpole Electronics Inc
1	R4	0.033	LVK24R033FER	Ohmite
1	R5	150 k	ERJ-14NF1503U	Panasonic Electronic Comp.
2	R9, R13	13 k	RMCF0603FT13K0	Stackpole Electronics Inc
1	U1		IXDD604S1	IXYS Corp.
1	ZD1	BZT52C13T	BZT52C13T-7	Diodes Inc.
1	ZD2	MMSZ5264BT1G	MMSZ5264BT1G	ON Semiconductor

Table 2. Components of Digital Control Module

Count	Reference Designator	Value	Description	Manufacturer
2	C1, C2	0.033 µF	C0603C333K4RACTU	Kemet
2	C9, C16	0.1 µF	CL10B105KA8NNNC	Samsung
2	C14, C15	1 µF	CL10B106KA8NNNC	Samsung
1	C8	4.7 µF	CL10A475KA8NQNC	Samsung
1	C13	820 pF	TMK107B7821KA-T	Taiyo Yuden
2	D5, D6	BAT42XV2	BAT42XV2	Diodes Inc.
1	J6		Board Layout	
1	J4		Header 67996-406HLF	FCI
1	R23	1.74 k	RMCF0603FT1K74	Stackpole Electronics Inc
2	R17, R18	5.62 k	RMCF0603FT5K62	Stackpole Electronics Inc
3	R11, R12, R24	10 k	RMCF0603FT10K0	Stackpole Electronics Inc
1	R21	18.2 k	RMCF0603FT18K2	Stackpole Electronics Inc
2	R19, R20	806	RMCF0603FT806R	Stackpole Electronics Inc
1	U1	Z8F3281	Z8F3281AN024XK	Zilog

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