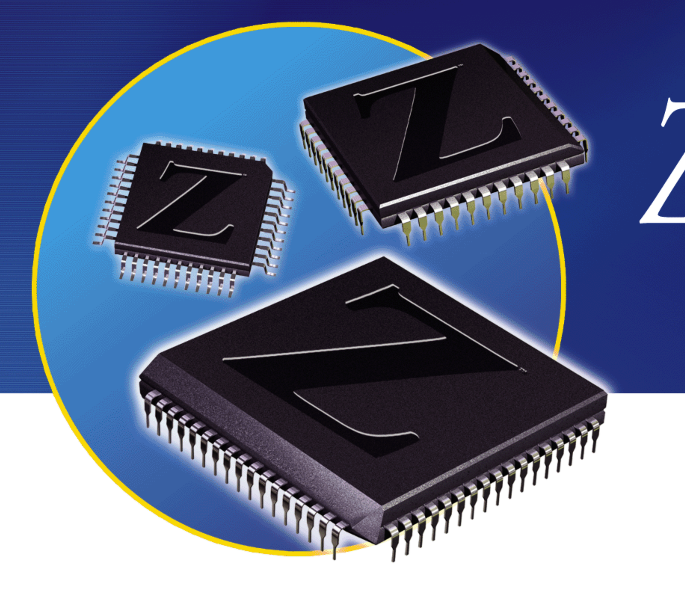


Z8 Encore! MC™ Z8FMC16100 Series Motor Control MCU EASY REFERENCE CHART

ZiLOG

Program Memory Map

Flash Memory Configurations

Part Number	Flash Size	Number of Pages	Program Memory Addresses	Sector Size	Number of Sectors	Pages per Sector
Z8FMC16	16K (16,384)	32	0000h–3FFFh	2K (2048)	8	4
Z8FMC08	8K (8,192)	16	0000h-1FFFh	1K (1024)	8	2
Z8FMC04	4K (4,096)	8	0000h-0FFFh	512	8	1

Program Memory Address (Hex)	Function
0000-0001	Option Bits
0002-0003	Reset Vector
0004-0007	System Exception Vectors
0008-003F	Interrupt Vectors
0040-3FFF	Program Memory

Comparator and Op Amp Registers

Comparator and Op Amp Control Register
(CMPOPC = F90h)

7	OPEN	0 = Operational amplifier is disabled 1 = Operational amplifier is enabled
6:5		Reserved
4	CPSEL	0 = Comparator input is PA1 1 = Comparator input is PB4
3	CMPIRQ	0 = Interrupt request on comparator rising edge 1 = Interrupt request on comparator falling edge
2	CMPIV	0 = PWM fault is active when CP+ > CP- 1 = PWM fault is active when CP- >CP+
1	CMPOUT	0 = Comparator output value is a logical 0 1 = Comparator output value is a logical 1
0	CMPEN	0 = Comparator is disabled 1 = Comparator is enabled

A/D Converter Registers

ADC Control Register 0
(ADCCTL0 = F70h)

7	START	0 = Writing to 0 has no effect. Reading a 0 indicates the ADC is available to begin a conversion 1 = Writing to 1 starts a conversion. Reading a 1 indicates a conversion is currently in progress.
6		Reserved
5	REFEN	0 = Internal reference voltage is disabled allowing an external reference voltage to be used by the ADC 1 = Internal reference voltage for the ADC is enabled. The internal reference voltage can be measured on the VREF pin
4	ADCEN	0 = ADC is disabled for low power operation 1 = ADC is enabled for normal use
3		Reserved
2:0	ANAIN	000 ANA0 input is selected for analog to digital conversion 001 ANA1 input is selected for analog to digital conversion 010 ANA2 input is selected for analog to digital conversion 011 ANA3 input is selected for analog to digital conversion 100 ANA4 input is selected for analog to digital conversion 101 ANA5 input is selected for analog to digital conversion 110 ANA6 input is selected for analog to digital conversion 111 ANA7 input is selected for analog to digital conversion

ADC Data High Byte Register
ADCD_H = F72h

7:0	ADCD_H	00h–FFh The high byte of the last conversion output is held in the data registers until the next ADC conversion has completed

ADC Data Low Bits Register
ADCD_L = F73h

7:6	ADCDL	00–11b These bits are the 2 least significant bits of the 10-bit ADC output. The low bits are latched into this register whenever the ADC Data High Byte Register is read.
5:0		Reserved

ADC Clock Prescale Register
ADCCP = F76h

7:4		Reserved
3	DIV16	0 = Clock is not divided 1 = System Clock is divided by 16 for ADC Clock
2	DIV8	0 = Clock is not divided 1 = System Clock is divided by 8 for ADC Clock
1	DIV4	0 = Clock is not divided 1 = System Clock is divided by 4 for ADC Clock
0	DIV2	0 = Clock is not divided 1 = System Clock is divided by 2 for ADC Clock

Sample and Settling Time
ADCSST = F74h

7:4		Reserved
3:0	SST	Sample settling time in number of system clock periods to meet 0.5 µs minimum.

Sample Hold Time
ADCST = F75h

7:5		Reserved
4:0	ST	Sample Hold time in number of system clock periods to meet 1 µs minimum.

GPIO Registers

Port A through C GPIO Address Registers (Use subregister address)

PAADDR = FD0h

7:0	PAADDR	Port A GPIO Address Register

PBADDR = FD4h

7:0	PBADDR	Port B GPIO Address Register

PCADDR = FD8h

7:0	PCADDR	Port C GPIO Address Register

Port A through C Control Register (Value in this register is loaded in subregister identified by GPIO address register)

PACTL = FD1h

7:0	PACTL	Port A Control Register

PBCTL = FD5h

7:0	PBCTL	Port B Control Register

PCCTL = FD9h

7:0	PCCTL	Port C Control Register

Port A through C Input Data Register

PACTL = FD2h

7:0	PINA	Port A Input Data Register

PBCTL = FD6h

7:0	PINB	Port B Input Data Register

PCCTL = FDAh

7:0	PINC	Port C Input Data Register

Port A through C Output Data Register

PACTL = FD3h

7:0	POUTA	Port A Output Data Register

PBCTL = FD7h

7:0	POUTB	Port B Output Data Register

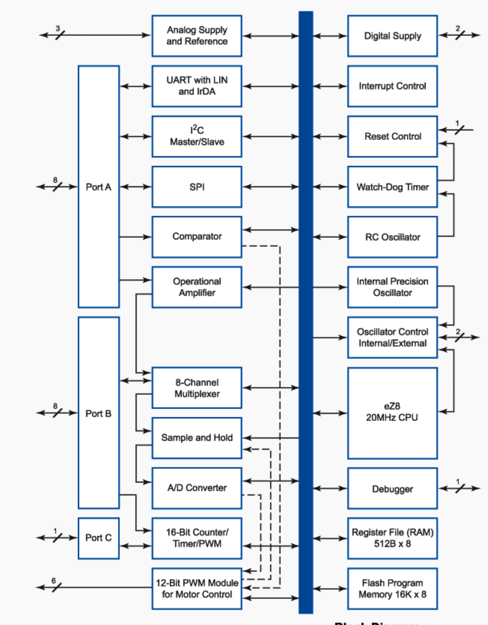
PCCTL = FDBh

7:0	POUTC	Port C Output Data Register

Subregisters by Port Address (used in GPIO Address register)

01h	PxDD	Data direction. 0=output, 1=input
02h	PxAF0	Alternate Function 0. 0=not selected, 1=selected
03h	PxOC	Output Control. 0=drain enabled, 1=open-drain
04h	PxHDE	High Drive Enable. 0=standard drive, 1=high drive
05h	PxSMRE	Stop-Mode Recovery Source. 0=disabled, 1=enabled
06h	PxPUE	Pull-up enable. 0=disabled, 1=enabled
07h	PxAF1	Alternate Function 1—Ports A and B only. 0=not selected, 1=selected
08h	PxIRQES	Interrupt Edge Select—Port A and Port C only. 0=falling edge, 1=rising edge
09h	IRQPSEL	Interrupt Port Select—Port A only. 0=PA0 through PA3, 1=PA4 through PA7

Functional Block Diagram



Block Diagram

Pulse-Width Modulator Registers (PWM)

PWM High Byte Register
PWMH = F2Ch

7:4		Reserved
3:0	PWMH	Contains current count for PWM[11:8]

PWM Low Byte Register
PWML = F2Dh

7:0	PWML	Contains current count for PWM[7:0]

PWM Reload High Byte Register
PWMRH = F2Eh

7:4		Reserved
3:0	PWMRH	The high byte of the reload value for the PWM

PWM Reload Low Byte Register
PWMRL = F2Fh

7:0	PWMRL	The low byte of the reload value for the PWM

PWM 0-2 H/L Duty Cycle High Byte Register
PWMHxDH, PWMLxDH

7	SIGN	0 = Duty Cycle is a positive two's complement number 1 = Duty Cycle is a negative two's complement number. Output is forced to the OFF state.
6:0	DUTYH	The two bytes {DUTYH[7:0], DUTYL[7:0]} form a 14-bit signed value (bits 5 and 6 of the high byte are always 0). The value is compared to the current 12-bit PWM count.

PWM 0-2 H/L Duty Cycle Low Byte Register
PWMHxDL, PWMLxDL

7:0	DUTYL	The two bytes {DUTYH[7:0], DUTYL[7:0]} form a 14-bit signed value. The value is compared to the current 12-bit PWM count.

PWM Control 0 Register
PWMCTL0 = F20h

7	PWMOFF	0 = Disable modulator control of PWM pins. Outputs are in predefined off-state. This is not dependent on the reload event. 1 = Reenable modulator control of PWM pins at next PWM reload event.
6	OUTCTL	0 = PWM outputs are controlled by the Pulse-Width Modulator 1 = PWM outputs selectively disabled (set to off-state) according to values in the OUTx bits of the PWMOUT register
5	ALIGN	0 = PWM outputs are edge aligned 1 = PWM outputs are center aligned
4		Reserved
3	ADCTRIG	0 = No ADC trigger pulses 1 = ADC trigger enabled
2		Reserved
1	READY	0 = PWM values (prescale, period, and duty cycle) are not ready. Do not use values in holding registers at next PWM reload event. 1 = PWM values (prescale, period, and duty cycle) are ready. Transfer all values from temporary holding registers to working registers at next PWM reload event.
0	PWMEN	0 = Pulse-width modulator is disabled and enabled PWM output pins are forced to default off-state. PWM master counter is stopped. 1 = Pulse-width modulator is enabled and PWM output pins are enabled as outputs.

PWM Control 1 Register
PWMCTL1 = F21h

7:6	FLFREQ[1:0]	00 = PWM reload event occurs at the end of every PWM period 01= PWM reload event occurs one time every 2 PWM periods 10 = PWM reload event occurs one time every 4 PWM periods 11 = PWM reload event occurs one time every 8 PWM periods
5	INDEN	0 = PWM outputs operate as 3 complementary pairs 1 = PWM outputs operate as 6 independent channels
4	POL45	1 = Invert output polarity for channel pair PWM2 0 = Noninverted polarity for channel pair PWM2
3	POL23	1 = Invert output polarity for channel pair PWM1 0 = Noninverted polarity for channel pair PWM1
2	POL10	1 = Invert output polarity for channel pair PWM0 0 = Noninverted polarity for channel pair PWM0
1:0	PRES	00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8

PWM Deadband Register
PWMDB = F22h

7:0	PWMDB[7:0]	Sets the PWM deadband period for which both PWM outputs of a complementary PWM output pair are deasserted.
Note: This register can only be written when PWEN is cleared.		

PWM Minimum Pulse Width Filter Register
PWMMPF = F23h

7:0	PWMMPF	Sets the minimum allowed output pulse width in PWM clock cycles.
Note: This register can only be written when PWEN is cleared and must not be 00h.		

PWM Fault Mask Register
PWMFM = F24h

7:6		Reserved
5	DBGMSK	0 = Entering CPU DEBUG Mode generates a PWM fault 1 = Entering CPU DEBUG mode does not generate a PWM fault
4:3		Reserved
2	F1MASK	0 = Fault 1 generates a PWM fault 1 = Fault 1 does not generate a PWM fault
1	C0MASK	0 = Comparator generates a PWM fault 1 = Comparator does not generate a PWM fault
0	F0MASK	0 = Fault0 pin generates a PWM fault 1 = Fault0 pin does not generate a PWM fault

PWM Fault Status Register
PWMFSTAT = F25h

7	RLDFLAG	This bit is set and latched when a PWM timer reload occurs.
6		Reserved
5	DBGFLAG	This bit is set and latched when DEBUG mode is entered.
4:3		Reserved
2	F1FLAG	This bit is set and latched when Fault1 is asserted.
1	C0FLAG	This bit is set and latched when Comparator is asserted. .
0	FFLAG	This bit is set and latched when the FAULT0 input is asserted. .
Note: Writing a 1 to a FLAG bit clears the flag.		

PWM Fault Control Register
PWMFCTL = F28h

7		Reserved
6	DBGRST	0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered and a new PWM period begins. 1 = Software controlled recovery.
5	CMP1INT	0 = Interrupt on comparator assertion disabled 1 = Interrupt on comparator assertion enabled
4	CMP1RST	0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered. 1 = Software controlled recovery.
3	CMP0INT	0 = Interrupt on comparator 0 assertion disabled 1 = Interrupt on comparator 0 assertion enabled
2	CMP0RST	0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered. 1 = Software controlled recovery.
1	Fault0INT	0 = Interrupt on Fault0 pin assertion disabled 1 = Interrupt on Fault0 pin assertion enabled
0	Fault0RST	0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered. 1 = Software-controlled recovery.
Note: PWM resumes control of outputs only after all fault sources have deasserted and all fault flags are cleared and a PWM reload occurs. This register can only be written when PWEN is cleared.		

PWM Input Sample Register
PWMIN = F26h

7		Reserved
6	FAULT	0 = A Low signal was read on the FAULT pin 1 = A High signal was read on the FAULT pin
5:0	IN2L IN2H IN1L IN1H IN0L IN0H	A 0 in the bit location indicates a Low signal is read on the respective PWM pin A 1 in the bit location indicates a High signal is read on the respective PWM pin

PWM Output Control Register
PWMOUT = F27h

7:6		Reserved
5,3,1	OUT2L OUT1L OUT0L	0 = The PWM 2L/1L/0L output signal is enabled and controlled by the PWM 1 = The PWM 2L/1L/0L output signal is in a low-side Off-state
4,2,0	OUT2H OUT1H OUT0H	0 = The PWM 2H/1H/0H output signal is enabled and controlled by the PWM 1 = The PWM 2H/1H/0H output signal is in a high-side Off state

General Purpose Timer Registers

Timer 0 High Byte Register
T0H = F00h

7:0	TH	The high byte of the Timer0 count

Timer 0 Low Byte Register
T0L = F01h

7:0	TL	The low byte of the Timer0 count

Timer 0 Reload High Byte Register
T0RH = F02h

7:0	TRH	The high byte of the reload value for Timer0

Timer 0 Reload Low Byte Register
T0RL = F03h

7:0	TRL	The low byte of the reload value for Timer0

Timer 0 PWM High Byte Register
T0PWMH = F04h

7:0	PWMH	The high byte of the PWM compare value of Timer0

Timer 0 PWM Low Byte Register
T0PWML = F05h

7:0	PWML	The low byte of the PWM compare value of Timer0

Timer 0 Control 0 Register
T0CTL0 = F06h

7	TMODE[3]	Timer mode high bit (used with TMODE[2:0])
6:5	TICONFIG	Configures interrupt definitions for the following modes. ONE SHOT, CONTINUOUS, COUNTER, PWM, COMPARE, DUAL PWM, TRIGGERED ONE-SHOT, COMPARATOR COUNTER 00 = Timer interrupt occurs on reload 01 = Timer interrupt occurs on reload 10 = Timer interrupts are disabled 11 = Timer Interrupt occurs on reload GATED 00 = Timer interrupt occurs on reload 01 = Timer interrupt occurs on reload 10 = Timer interrupt occurs on inactive gate edge 11 Timer interrupt occurs on reload CAPTURE, CAPTURE/COMPARE, CAPTURE RESTART 00 = Timer interrupt occurs on reload and capture 01 = Timer interrupt occurs on reload and capture 10 = Timer interrupt occurs on capture only 11 = Timer interrupt occurs on reload only
4		Reserved
3:1	PWMD	000 = No delay 001 = 2 cycles delay 010 = 4 cycles delay 011 = 8 cycles delay 100 = 16 cycles delay 101 = 32 cycles delay 110 = 64 cycles delay 111 = 128 cycles delay
0	INCAP	0 = Previous timer interrupt is not a result of a timer input capture event 1 = Previous timer interrupt is a result of a timer input capture event

Timer 0 Control 1 Register
T0CTL1 = F07h

7	TEN	0 = Timer is disabled 1 = Timer enabled
6	TPOL	Timer Input/Output Polarity
5:3	PRES	000 = Divide by 1 001 = Divide by 2 010 = Divide by 4 011 = Divide by 8 100 = Divide by 16 101 = Divide by 32 110 = Divide by 64 111 = Divide by 128
2:0	TMODE[2:0]	Use with TMODE[3] in previous register to define mode. 0000 = ONE-SHOT mode 0001 = CONTINUOUS mode 0010 = COUNTER mode 0011 = PWM SINGLE OUTPUT mode 0100 = CAPTURE mode 0101 = COMPARE mode 0110 = GATED mode 0111 = CAPTURE/COMPARE mode 1000 = PWM DUAL OUTPUT mode 1001 = CAPTURE RESTART mode 1010 = COMPARATOR COUNTER mode 1011 = TRIGGERED ONE-SHOT mode

Interrupt Controller Registers

Reset, System Exception, and Interrupt Vectors in Order of Priority

Priority	Program Memory Vector Base Address	Interrupt or Trap Source
	Reset and System Exceptions	
	0002h	Reset
	0004h	Watch-Dog Timer
	003AH	Primary Oscillator Fail Trap
	003CH	Watch-Dog Timer Oscillator Fail Trap
	0006h	Illegal Instruction Trap
	Interrupts (maskable)	
Highest	0008h	PWM Timer
	000Ah	PWM Fault
	000Ch	ADC
	000Eh	Comparator output rising and falling edge
	0010h	Timer 0
	0012H	UART 0 receiver
	0014H	UART 0 transmitter
	0016H	SPI
	0018H	I2C
	001AH	Reserved
	001CH	Port C0 with selectable rising or falling input edge
	001EH	Port B[3:0] rising and fall input edge
	0020h	Port A7/A3 with selectable rising or falling input edge
	0022H	Port A6/A2 with selectable rising or falling input edge
	0024H	Port A5/A1 with selectable rising or falling input edge
	0026H	Port A4/A0 with selectable rising or falling input edge
Lowest	0028H–0039H	Reserved

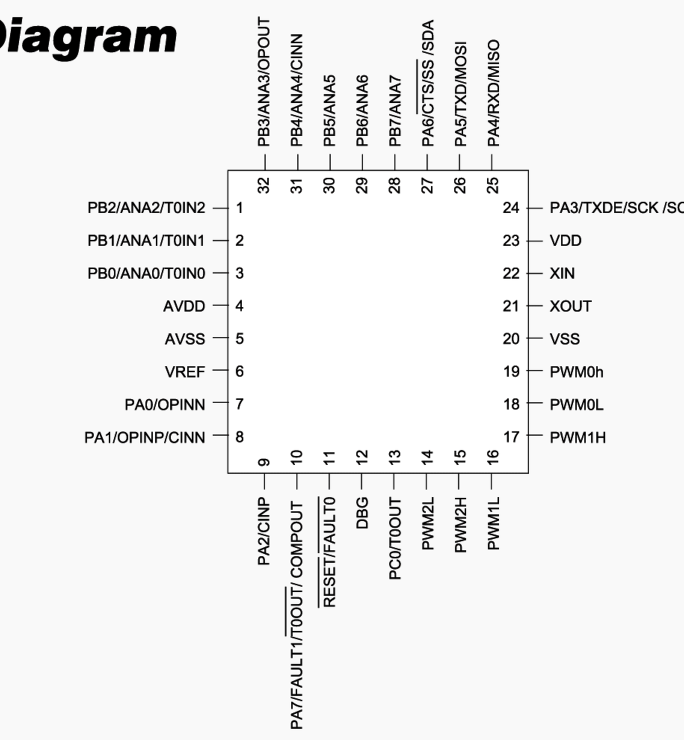
Interrupt Request 0 Register
IRQ0 = FC0h

7	PWMI	0 = No interrupt request is pending for the PWM 1 = Interrupt request from the PWM is awaiting service
6	FLTI	0 = No Fault interrupt request is pending. 1 = A Fault interrupt request is awaiting service
5	ADCI	0 = No interrupt request is pending for the ADC 1 = Interrupt request from the ADC is awaiting service
4	CMPI	0 = No interrupt request is pending for the comparators 1 = Interrupt request from the comparators is awaiting service
3	T0I	0 = No interrupt request is pending for Timer0 1 = Interrupt request from Timer0 is awaiting service
2	U0RXI	0 = No interrupt request is pending for the UART0 receiver 1 = Interrupt request from the UART0 receiver is awaiting service
1	U0TXI	0 = No interrupt request is pending for the UART0 transmitter 1 = Interrupt request from the UART0 transmitter is waiting service
0	SPII	0 = No interrupt request is pending for the SPI 1 = Interrupt request from the SPI is awaiting service

Interrupt Request 1 Register
IRQ1 = FC3h

7	I2CI	0 = No interrupt request is pending for I2C 1 = Interrupt request from I2C is awaiting service
6		Reserved
5	PC0I	0 = No interrupt request is pending for PC0 1 = Interrupt request from PC0 is awaiting service
4	PBI	0 = No interrupt request is pending for PB3 through PB0 1 = Interrupt request from PB3 through PB0, is awaiting service
3	PA73I	0 = No interrupt request is pending for PA7 or PA3 1 = Interrupt request from PA7 or PA3, is awaiting service
2	PA62I	0 = No interrupt request is pending for Port A6 or A2 1 = Interrupt request from PA6 or PA2, is awaiting service
1	PA51I	0 = No interrupt request is pending for PA5 or PA1 1 = Interrupt request from PA5 or PA1, is awaiting service
0	PA40I	0 = No interrupt request is pending for PA4 or pin PA0 1 = Interrupt request from PA4 or PA0, is awaiting service

Pin Diagram



Watch-Dog Timer Registers

Watch-Dog Timer Reload High Byte Register
(WDTH = FF2h)

7:0	WDTH	00h to FFh = The WDT Reload High Byte is the most significant byte, or bits [15:8] of the 16-bit WDT reload value

Watch-Dog Timer Reload Low Byte Register
(WDTL = FF3h)

7:0	WDTL	00h to FFh = The WDT Reload Low Byte is the least significant byte, or bits [7:0] of the 16-bit WDT reload value

First Op Code Map

Lower Nibble (Hex)

Upper Nibble (Hex)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	1.1 BRK	2.2 SRP IM	2.3 ADD r1,r2	2.4 ADD r1,Ir2	3.3 ADD R2,R1	3.4 ADD IR2,R1	3.3 ADD R1,IM	3.4 ADD IR1,IM	4.3 ADDX ER2,ER1	4.3 ADDX IM,ER1	2.3 DJNZ r1,X	2.2 JR cc,X	2.2 LD r1,IM	3.2 JP cc,DA	1.2 INC r1	1.2 NOP

Figure 57. First Op Code Map

Refer to the Product Specification for the 2nd Op Code Map

UART Registers

LIN-UART Transmit Data Register

LIN-UART Receive Data Register

LIN-UART Status 0 Register - Standard UART Mode

LIN-UART Status 0 Register - LIN Mode

LIN-UART Control 0 Register

LIN-UART Baud Rate High Byte Register

LIN-UART Baud Rate Low Byte Register

I²C Registers

I²C Control Registers

I²C Baud Rate High Byte Register

I²C Baud Rate Low Byte Register

I²C State Register

I²C State Register

I²C Mode Register

I²C Slave Register

SPI Registers

SPI Data Register

SPI Control Register

SPI Status Register

SPI Mode Register

LEGEND

Read/Write | Read Only | Write Only | Unique Parameter-dependent Read/Write Behavior | Reserved

FL009201-0705

WWW.ZILOG.COM

EMBEDDED IN LIFE