



Technical Note

Setting the GPIO Port Pins of the eZ80F91 MCU

TN003203-0707

Abstract

This Technical Note describes how to configure the GPIO pins of Zilog's eZ80F91 MCU for input, output, alternate functions, and interrupt-related operations.

Overview of General-Purpose Input/Output

The eZ80F91 device features 32 general-purpose input/output (GPIO) pins. These GPIO pins are assembled as four 8-bit ports:

1. Port A
2. Port B
3. Port C
4. Port D

All port pins can be configured either as inputs or outputs. In addition, all the port pins can be used as vectored interrupt sources for the eZ80[®] CPU. When setting these GPIO pins, it is important to consider the features of the port pins.

GPIO Operation

Input, output, and alternate function operations are the same for all four GPIO ports (ports A, B, C, and D). Each port features eight GPIO port pins. These eZ80F91 MCU GPIO ports can be configured in nine different modes using the following GPIO control registers:

- Port x Data Register (Px_DR)
- Port x Data Direction Register (Px_DDR)
- Port x Alternate Register 1 (Px_ALT1)
- Port x Alternate Register 2 (Px_ALT2)

Where x can be any of the four ports: A, B, C, or D.

GPIO Control Registers

The 16 GPIO control registers operate in groups of four with a set of registers for each port (Ports A, B, C, and D). Each GPIO port features a Port Data Register, a Port Data Direction Register, a Port Alternate Register 1, and a Port Alternate Register 2. In addition to these four control registers, each port also have a Port Alternate Register 0, which is used to clear edge-triggered interrupts.

Table 1 displays how the port control registers are organized into four words. Each control word represents an 8-bit value with each bit corresponding to one pin of the GPIO port. See [Quick Reference: GPIO Operating Modes](#) on page 10 for a brief discussion of the GPIO operating modes. For a complete and detailed explanation about GPIO operating modes and control registers, refer to *eZ80F91 Product Specification (PS0192)*, available for download on www.zilog.com.

Table 1. Alternate Function Mode for PA0

Mode Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Control Word
Px_DR	0	0	0	0	0	0	0	0	0x00
Px_DDR	0	0	0	0	0	0	0	1	0x01
Px_ALT1	0	0	0	0	0	0	0	0	0x00
Px_ALT2	0	0	0	0	0	0	0	1	0x01

Follow the steps below to set Port A, pin 0 (PA0) in alternate function mode. These register combinations will select the alternate function PWM0/OC0 for PA0.

1. Set PA_DR = 0x00
2. Set PA_ALT2 = 0x01
3. Set PA_ALT1 = 0x00
4. Set PA_DDR = 0x01

Figure 1 displays a block diagram of the eZ80F91 MCU’s GPIO port pins. A brief description of the functions of each GPIO control register is explained below:

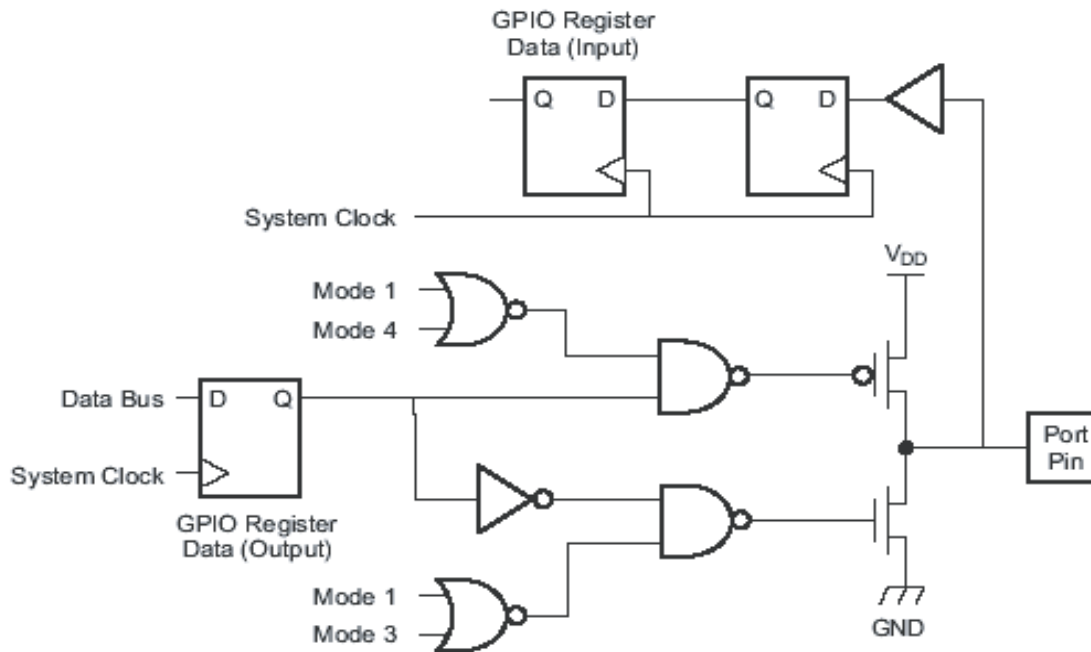


Figure 1. GPIO Port Pin Block Diagram

Port x Data Registers (Px_DR)

These registers function as control and data registers. When a pin is programmed as an output, data written to the Port x Data Registers is driven onto the corresponding pins. In all the GPIO operating modes, reading from the Port Data registers always returns the current sampled value of the data on the corresponding pins.

Port x Data Direction Registers (Px_DDR)

These registers in conjunction with the other control registers determine the operating mode of a GPIO port pin. See [Quick Reference: GPIO Operating Modes](#) on page 10 for a brief discussion of the GPIO operating modes.

Port x Alternate Register 1 (Px_ALT1)

The Port x Alternate Register 1 controls the operating modes of the GPIO port pins. See [Quick Reference: GPIO Operating Modes](#) on page 10 for a brief discussion of the GPIO operating modes.

Port x Alternate Register 2 (Px_ALT2)

The Port x Alternate Register 2 controls the operating modes of the GPIO port pins.

Port x Alternate Register 0 (Px_ALT0)

The Port x Alternate Register 0 is used to clear edge-triggered interrupts. When a pin is in one of the edge-triggered interrupt modes writing a one to this register will clear the interrupt. Px_ALT0 is a write only register.

► **Note:** For details about GPIO Control Registers, refer to *eZ80F91 Product Specification (PS0192)*.

Setting the GPIO Port Pins in Different Operating Modes

This section describes the settings of GPIO port pins in different modes of operation.

Setting the GPIO Port in Output Mode (Mode 1)

In this mode, the GPIO port pins are set as output pins. You can send data out through the GPIO port either by using any individual pin of the port or any pin combination or by using the entire port itself. For information on initializing the GPIO port pins for output mode, see [Table 1](#) on page 2.

Follow the steps below to set Port B as an output port with an initial value of logic High:

1. Set PB_DR = 0xFF
2. Set PB_ALT2 = 0x00
3. Set PB_ALT1 = 0x00
4. Set PB_DDR = 0x00

Follow the steps below to set bit 0 of the Port B to an initial value of logic High:

1. Set PB_DR = 0x01
2. Set PB_ALT2 = 0x00
3. Set PB_ALT1 = 0x00
4. Set PB_DDR = 0x00

Setting the GPIO Port in Input Mode (Mode 2)

In this mode, the GPIO port pin is configured as a standard digital input pin and the output is tristated (high impedance). Mode 2 is the default mode for all port pins. You can read data in through the GPIO port either by using any individual pin of the port or any pin combination or by using the entire port itself. [Table 1](#) on page 2 provides a reference for programming the control register to select Input mode.

Follow the steps below to set Port A as an input port:

1. Set PA_DR = 0xFF
2. Set PA_ALT2 = 0x00
3. Set PA_ALT1 = 0x00
4. Set PA_DDR = 0xFF

Setting the GPIO Port in Open Drain Mode (Mode 3)

The GPIO pins do not feature an internal pull-up resistor. Therefore, an external pull-up resistor must be used to connect the pin to the supply voltage when OPEN DRAIN mode is used. The state of the pin is determined by the value stored in the PA_DR register. If the register bit is set to 0, then the output of that bit is 0. However, if the bit is set to 1, the port pin is set to High impedance.

Follow the steps below to set Port A as open-drain. The output in this case is 0.

1. Set PA_DR = 0x00
2. Set PA_ALT2 = 0x00
3. Set PA_ALT1 = 0xFF
4. Set PA_DDR = 0x00

Setting the GPIO Port in Open Source Mode (Mode 4)

The GPIO pins do not feature an internal pull-down resistor, so an external pull-down resistor connecting the pin to ground is required in this mode. This mode is similar to OPEN DRAIN mode, in that the output value is determined by the value stored in the Px_DR.

► **Note:** *The driven value and the high impedance value are set opposite to OPEN DRAIN mode. In OPEN SOURCE mode a zero in the Px_DR will produce a high impedance at the pin while a one in the Px_DR produces a value of one at the pin.*

Follow the steps below to set Port A as open source. The output in this case is 1.

1. Set PA_DR = 0xFF
2. Set PA_ALT2 = 0x00
3. Set PA_ALT1 = 0xFF
4. Set PA_DDR = 0xFF

Setting the GPIO Port in Alternate Function Mode (Mode 7)

When a GPIO port pin is configured in the alternate function mode, it provides access to special on-chip peripheral functions such as timers and serial communication devices.

Table 2 lists the alternate functions associated with each GPIO port pin for the eZ80F91 MCU.

Table 2. Port Alternate Function Mapping*

Port	Pin	Alternate Function
Port A	PA0	PWM0/OC0
	PA1	PWM1/OC1
	PA2	PWM2/OC2
	PA3	PWM3/OC3
	PA4	$\overline{\text{PWM0/TOUT0}}$
	PA5	$\overline{\text{PWM1/TOUT1}}$
	PA6	$\overline{\text{PWM2/EC1}}$
	PA7	$\overline{\text{PWM3}}$
Port B	PB0	IC0/EC0
	PB1	IC1
	PB2	$\overline{\text{SS}}$
	PB3	SCK
	PB4	IC2
	PB5	IC3
	PB6	MISO
	PB7	MOSI
Port C	PC0	TxD1
	PC1	RxD1
	PC2	$\overline{\text{RTS1}}$
	PC3	$\overline{\text{CTS1}}$
	PC4	$\overline{\text{DTR1}}$
	PC5	$\overline{\text{DSR1}}$
	PC6	$\overline{\text{DCD1}}$
	PC7	$\overline{\text{RI1}}$

Table 2. Port Alternate Function Mapping* (Continued)

Port	Pin	Alternate Function
Port D	PD0	TxD0/IR_RxD
	PD1	RxD0/IR_TxD
	PD2	$\overline{\text{RTS0}}$
	PD3	$\overline{\text{CTS0}}$
	PD4	$\overline{\text{DTR0}}$
	PD5	$\overline{\text{DSR0}}$
	PD6	$\overline{\text{DCD0}}$
	PD7	$\overline{\text{RI0}}$

*All signals with an overline are active Low. For example, $\overline{\text{B/W}}$, for which WORD is active Low, and $\overline{\text{B/W}}$, for which BYTE is active Low.

From [Table 2](#), it is clear that some GPIO pins offer more than one alternate function. You can select only one function at a time by using the control register of that particular peripheral. For example, PA0 features two alternate functions—PWM0 (pulse width modulation) and OC0 (output capture). In this case, you can select either the PWM function or the OC function.

Assuming that you select UART0, the following steps illustrates how to configure Port D, pin 0 (PD0) and Port D, pin 1 (PD1) in the alternate function mode, resulting in PD0 functioning as an Rx pin of the UART and PD1 functioning as a Tx pin of the UART (RxD0 and TxD0, respectively).

1. Set PD_DR = 0x00
2. Set PD_DDR = 0x03
3. Set PD_ALT1 = 0x00
4. Set PD_ALT2 = 0x03

Setting the GPIO Port in Interrupt Mode

The eZ80F91 MCU supports three types of interrupts. They are dual edge-triggered interrupt, level-triggered interrupt, and rising or falling edge-triggered interrupt. For a detailed explanation of these interrupt modes, refer to *eZ80F91 Product Specification (PS0192)*.

Dual Edge-Trigger (Mode 6)

In this mode, the GPIO port generates interrupts at both falling and rising edges.

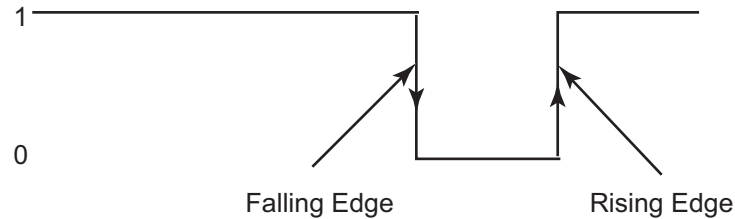


Figure 2. Input Signal at the Port Pin (Dual Edge-Trigger)

Follow the steps below to initialize Port D, pin 0 (PD0) for dual edge-trigger mode:

1. Set `PD_DR = 0x01`
2. Set `PD_ALT2 = 0x01`
3. Set `PD_ALT1 = 0x00`
4. Set `PD_DDR = 0x00`

The interrupt is then cleared by writing a one to the `Px_ALT0` register.

Set `PD_ALT0 = 0x01`

Level-Trigger (Mode 8)

When a GPIO port pin is configured for generating an interrupt at a given level (active level can be High or Low), it generates an interrupt when the selected level appears at port pin. The value stored in `Px_DR` determines whether the interrupt will be triggered by a low or high level. A zero in `Px_DR` selects low level interrupt while a one in `Px_DR` selects high level interrupt. The minimum input duration should be 2-system clocks. [Figure 3](#) displays the occurrence of an input signal at the port pin, in level-trigger mode.

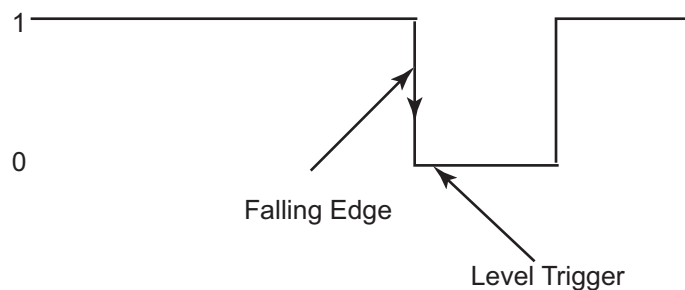


Figure 3. Input signal at the Port Pin (Level Trigger)

The following settings illustrates the initialization of PD0 in the level (active Low) trigger mode.

► **Note:** *The initialization sequence transitions the port pin through mode 9 (single edge interrupts) on the way to the desired mode 8.*

In order to eliminate the possibility of catching an unwanted edge interrupt while passing through mode 9 you should disable interrupts as the first step in the initialization process and clear the interrupts as the final step. These steps are displayed below:

1. Disable Interrupts
2. Set PD_DR = 0x00
3. Set PD_ALT2 = 0x01
4. Set PD_ALT1 = 0x01 (now in mode 9)
5. Set PD_DDR = 0x00 (now in mode 8)
6. Set PD_ALT0 = 0x01 (clear possible mode 9 interrupt)
7. Enable Interrupt

Interrupts requests in level sensitive mode remain asserted until the source of the interrupt is removed.

Single Edge-Trigger (Mode 9)

When a GPIO port pin is configured for single edge interrupt mode, it generates an interrupt when the selected edge appears on the port pin. The edge (rising or falling) is selected by the Px_DR. If Px_DR is set to zero falling edges will produce an interrupt. If Px_DR is set to one, rising edges will produce an interrupt.

Follow the steps below to initialize PD0 in the single edge-trigger mode for rising edge interrupt:

1. Set PD_DR = 0x01
2. Set PD_ALT2 = 0x01
3. Set PD_ALT1 = 0x01
4. Set PD_DDR = 0x01

For a falling edge interrupt the steps would be the same only as PD_DR would be set to 0x00 instead of 0x01. In either case the interrupt is cleared by writing a one to the Px_ALT0 register.

Set PD_ALT0 = 0x01 (to clear the interrupt)

► **Note:** *For a detailed explanation about GPIO operating modes, refer to eZ80F91 Product Specification (PS0192).*

Status of the Ports at RESET

After a RESET event, all GPIO port pins are configured as standard digital inputs (GPIO Mode 2), with interrupts disabled, and the output of the port is tristated (high impedance).

Table 3 lists the values at the GPIO port pins at RESET.

Table 3. Ports at RESET

Control Register	Defined Value	Value at RESET
Px_DR	Not Defined	Not defined.
Px_DDR	FFh	Port pins are initialized as input.
Px_ALT1	00h	No alternate function is selected.
Px_ALT2	00h	No alternate function is selected.
Px_ALTO	00h	No interrupt clears.

The port pins of the eZ80F91 MCU GPIO can be configured to generate external interrupt requests on either the rising edge, the falling edge, or the dual edge of the input signal. External interrupts are generated only when they are properly initialized. For a detailed explanation about GPIO external interrupts, refer to *eZ80F91 Product Specification (PS0192)*.

Summary

This Technical Note discusses how to conveniently use the eZ80F91 GPIO via the port control registers. The GPIO ports can be used as a source of external interrupts in modes 6, 8, and 9. In the alternate function mode, the GPIO port pins are configured to work with the on-chip peripherals of the eZ80[®] CPU.

Quick Reference: GPIO Operating Modes

The GPIO pin is configured for input, output, and alternate function operations using the GPIO Control registers. The operation is the same for each of the four GPIO ports (Ports A, B, C, and D). Each port features eight GPIO port pins. The operating mode for each pin is controlled by four bits that are divided between the four 8-bit control registers.

Table 4 describes the function of each port pin based on the above mentioned four control registers.

Table 4. GPIO Port Pin Control Register Functions

GPIO Mode	Px_ALT2 Bits 7:0	Px_ALT1 Bits 7:0	Px_DDR Bits 7:0	Px_DR Bits 7:0	Port Mode	Output
1	0	0	0	0	Output	0
	0	0	0	1	Output	1
2	0	0	1	0	Input from pin	High impedance
	0	0	1	1	Input from pin	High impedance
3	0	1	0	0	Open-drain output	0

Table 4. GPIO Port Pin Control Register Functions (Continued)

GPIO Mode	Px_ALT2 Bits 7:0	Px_ALT1 Bits 7:0	Px_DDR Bits 7:0	Px_DR Bits 7:0	Port Mode	Output
	0	1	0	1	Open-drain I/O	High impedance
4	0	1	1	0	Open-source I/O	High impedance
	0	1	1	1	Open-source output	1
5	1	0	0	0	Reserved	High impedance
6	1	0	0	1	Interrupt—dual ed.trig.	High impedance
7	1	0	1	0	Port A, C, or D—alt. fun	Controls port I/O
	1	0	1	1	Port A, C or D—alt.fun	Controls port I/O
8	1	1	0	0	Interrupt—active Low	High impedance
	1	1	0	1	Interrupt— active High	High impedance
9	1	1	1	0	Interrupt-fall, Edge, trig	High impedance
	1	1	1	1	Interrupt-rise, Edge, trig	High impedance

The nine GPIO operating modes of the eZ80F91 MCU are described below:

GPIO Mode 1—The port pin is configured as a standard digital output pin. The value written to the Port Data Register (Px_DR) is presented on the pin.

GPIO Mode 2—The port pin is configured as a standard digital input pin and the output is tristated (high impedance). The value stored in the Port Data Register produces no effect. As in all modes, a Read from the Port Data Register returns the pin value. GPIO Mode 2 is the default-operating mode following a RESET.

GPIO Mode 3—The port pin is configured as OPEN-DRAIN I/O. The GPIO pins do not feature an internal pull-up to the supply voltage. To employ the GPIO pin in OPEN-DRAIN mode, an external pull-up resistor must connect the pin to the supply voltage. Writing a 0 to the Port Data Register outputs a Low at the pin. Writing a 1 to the Port Data Register results in high-impedance output.

GPIO Mode 4—The port pin is configured as OPEN-SOURCE I/O. The GPIO pins do not feature an internal pull-down to the supply ground. To employ the GPIO pin in OPEN-SOURCE mode, an external pull-down resistor must connect the pin to the supply ground. Writing a 1 to the Port Data Register outputs a High at the pin. Writing a 0 to the Port Data Register results in a high-impedance output.

GPIO Mode 5—Reserved. This pin produces high-impedance output.

GPIO Mode 6—The port pin is configured for dual edge-triggered interrupt mode. Both a rising and a falling edge on the pin cause an interrupt request to be sent to the CPU. Writing a 1 to a Port Alternate Register 0 bit resets the corresponding interrupt request.

GPIO Mode 7—For Ports A, B, C, and D, the port pin is configured to pass control over to the alternate (secondary) functions assigned to the pin. The value in the Port Data Register produces no effect on operation.

► **Note:** *When Alternate function mode is not selected, inputs to the alternate function blocks are held in a de-asserted state. For instance, if an alternate function pin is a low level true input and alternate function mode is not selected the block will see a high level on that input pin.*

GPIO Mode 8—The port pin is configured for level-sensitive interrupt modes. An interrupt request is generated when the level at the pin is the same as the level stored in the Port Data Register for 2 system clocks. Interrupt requests in level sensitive mode remain asserted until the source of the request is removed.

GPIO Mode 9—The port pin is configured for a single edge-triggered interrupt mode. The value in the Port Data Register determines whether a positive or negative edge causes an interrupt request. Writing a 0 to the Port Data Register bit sets the selected pin to generate an interrupt request for falling edges. Writing a 1 to the Port Data Register bit sets the selected pin to generate an interrupt request for rising edges. If a port pin is configured for an edge-trigger interrupt, writing a 1 to the Port Alternate Register 0 causes a reset of the edge-trigger interrupt.



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