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An IXYS Company

eZ80190 Development Kit

User Manual

UM014108-0810

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Safeguards

The following precautions must be observed when working with the devices described in this document.

⚠ **Caution:** Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

Table of Contents

Introduction

The eZ80190 Development Kit provides a general-purpose platform for evaluating the capabilities and operation of ZiLOG's eZ80190 microprocessor. The eZ80F91 Development Kit features two primary boards: the eZ80Acclaim!® Development Platform and the eZ80190 Module. This arrangement provides a full development platform when using both boards. It can also provide a smaller-sized reference platform with the eZ80190 Module as a stand-alone development tool.

Kit Features

The key features of the eZ80190 Development Kit are:

- eZ80Acclaim!® Development Platform:
    - Up to 2 MB fast SRAM (12 ns access time)
    - Embedded Modem Socket with a U.S. Telephone Line Interface
    - I^{2}C EEPROM
    - I^{2}C Configuration Register
    - GPIO Port and Memory Headers
    - LEDs, including a 7 x 5 LED matrix
    - Jumpers
    - Two RS232 connectors—Console, Modem
    - 9 VDC Power Connector
    - RS485 connector[1]
    - JTAG Debug Interface[1]
    - ZiLOG Debug Interface (ZDI)
    - ZiLOG Developer Studio II and the eZ80® C-Compiler

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1. The eZ80Acclaim!® Development Platform's RS485 and JTAG functions are not supported on the eZ80190 device.

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- eZ80190 Module:
  - eZ80190 device operating at 50 MHz
  - 1 MB Flash Memory
  - 512 KB SRAM
  - 10 BaseT Ethernet Interface
  - Real-Time Clock with Battery Back-Up
- ZPAK II Debug Interface Tool
- 4-port 10 BaseT Ethernet hub
- eZ80® Software and Documentation CD-ROM

Hardware Specifications

Table 1 lists the specifications of the eZ80Acclaim!® Development Platform.

**Table 1. eZ80Acclaim!® Development Platform
Hardware Specifications**

Operating Temperature:	20ºC ±5ºC
Operating Voltage:	9 VDC

eZ80190 Development Board Revision History

99C0858-001 Rev C or later:

10/20/03 - Updated layout and added reset fix.

05/30/06 - The following components are not populated on the board:

- U11: Triac, SCR Phone Line D0-214
- U26 and U27: IC RS485, XCVR, Low PWR, 8-SOIC
- C3 and C4: CAP 1000pF Ceramic Disc 1KV
- D1 and D3: Diode LED Amber 0805 SMT

- – T1: Inductor Ferrite Bead, 2x15 Turns
- – J1: Conn HDR/Pin 1x32 2mm socket
- – J5: Conn HDR/Pin 1x2 2mm socket
- – J9: Conn HDR/Pin 1x9 2mm socket
- – P4: Conn RJ14 Jack 6-Pos 4-CKT
- – P5: Conn 9-CKT Cir rt-angl PC Mount

eZ80Acclaim! Development Platform Overview

The purpose of the eZ80190 Development Kit is to provide the developer with a set of tools for evaluating the features of the eZ80® family of devices, and to be able to develop a new application before building application hardware. The eZ80Acclaim!® Development Platform is designed to accept a number of application-specific modules and eZ80®-based add-on modules, including the eZ80190 Module, which features an Ethernet MAC, a Real-Time Clock, and the eZ80190 microprocessor with a fast Multiply-Accumulate unit.

When attached to the eZ80® Development Platform, the eZ80190 Module can operate in stand-alone mode with Flash memory, or interface via the ZPAK II debug interface tool to a host PC running ZiLOG Developer Studio II Integrated Development Environment (ZDS IDE) software. If the user's eZ80® application demands Internet connectivity and/or a network connection, the eZ80190 microprocessor can serve web pages over a TCP/IP network, allowing easy system monitoring and control, and effortless processor code updates.

The address bus, data bus, and all eZ80190 Module control signals are buffered on the eZ80Acclaim!® Development Platform to provide sufficient drive capability.

A block diagram of the eZ80Acclaim!® Development Platform and the eZ80190 Module is shown in Figure 1.

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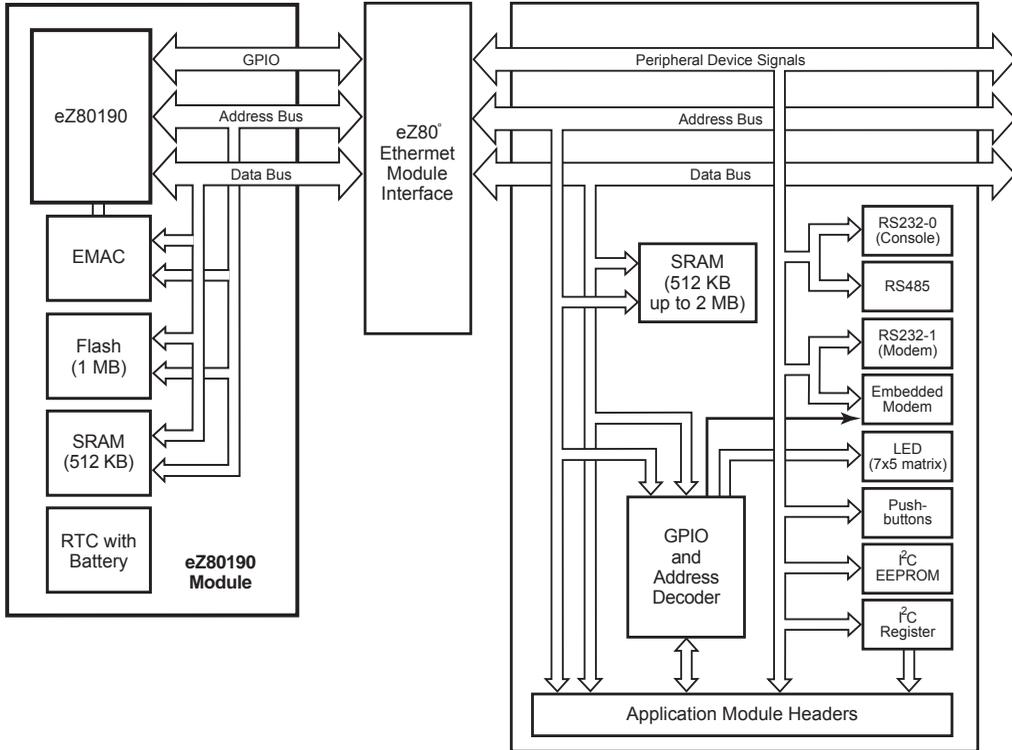
**Figure 1. eZ80Acclaim!® Development Platform Block Diagram
with eZ80190 Module**

Figure 2 is a photographic representation of the eZ80Acclaim!® Development Platform segmented into its key blocks, as shown in the legend for the figure.
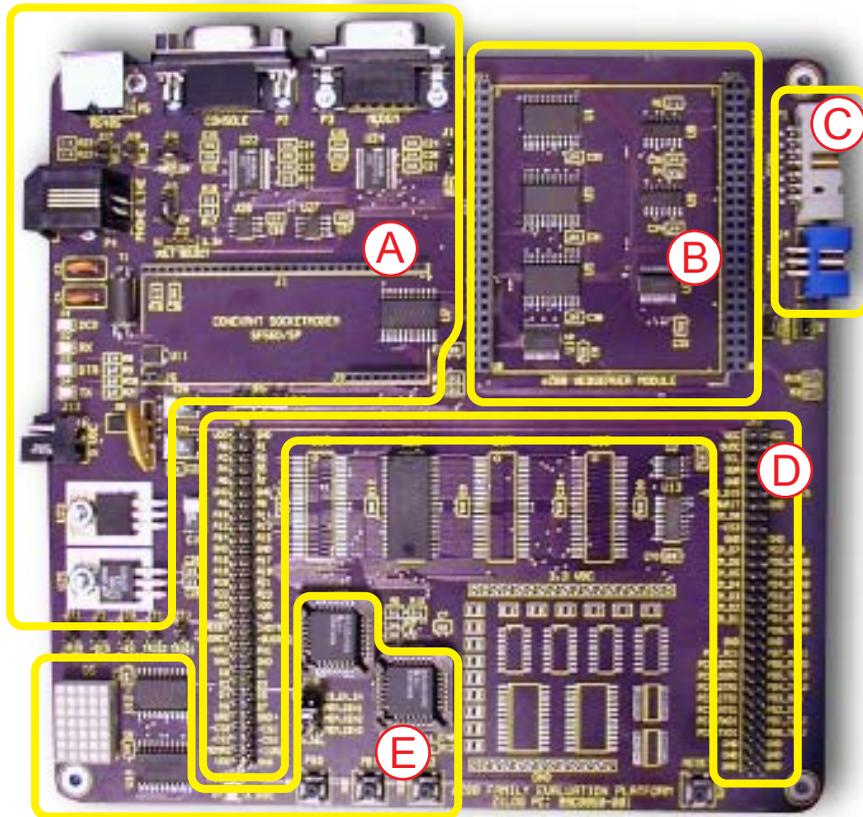
Key to blocks A–E:
A. Power and serial communications.
B. eZ80190 Module interface.
C. Debug interface.
D. Application module interfaces.
E. General-Purpose Port and LED with address decoder.

Figure 2. The eZ80Acclaim!® **Development Platform**

Figure 3 is a photographic representation of the eZ80190 Module segmented into its key blocks, as shown in the legend for the figure.
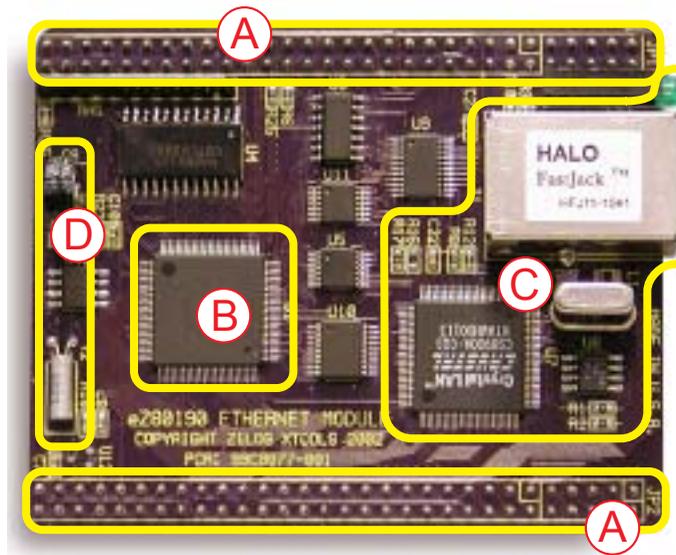
Note: Key to blocks A–D.
    A. eZ80190 Module interfaces.
    B. eZ80190 CPU.
    C. 10/100 BaseT Ethernet Interface
    D. IrDA transceiver.

Figure 3. The eZ80190 Module

The structures of the eZ80Acclaim!® Development Platform and the eZ80190 Module are illustrated in the Schematic Diagrams starting on page 61.

eZ80Acclaim! Development Platform

This section describes the eZ80Acclaim!® Development Platform hardware, its key components and its interfaces, including detailed programmer interface information such as memory maps, register definitions, and interrupt usage.

Functional Description

The eZ80Acclaim!® Development Platform consists of seven major hardware blocks. These blocks, listed below, are diagrammed in Figure 4.

- eZ80190 Module interface (2 male headers)

- Power supply for the eZ80Acclaim!® Development Platform, the eZ80190 Module, and application modules

- Application Module interface (2 female headers)

- General-Purpose Port and LED matrix

- RS232 serial communications ports

- Embedded modem interface

- I^2C devices

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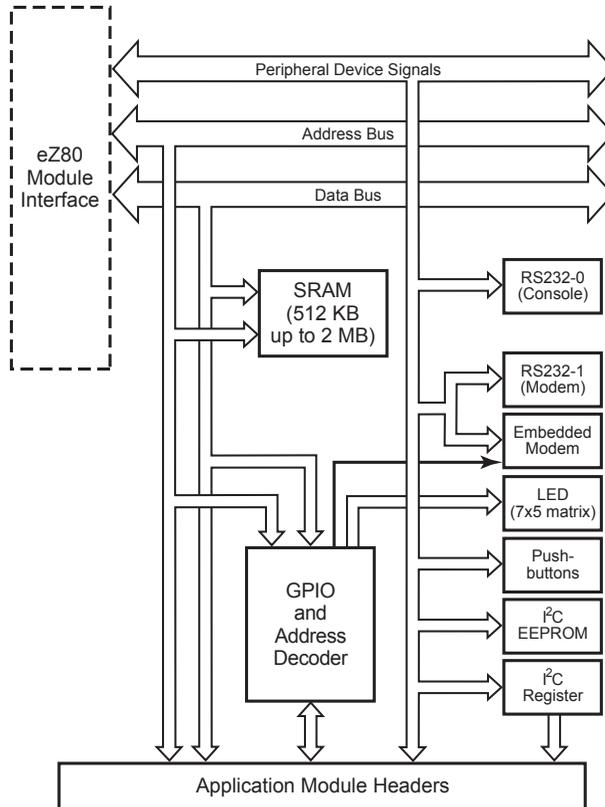
Figure 4. Basic eZ80Acclaim!® Development Platform Block Diagram

Physical Dimensions

The dimensions of the eZ80Acclaim!® Development Platform PCB is 177.8 mm x 182.9 mm. The overall height is 38.1 mm. See Figure 5.

Figure 5. Physical Dimensions of the eZ80Acclaim!® Development Platform
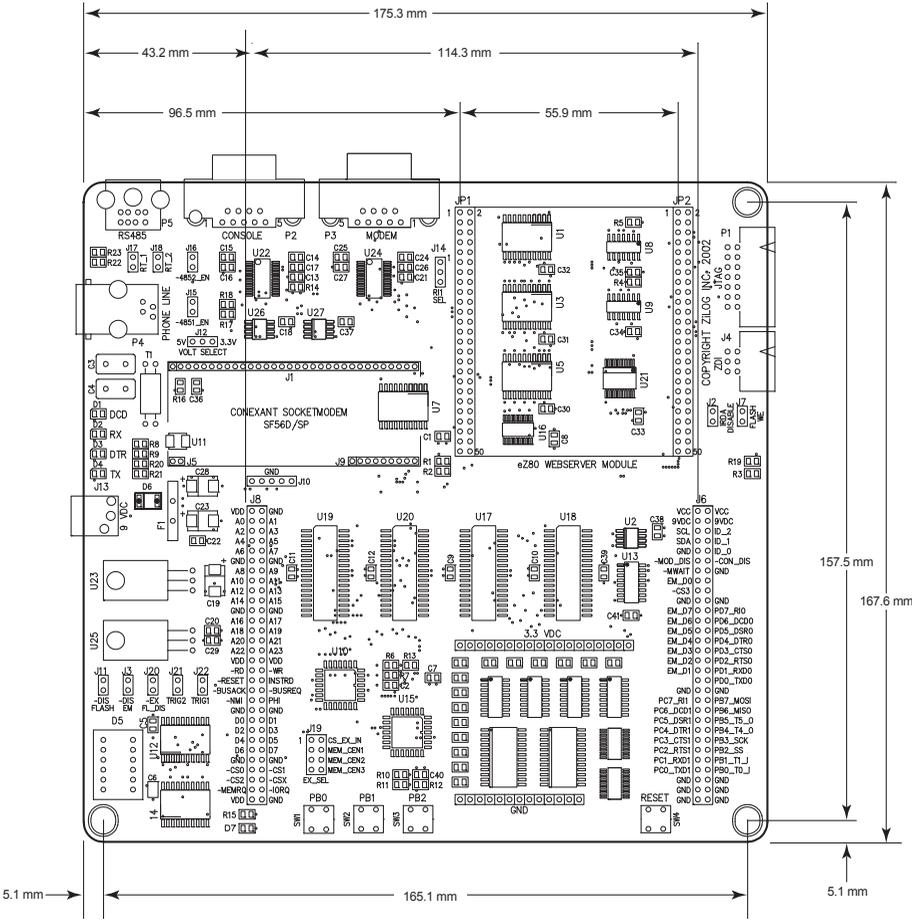
Operational Description

The eZ80Acclaim!® Development Platform can accept any eZ80®-core-based modules, provided that the module interfaces correctly to the eZ80Acclaim!® Development Platform. The purpose of the eZ80Acclaim!® Development Platform is to provide the application developer with a tool to evaluate the features of the eZ80190 device and to develop an application without building additional hardware.

eZ80190 Module Interface

The eZ80190 Module interface provides easy an connection for the eZ80190 Module. This interface is designed to fit future eZ80® modules and user-developed modules using current eZ80® devices.

The eZ80190 Module interface consists of two 50-pin receptacles, JP1 and JP2, which are described in the next pages.

Peripheral Bus Connector (JP1)

Figure 6 illustrates the pin layout of the Peripheral Bus Connector in the 50-pin header, located at position JP1 on the eZ80Acclaim!® Development Platform. Table 2 describes the pins and their functions.

```
                    JP1
        A6    ┌─────────┐    A0
       A10    │  1    2 │    A3
   GND_EXT    │  3    4 │    V3.3_EXT
        A8    │  5    6 │    A7
       A13    │  7    8 │    A9
       A15    │  9   10 │    A14
       A18    │ 11   12 │    A16
       A19    │ 13   14 │    GND_EXT
        A2    │ 15   16 │    A1
       A11    │ 17   18 │    A12
        A4    │ 19   20 │    A20
        A5    │ 21   22 │    A17
    DIS_ETH   │ 23   24 │    DIS_FLASH
       A21    │ 25   26 │    V3.3_EXT
       A22    │ 27   28 │    A23
       CS0    │ 29   30 │    CS1
       CS2    │ 31   32 │    D0
        D1    │ 33   34 │    D2
        D3    │ 35   36 │    D4
        D5    │ 37   38 │    GND_EXT
        D7    │ 39   40 │    D6
      MREQ    │ 41   42 │    IOREQ
   GND_EXT    │ 43   44 │    RD
        WR    │ 45   46 │    INSTRD
    BUSACK    │ 47   48 │    BUSREQ
              │ 49   50 │
              └─────────┘
          HEADER 25X2
          IDC50
```
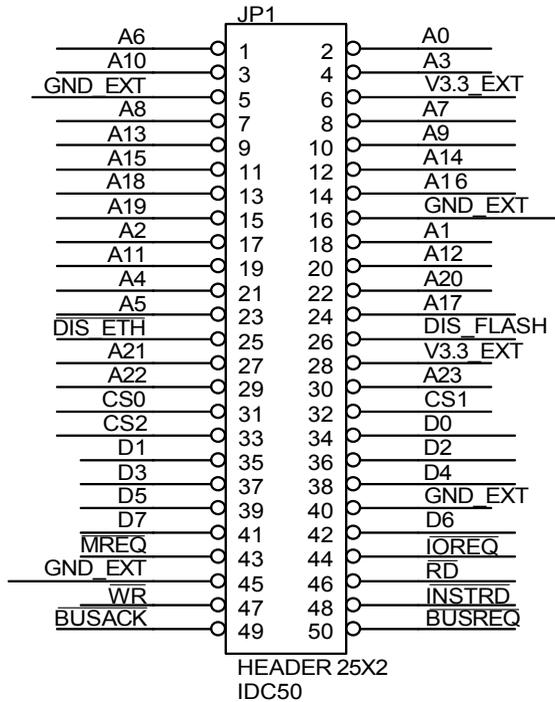
**Figure 6. eZ80Acclaim!® Development Platform
Peripheral Bus Connector Pin Configuration—JP1**

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**Table 2. eZ80Acclaim!® Development Platform
Peripheral Bus Connector Identification—JP1[1]**

Pin #	Symbol	Signal Direction	Active Level	eZ801900100ZCO Signal[2]
1	A6	Bidirectional		Yes
2	A0	Bidirectional		Yes
3	A10	Bidirectional		Yes
4	A3	Bidirectional		Yes
5	GND			
6	V_{DD}			
7	A8	Bidirectional		Yes
8	A7	Bidirectional		Yes
9	A13	Bidirectional		Yes
10	A9	Bidirectional		Yes
11	A15	Bidirectional		Yes
12	A14	Bidirectional		Yes
13	A18	Bidirectional		Yes
14	A16	Bidirectional		Yes
15	A19	Bidirectional		Yes

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80190 Module Schematic Diagrams on pages 66 through 73.

2. The Power and Ground nets are connected directly to the eZ801900100ZCO device.

Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

**Table 2. eZ80Acclaim!® Development Platform
Peripheral Bus Connector Identification—JP1[1] (Continued)**

Pin #	Symbol	Signal Direction	Active Level	eZ801900100ZCO Signal[2]
16	GND			
17	A2	Bidirectional		Yes
18	A1	Bidirectional		Yes
19	A11	Bidirectional		Yes
20	A12	Bidirectional		Yes
21	A4	Bidirectional		Yes
22	A20	Bidirectional		Yes
23	A5	Bidirectional		Yes
24	A17	Bidirectional		Yes
25	$\overline{DIS\_ETH}$	Output	Low	No
26	$\overline{EN\_FLASH}$	Output	Low	No
27	A21	Bidirectional		Yes
28	V_{DD}			
29	A22	Bidirectional		Yes
30	A23	Bidirectional		Yes

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80190 Module Schematic Diagrams on pages 66 through 73.

2. The Power and Ground nets are connected directly to the eZ801900100ZCO device.

Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

**Table 2. eZ80Acclaim!® Development Platform
Peripheral Bus Connector Identification—JP1[1] (Continued)**

Pin #	Symbol	Signal Direction	Active Level	eZ801900100ZCO Signal[2]
31	$\overline{CS0}$	Input	Low	Yes
32	$\overline{CS1}$	Input	Low	Yes
33	$\overline{CS2}$	Input	Low	Yes
34	D0	Bidirectional		Yes
35	D1	Bidirectional		Yes
36	D2	Bidirectional		No
37	D3	Bidirectional		Yes
38	D4	Bidirectional		Yes
39	D5	Bidirectional		Yes
40	GND			
41	D7	Bidirectional		Yes
42	D6	Bidirectional		Yes
43	$\overline{MREQ}$	Bidirectional	Low	Yes
44	$\overline{IORQ}$	Bidirectional	Low	Yes
45	GND			

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80190 Module Schematic Diagrams on pages 66 through 73.

2. The Power and Ground nets are connected directly to the eZ801900100ZCO device.

Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

**Table 2. eZ80Acclaim!® Development Platform
Peripheral Bus Connector Identification—JP1[1] (Continued)**

Pin #	Symbol	Signal Direction	Active Level	eZ801900100ZCO Signal[2]
46	$\overline{RD}$	Bidirectional	Low	Yes
47	$\overline{WR}$	Bidirectional	Low	Yes
48	$\overline{INSTRD}$	Input	Low	Yes
49	$\overline{BUSACK}$	Input	Pull-Up 10K¾; Low	Yes
50	$\overline{BUSREQ}$	Output	Pull-Up 10K¾; Low	Yes

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80190 Module Schematic Diagrams on pages 66 through 73.

2. The Power and Ground nets are connected directly to the eZ801900100ZCO device.

Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

I/O Connector (JP2)

Figure 7 illustrates the pin layout of the eZ80Acclaim!® Development Platform's I/O Connector in the 50-pin header. The I/O Connector is located at position JP2 on the eZ80Acclaim!® Development Platform. Table 3 describes the pins and their functions.
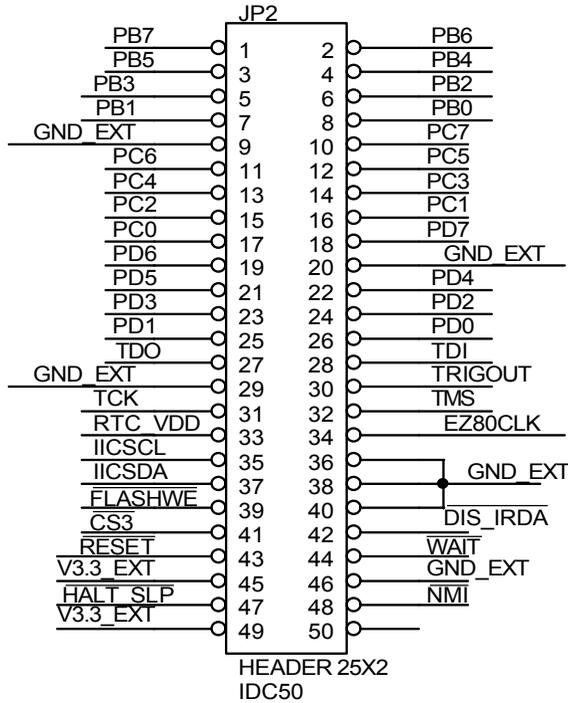
Figure 7. eZ80Acclaim![®] **Development Platform**
I/O Connector Pin Configuration—JP2

**Table 3. eZ80Acclaim!® Development Platform
I/O Connector Identification—JP2[1]**

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1	PB7	Bidirectional		Yes
2	PB6	Bidirectional		Yes
3	PB5	Bidirectional		Yes
4	PB4	Bidirectional		Yes
5	PB3	Bidirectional		Yes
6	PB2	Bidirectional		Yes
7	PB1	Bidirectional		Yes
8	PB0	Bidirectional		Yes
9	GND			
10	PC7	Bidirectional		Yes
11	PC6	Bidirectional		Yes
12	PC5	Bidirectional		Yes
13	PC4	Bidirectional		Yes
14	PC3	Bidirectional		Yes
15	PC2	Bidirectional		Yes
16	PC1	Bidirectional		Yes
17	PC0	Bidirectional		Yes
18	PD7	Bidirectional		Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80190 Module Schematic Diagrams on pages 66 through 73.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

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**Table 3. eZ80Acclaim!® Development Platform
I/O Connector Identification—JP2[1] (Continued)**

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
19	PD6	Bidirectional		
20	GND			
21	PD5	Bidirectional		Yes
22	PD4	Bidirectional		Yes
23	PD3	Bidirectional		Yes
24	PD2	Bidirectional		Yes
25	PD1	Bidirectional		Yes
26	PD0	Bidirectional		Yes
27	TDO	Input		Yes
28	TDI/ZDA	Output		Yes
29	GND			
30	TRIGOUT	Input	High	
31	TCK/ZCL	Output		Yes
32	TMS	Output	High	Yes
33	RTC_V_{DD}			
34	EZ80CLK	Input		Yes
35	SCL	Bidirectional		Yes
36	GND			

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80190 Module Schematic Diagrams on pages 66 through 73.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

**Table 3. eZ80Acclaim!® Development Platform
I/O Connector Identification—JP2[1] (Continued)**

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
37	SDA	Bidirectional		Yes
38	GND			
39	$\overline{\text{FlashWE}}$	Output	Low	No
40	GND			
41	$\overline{\text{CS3}}$	Input	Low	Yes
42	$\overline{\text{DIS\_IrDA}}$	Output	Low	No
43	$\overline{\text{RESET}}$	Bidirectional	Low	Yes
44	$\overline{\text{WAIT}}$	Output	Pull-Up 10K¾; Low	Yes
45	V_{DD}			
46	GND			
47	$\overline{\text{HALT\_SLP}}$	Input	Low	Yes
48	$\overline{\text{NMI}}$	Output	Low	Yes
49	V_{DD}			
50	Reserved			

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80190 Module Schematic Diagrams on pages 66 through 73.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Almost all of the connectors' signals are received directly from the CPU. Four input signals, in particular, offer options to the application developer by disabling certain functions of the eZ80190 Module.

These four inputs are:

- Disable Ethernet ($\overline{\text{DIS\_ETH}}$)
- Enable Flash ($\overline{\text{EN\_FLASH}}$)
- Flash Write Enable ($\overline{\text{FlashWE}}$)
- Disable IrDA (DIS_IrDA—not used)

These four signals are described below.

Disable Ethernet

When active Low, the $\overline{\text{DIS\_ETH}}$ output signal disables the EMAC from responding to CPU requests. As a result, additional input/output or memory devices can be used in the $\overline{\text{CS3}}$ address space. The logic that disables the Ethernet signal is listed in <u>Appendix A</u> on page 74.

Disable Flash

When active Low, the $\overline{\text{EN\_FLASH}}$ input signal disables the Flash chip on the eZ80190 Module.

Flash Write Enable

When active Low, the $\overline{\text{FlashWE}}$ input signal enables Write operations on the Flash boot block of the eZ80190 Module.

Disable IrDA

This signal does not perform a function on the eZ80190 Module. UART0 is always used with the RS232 interface on the eZ80Acclaim!® Development Platform.

Application Module Interface

An Application Module Interface is provided to allow the user to add an application-specific module to the eZ80Acclaim!® Development Platform. ZiLOG's Thermostat Application Module (not provided in the kit) is an example application-specific module that demonstrates an HVAC control system.

To design an application module, the user should be familiar with the architecture and features of the eZ80190 Module currently installed. Implementing an application module via the Application Module Interface requires that the eZ80190 Module also be mounted on the eZ80Acclaim!® Development Platform, because it (the eZ80190 Module) contains the eZ80190 microprocessor. To mount an application module, use the two male connectors J6 and J8.

Connector J6 carries the GPIO signals, and connector J8 carries memory and control signals. Tables 4 and 5 list the signals and functions related to each of these jumpers by pin. Power and ground signals are omitted for the sake of simplicity.

Table 4. GPIO Port Connector J6*

Signal	Pin #	Function	Direction	Notes
SCL	5	I^2C Clock	Bidirectional	
SDA	7	I^2C Data	Bidirectional	
MOD_DIS	9	Modem Disable	Input	If a shunt is installed between pins 6 and 9, the modem function on the eZ80Acclaim!® Development Platform is disabled.
MWAIT	13	WAIT signal for the CPU	Input	This signal does not perform a function on the eZ80190 Module.
EM_D0	15	GPIO, Bit 0	Bidirectional	
CS3	17	Chip Select 3 of the CPU	Output	This signal is also present on the J8.
EM_D[7:1]	21,23,25, 27,29,31, 33	Port A, Bit [7:1]	Bidirectional	

Note: *All of the signals are driven directly by the CPU.

Table 4. GPIO Port Connector J6* (Continued)

Signal	Pin #	Function	Direction	Notes
Reserved	35			
PC[7:0]	39,41,43, 45,47,49, 51,53	Port C, Bit [7:0]	Bidirectional	
ID_[2:0]	6,8,10	eZ80Acclaim!® Development Platform ID	Output	
CON_DIS	12	Console Disable	Input	If a shunt is installed between pins 12 and 14, the Console function on the eZ80Acclaim!® Development Platform is disabled.
Reserved	16,18			
PD[7:0]	22,24,26, 28,30,32, 34,36	Port D, Bit[7:0]	Bidirectional	
PB[7:0]	40,42,44, 46,48,50, 52,54	Port B, Bit[7:0]	Bidirectional	
Note: *All of the signals are driven directly by the CPU.				

Table 5. CPU Bus Connector J8*

Signal	Pin #	Function	Direction
A[0:7]	3–10	Address Bus, Low Byte	Output
A[8:15]	13–20	Address Bus, High Byte	Output
A[16:23]	23–30	Address Bus, Upper Byte	Output
$\overline{RD}$	33	Read Signal	Output
$\overline{RESET}$	35	Push Button Reset	Output
$\overline{BUSACK}$	37	CPU Bus Acknowledge Signal	Output
$\overline{NMI}$	39	Nonmaskable Interrupt	Input
D[0:7]	43–50	Data Bus	Bidirectional
CS[0:3]	53–56	Chip Selects	Output
$\overline{MREQ}$	57	Memory Request	Output
$\overline{WR}$	34	Write Signal	Output
$\overline{INSTRD}$	36	Instruction Fetch	Output
$\overline{BUSREQ}$	38	CPU Bus Request signal	Input
PHY	40	Clock output of the CPU	Output

Note: *All of the signals except BUSACK and INSTRD are driven by low-voltage CMOS technology (LVC) drivers.

I/O Functionality

The eZ80Acclaim!® Development Platform provides additional functionality, featuring general-purpose port, an LED matrix, a modem reset, and two user triggers. These functions are memory-mapped with an address decoder based on the Generic Array Logic GAL22lV10D (U15) device manufactured by Lattice Semiconductor, and a bidirectional latch (U16). Additionally, U15 is used to decode addresses for access to the 7x5 LED matrix.

Table 6 lists the memory map addresses to registers that allow access to the above functions. The register at address 800000h controls general-purpose port output control and LED anode register functions. The register at address 800001h controls the register functions for the LED cathode, modem reset, and user triggers. Address 800002h controls general-purpose port data.

Table 6. LED and Port Emulation Addresses

Address	Register Function	Access
800000h	LED Anode/General-Purpose Port Output Control	$\overline{\text{WR}}$
800001h	LED Cathode/Modem/Trig	$\overline{\text{WR}}$
800002h	General-Purpose Port Data	$\overline{\text{RD}}$/$\overline{\text{WR}}$

General-Purpose Port

The general-purpose port is emulated with the use of the GPIO Output Control Register and the GPIO Data Register. If bit 7 in the GPIO Output Control Register is 1, all of the lines on the general-purpose port are configured as inputs. If this bit is 0, all of the lines on the general-purpose port are configured as outputs. Table 7 lists the multiple functions of the register.

Table 7. LED Anode/General-Purpose Port Output Control Register

Function	7	6	5	4	3	2	1	0
Anode Col 1								X
Anode Col 2							X	
Anode Col 3						X		
Anode Col 4					X			

(Bit # spans columns 7 through 0)

Table 7. LED Anode/General-Purpose Port Output Control Register (Continued)

	Bit #							
Function	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Anode Col 5				X				
Anode Col 6			X					
Anode Col 6		X						
GPIO Output	X							

The GPIO Data Register receives inputs or provides outputs for each of the seven general-purpose port lines, depending on the configuration of the port. See Table 8.

Table 8. General-Purpose Port Data Register

	Bit #							
Function	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GPIO D0								X
GPIO D1							X	
GPIO D2						X		
GPIO D3					X			
GPIO D4				X				
GPIO D5			X					
GPIO D6		X						
GPIO D7	X							

⚠ **Caution:** Reading from the general-purpose port can damage the drivers used for the general-purpose port and memory. The port can, however, be used for writing data.

LED Matrix

The one 7x5 LED matrix device on the eZ80Acclaim!® Development Platform is a memory-mapped device that can be used to display information, such as programmed alphanumeric characters. For example, the LED display sample program that is shipped with this kit displays the alphanumeric message:

```
eZ80
```

To illuminate any LED in the matrix, its respective anode bit must be set to 1 and its corresponding cathode bit must be set to 0.

Bits 0–6 in Table 7 are LED anode bits. They must be set High (1) and their corresponding cathode bits, bits 0–4 in Table 9, must be set Low (0) to illuminate each of the LED's, respectively.

Bit 7 in Table 7 does not carry any significance within the LED matrix. It is used for the general-purpose port as a control bit.

Table 9 indicates the multiple register functions of the LED cathode, modem, and triggers. This table shows the bit configuration for each cathode bit. Bits 5, 6, and 7 do not carry any significance within the LED matrix. These three bits are control bits for the modem reset, Trig1, and Trig2 functions, respectively.

Table 9. Bit Access to the LED Cathode, Modem, and Triggers

Function	Bit #							
	7	6	5	4	3	2	1	0
Cathode Row 5								X
Cathode Row 4							X	
Cathode Row 3						X		
Cathode Row 2					X			

Table 9. Bit Access to the LED Cathode, Modem, and Triggers (Continued)

Function	Bit #							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Cathode Row 1				X				
MRESET			X					
Trig 1		X						
Trig 2	X							

An LED display sample program is shipped with the eZ80190 Development Kit. Please refer to the *eZ80190 Development Kit Quick Start Guide* (QS0004) or to the Tutorial section in the *ZiLOG Developer Studio II—eZ80Acclaim! User Manual* (UM0144).

Modem Reset

The Modem Reset signal, MRESET, is used to reset an optional socket modem. This signal is controlled by bit 5 in the register shown in Table 9. The MRESET signal is available at the embedded modem socket interface (J9, Pin 1). Setting this bit Low places the optional socket modem into a reset state. The user must pull this bit High again to enable the socket modem. Reference the appropriate documentation for the socket modem to reset timing requirements. More information about this signal is provided in the next section.

User Triggers

Two general-purpose trigger output pins are provided on the eZ80Acclaim!® Development Platform. Labeled J21 (Trig2) and J22 (Trig1), these pins allow the user a way to *trigger* external equipment to aid in the debug of the system. See Figure 8 for trigger pin details.
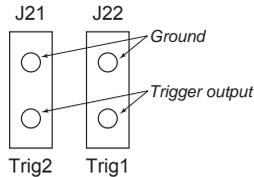
Figure 8. Trigger Pins J21 and J22

Bits 6 and 7 in Table 9 are the control bits for the user triggers. If either bit is a 1, the corresponding Trig1 and Trig2 signals are driven High. If either bit is 0, the corresponding Trig1 and Trig2 signals are driven Low.

Embedded Modem Socket Interface

The eZ80Acclaim!® Development Platform features a socket for an optional 56K modem (a modem is not included in the kit). The tested modem for this eZ80190 Development Kit is a Conexant socket modem, part number SF56D/SP. Information about this modem and its interface is available in the SmartSCM SocketModem data sheet (Doc. No. 101522D) from www.conexant.com.

Connectors J1, J5, and J9 provide connection capability. The modem socket interface provided by these three connectors is shown in Figure 9. Tables 10 through 12 identify the pins for each connector. The embedded modem utilizes UART1, which is available via the Port C pins.
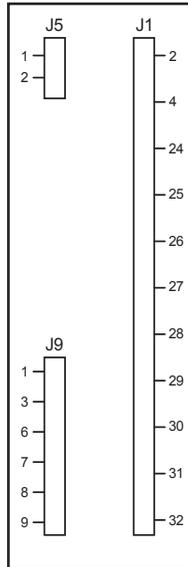
Figure 9. Embedded Modem Socket Interface—J1, J5, and J9

Table 10. Connector J5

Pin	Symbol	Description
1	M-TIP	Telephone Line Interface—TIP.
2	M-RING	Telephone Line Interface—RING.

Table 11. Connector J9

Pin	Symbol	Description
1	MRESET	Reset, active Low, 50–100 ms. Closure to GND for reset.
3	GND	Ground.

Table 11. Connector J9

6	D1	DCD indicator; can drive an LED anode without additional circuitry.
7	D2	RxD indicator; can drive an LED anode without additional circuitry.
8	D3	DTR indicator; can drive an LED anode without additional circuitry.
9	D4	TxD indicator; can drive an LED anode without additional circuitry.

Table 12. Connector J1

Pin	Symbol	Description
2	MOD_DIS	Modem disable, active Low.
4	V_{CC}	+5 VDC or +3.3 VDC input.
24	GND	Ground.
25	PC4_DTR1	DTR interface; TTL levels.
26	PC6_DCD1	DCD interface; TTL levels.
27	PC3_CTS1	CTS interface; TTL levels.
28	PC5_DSR1	DSR interface; TTL levels.
29	PC7_RI1	Ring Indicator interface; TTL levels.
30	PC0_TXD1	TxD interface; TTL levels.
31	PC1_RXD1	RxD interface; TTL levels.
32	PC2_RTS1	RTS interface; TTL levels.

Components P4, T1, C3, C4, and U11 provide the phone line interface to the modem. On the eZ80Acclaim!® Development Platform, LEDs D1, D2, D3, and D4 function as status indicators for this optional modem.

The phone line connection for the modem is for the United States only. Connecting the modem outside of the U.S. requires modification.

eZ80Acclaim!® Development Platform Memory

Memory space on the eZ80Acclaim!® Development Platform consists of onboard SRAM and additional footprints.

Onboard SRAM

The eZ80Acclaim!® Development Platform features 512KB SRAM at U20. This SRAM provides the basic memory requirement for small applications development. This SRAM is in the address range `B80000h–BFFFFFh`.

Additional SRAM

The amount of eZ80Acclaim!® Development Platform memory can be extended if required by adding SRAM devices. U19, U18, and U17 provide this capability. However, the user should be aware that additional SRAM must be installed in the following order:

1. U19, address range `B00000h–B7FFFFh`

2. U18, address range `A80000h–AFFFFFh`

3. U17, address range `A00000h–A7FFFFh`

If SRAM memory is installed in a different order than the above sequence, SRAM will not be contiguous unless the user is able to change the address decoder, U10. Memory access decoding is performed by this address decoder, implemented in the Generic Array Logic device, GAL22LV10D (U10).

Memory Map

A memory map of the eZ80® CPU is illustrated in Figure 10. Flash memory and SRAM on the eZ80190 Module are addressed when $\overline{CS0}$ and $\overline{CS1}$ are active Low. SRAM on the eZ80Acclaim!® Development Platform is addressed when $\overline{CS2}$ is active Low.

The eZ80190 MCU features 8 KB of internal SRAM in the address range E000h–FFFFh and 1 KB of MACC RAM in the address range DC00h–DFFFh. Internal RAM can be mapped anywhere in the 16 MB address space in 64 KB steps (DC00h–FFFFh to DC00h–FFFFFFh). The software included in the eZ80190 Development Kit assumes internal RAM in the range E000h–FFFFh for the interrupt vector table. This range overlaps the address range assigned to Flash memory ($\overline{CS0}$) on the eZ80190 Module.

> **Note:** The Ethernet controller, located on the eZ80190 Module, is mapped as an I/O device at address 300h. It uses $\overline{CS3}$.

```
┌─────────────────────────┐
│         FFFFFFh         │
│                         │
│                         │
│         DFFFFFh         │ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┐
│       SRAM Memory       │                           │
│        up to 2 MB       │                           } CS1
│         C7FFFFh         │  } Ethernet Module         │
│         C00000h         │    SRAM                    │
│         BFFFFFh         │  } Main Board       ─ ─ ─ ─┘
│         B80000h         │    SRAM (512 KB)          ┐
│  Expansion SRAM Memory  │                           │
│       up to 1.5 MB      │                           } CS2
│         80FFFFh         │                           │
│         800000h         │                           │
│         7FFFFFh         │ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┘
│     Expansion Module    │  } Up to 4 MB             ┐
│ Flash Memory up to 4 MB │                           │
│         400000h         │                           } CS0 (8 MB)
│         3FFFFFh         │ ─ ─ ─ ─ ─ ─ ─ ─           │
│                         │                           │
│       Flash Memory      │        } Up to 4 MB       │
│         0FFFFFh         │  } 1 MB on                 │
│         000000h         │    Ethernet Module ─ ─ ─ ─┘
└─────────────────────────┘
```
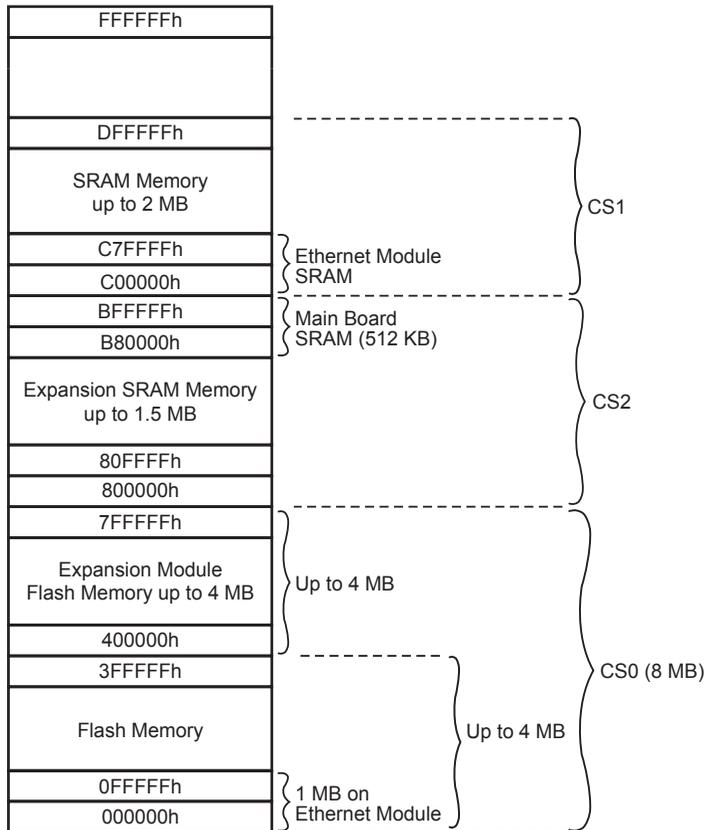
**Figure 10. Memory Map of the eZ80Acclaim!® Development Platform
and eZ80190 Module**

The LED matrix and the general-purpose port circuitry are mapped in the address range `800000h–80ffffh`. The $\overline{\text{CS2}}$ chip select should be driven Low to select the LED matrix or general-purpose port.

LEDs

As stated earlier, LEDs D1, D2, D3, and D4 function as status indicators for an optional modem. This section describes each LED and the LED matrix device.

Data Carrier Detect

The Data Carrier Detect (DCD) signal at D1 indicates that a good carrier signal is being received from the remote modem.

RX

The RX signal at D2 indicates that data is received from the modem.

Data Terminal Ready

The Data Terminal Ready (DTR) signal at D3 informs the modem that the PC is ready.

TX

The TX signal at D4 indicates that data is transmitted to the modem.

Push Buttons

The eZ80Acclaim!® Development Platform provides user controls in the form of push buttons. These push buttons serve as input devices to the eZ80® Ethernet Device device. The programmer can use them as necessary for application development. All push buttons are connected to the general-purpose port pins.

PB0

The PB0 push button switch, SW1, is connected to bit 0 of the general-purpose port. This switch can be used as the port input if required by the user.

PB1

The PB1 push button switch, SW2, is connected to bit 1 of the general-purpose port. This switch can be used as the port input if required by the user.

PB2

The PB2 push button switch, SW3, is connected to bit 2 of the general-purpose port. This switch can be used as the port input if required by the user.

RESET

The Reset push button switch, SW4, resets the eZ80® CPU and the eZ80Acclaim!® Development Platform.

Jumpers

The eZ80Acclaim!® Development Platform provides a number of jumpers that are used to enable or disable functionality on the platform, enable or disable optional features, or to provide protection from inadvertent use.

Jumper J2

The J2 jumper enables/disables IrDA transceiver functionality. When the shunt is placed, IrDA communication is disabled. This jumper does not perform any functions when the eZ80190 Module is installed.

z i l o g

Jumper J3

The J3 jumper connection controls the mode of the general-purpose port and communication with the 7x5 LED. When the shunt is placed, the general-purpose port is disabled. See Table 13.

Table 13. J3—DIS_EM

Shunt Status	Function	Affected Device
In	Application Module Hardware Disabled	Communication with 7x5 LED and Port emulation circuit is disabled.
Out	Application Module Hardware Enabled	Communication with 7x5 LED and the general-purpose port circuit is enabled.

Jumper J7

The J7 jumper connection controls Flash boot loader programming. When the shunt is placed, overwriting of the Flash boot loader program is enabled. See Table 14.

Table 14. J7—$\overline{\text{FlashWE}}$

Shunt Status	Function	Affected Device
Out	The Flash boot sector of the eZ80190 Module is write-protected.	Flash boot sector of the eZ80190 Module.
In	The Flash boot sector of the eZ80190 Module is enabled for writing or overwriting.	Flash boot sector of the eZ80190 Module.

Jumper J11

The J11 jumper connection controls access to the off-chip Flash memory device. When the shunt is placed, access to this Flash device is enabled. See Table 15.

▶ **Note:** The silk-screened label on the eZ80Acclaim!® Development Platform for jumper J11 is incorrect. Currently, it reads DIS_FLASH. The correct label is EN_FLASH.

Table 15. J11—EN_FLASH (Off-Chip)*

Shunt Status	Function	Affected Device
IN	All access to external Flash memory on the eZ80190 Module is enabled.	External Flash memory on the eZ80190 Module.
OUT	All access to external Flash memory on the eZ80190 Module is disabled.	External Flash memory on the eZ80190 Module.

Note: As shipped from the factory, external Flash memory is not installed.

Jumper J12

The J12 jumper connection controls the selection of a 5 V or 3 VDC power supply to the embedded modem, if an embedded modem is used. See Table 16.

Table 16. J12—5VDC/3.3VDC for an Embedded Modem

Shunt Status	Function	Affected Device
1–2	5 VDC is provided to power the embedded modem.	Embedded modem.
2–3	3.3 VDC is provided to power the embedded modem.	Embedded modem.

Jumper J14

The J14 jumper connection controls the polarity of the Ring Indicator. See Table 17.

Table 17. J14—RI

Shunt Status	Function	Affected Device
1–2	The Ring Indicator for UART1 is inverted.	UART1.
2–3	The Ring Indicator for UART1 is not inverted.	UART1.

For jumpers J15–J18, RS485 functionality is not available on the eZ80190 Module. However, this functionality is available in other eZ80® devices.

Jumper J15

The J15 jumper connection controls the selection RS485 circuit along with UART0. When the shunt is placed, the RS485 circuit is enabled. See Table 18. RS485 functionality will be available in future eZ80® devices.

Table 18. J15—RS485_1_EN*

Shunt Status	Function	Affected Device
In	The RS485 circuit is enabled on UART0. The UART0 CONSOLE interface and IrDA are disabled.	IrDA, UART0 CONSOLE interface, RS485 interface.
Out	The RS485 circuit is disabled on UART0.	IrDA, UART0 CONSOLE interface, RS485 interface.
Note: *To enable the RS485 circuit, the corresponding IrDA/RS232 circuit must be disabled.		

Jumper J16

The J16 jumper connection controls the selection of the RS485 circuit. However, UART1 MODEM interface and the socket modem interface are disabled if the RS485 circuit is enabled. When the shunt is placed, the RS485 circuit is enabled. See Table 19.

Table 19. J16—RS485_2_EN

Shunt Status	Function	Affected Device
In	The RS485 circuit is enabled on UART1. The UART1 MODEM interface and the Socket Modem interface are disabled.	UART1 MODEM interface, Socket Modem Interface, and RS485 interface.
Out	The RS485 circuit is disabled on UART1.	UART1 MODEM interface, Socket Modem Interface, and RS485 interface.

Jumper J17

The J17 jumper connection controls the selection of the RS485 termination resistor circuit. When the shunt is placed, the RS485 termination resistor circuit is enabled. See Table 20.

Table 20. J17—RT_1*

Shunt Status	Function	Affected Device
In	The Termination Resistor for RS485_1 is IN.	RS485 interface.
Out	The Termination Resistor for RS485_1 is OUT.	RS485 interface.

Note: *Before enabling the termination resistor, ensure that the device is located at the end of the interface line.

Jumper J18

The J18 jumper connection controls the selection of the RS485 termination resistor circuit. When the shunt is placed, the RS485 termination resistor circuit is enabled. See Table 21.

Table 21. J18—RT_2*

Shunt Status	Function	Affected Device
In	The Termination Resistor for RS485_2 is IN.	RS485 interface.
Out	The Termination Resistor for RS485_2 is OUT.	RS485 interface.

Note: *Before enabling the termination resistor, ensure that the device is located at the end of the interface line.

Jumper J19

The J19 jumper connection selects the range of memory addresses for the external chip select signal, $\overline{CS\_EX}$, to the application module. See Table 22.

Table 22. J19—$\overline{EX\_SEL}$

Shunt Status	Function	Affected Device
1–2	$\overline{CS\_EX}$ is decoded in the $\overline{CS0}$ memory space and is located in the address range 400000h–7FFFFFh.	Application module addressing.
3–4	$\overline{CS\_EX}$ is decoded in the $\overline{CS2}$ memory space and is located in the address range A00000h–A7FFFFh.	Application module addressing.
5–6	$\overline{CS\_EX}$ is decoded in the $\overline{CS2}$ memory space and is located in the address range A80000h–AFFFFFh.	Application module addressing.
7–8	$\overline{CS\_EX}$ is decoded in the $\overline{CS2}$ memory space and is located in the address range B00000h–B7FFFFh.	Application module addressing.

Jumper J20

The J20 jumper connection controls the selection of the external chip select in the external application module. When the shunt is placed, the external chip select signal, $\overline{\text{CS\_EX}}$, is disabled. See Table 23.

Table 23. J20—$\overline{\text{EX\_FL\_DIS}}$

Shunt Status	Function	Affected Device
IN	The jumper for EX_FL_DIS is IN.	The chip select on the application module is disabled.
OUT	The jumper for EX_FL_DIS is OUT.	The chip select on the application module is enabled.

Connectors

A number of connectors are available for connecting external devices such as the ZPAK II emulator, PC serial ports, external modems, the console, and LAN/telephone lines.

J6 and J8 are the headers, or connectors, that provide pin-outs to connect any external application module, such as ZiLOG's Thermostat Application Module.

Connector J6

The J6 connector provides pin-outs to make use of GPIO functionality.

Connector J8

The J8 connector provides pin-outs to access memory and other control signals.

Console

Connector P2 is the RS232 terminal, which can be used for observing the console output. P2 can be connected to a PC running a HyperTerminal program if required.

Modem

Connector P3 provides a terminal for connecting an external modem, if used with the eZ80190 Development Kit.

I²C Devices

The two I²C devices on the eZ80Acclaim!® Development Platform are the U2 EEPROM and the U13 Configuration register. The EEPROM provides 16KB of memory. The Configuration register provides access to control the configuration of an application-specific function at the Application Module Interface. Neither device is utilized by the eZ80190 Development Kit software. The user is free to develop proprietary software for these two devices. The addresses for accessing these devices are listed in Table 24.

Table 24. I²C Addresses

Device/Bit #	7	6	5	4	3	2	1	0
EEPROM (U10)*	1	0	1	0	0	A1	A0	R/W
Configuration Register (U13)	1	0	0	1	1	1	0	R/W
Note: *EEPROM address bits A0 and A1 are configured for 0s.								

DC Characteristics

Understanding proper DC current requirements for the eZ80Acclaim!® Development Platform when application modules are plugged into it is

very important for developing applications. This section provides an estimate of the average current requirement when different combinations of these application modules are plugged in to the eZ80Acclaim!® Development Platform.

The measurements of current that are shown in Table 25 are for the user's reference. These values can vary depending on the type of application that is developed to run with the platform.

Table 25. DC Current Characteristics of the
eZ80Acclaim!® Development Platform with Different Module Loads

Platform/Modules Configurations	Current Requirement (mA)	Status
eZ80Acclaim!® Development Platform and eZ80190 Module	173	When connected only to a power supply, and when no program is running.
eZ80Acclaim!® Development Platform, eZ80190 Module, and Modem Module	174	When connected only to a power supply, and when no program is running.
eZ80Acclaim!® Development Platform, eZ80190 Module, and Thermostat Application Module	195	When connected only to a power supply, and when no program is running.
eZ80Acclaim!® Development Platform, eZ80190 Module, Modem Module, and Thermostat Application Module	203	When connected only to a power supply, and when no program is running.
eZ80Acclaim!® Development Platform and eZ80190 Module	325	When the LED demo is running.
eZ80Acclaim!® Development Platform, eZ80190 Module, and Modem Module	325	When the LED demo is running.

Table 25. DC Current Characteristics of the
eZ80Acclaim![®] **Development Platform with Different Module Loads (Continued)**

Platform/Modules Configurations	Current Requirement (mA)	Status
eZ80Acclaim!® Development Platform, eZ80190 Module, and Thermostat Application Module	350	When the LED demo is running.
eZ80Acclaim!® Development Platform, eZ80190 Module, Modem Module, and Thermostat Application Module	360	When the LED demo is running.

eZ80190 Module

This section describes the eZ80190 Module hardware, its interfaces and key components, including the CPU, Ethernet Media Access Controller (EMAC), and memory.

Functional Description

The eZ80190 Module is a compact, high-performance Ethernet module specially designed for the rapid development and deployment of embedded systems requiring control and Internet/Intranet connectivity via Ethernet and/or fast Multiply-Accumulate operations. Additional devices such as serial ports, LED matrices, GPIO ports, and I^2C devices are supported when connected to the eZ80Acclaim!® Development Platform. A block diagram representing both of these boards is shown in

The eZ80190 Module is developed to be a plug-in module to the eZ80® Development Platform. The small-footprint eZ80190 Module provides a CPU, SRAM, Flash memory, a real-time clock, and an EMAC. This low-cost, expandable module is powered by the eZ80190 microprocessor, a member of ZILOG's new eZ80® product family. The module also contains a battery and an oscillator in support of the onboard Real-Time Clock (RTC). The eZ80190 Module can also be used as a stand-alone development tool when provided with an external power source.

Physical Dimensions

The footprint of the eZ80190 Module PCB is 63.5 mm x 78.7 mm. With an RJ-45 Ethernet connector, the overall height is 25 mm. See Figure 11.
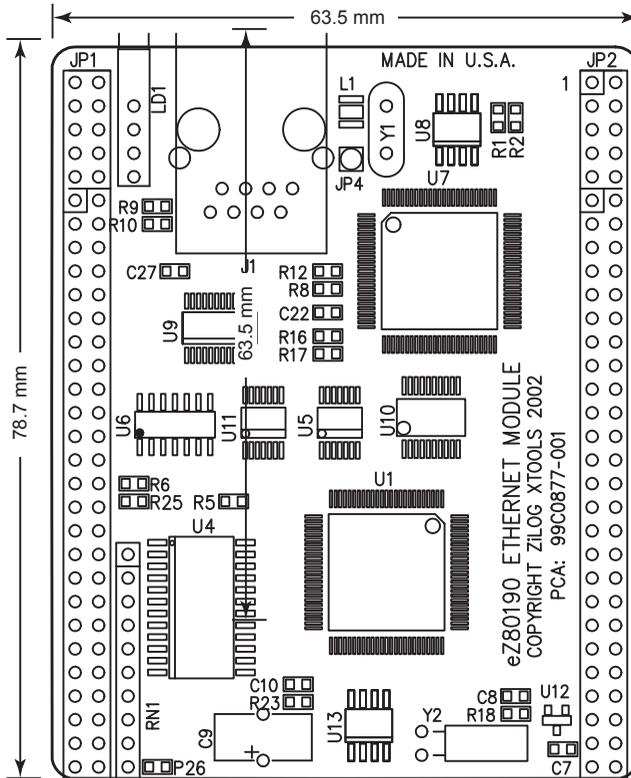
Figure 11. Physical Dimensions of the eZ80190 Module

Figure 12 illustrates the top layer silkscreen of the eZ80190 Module.
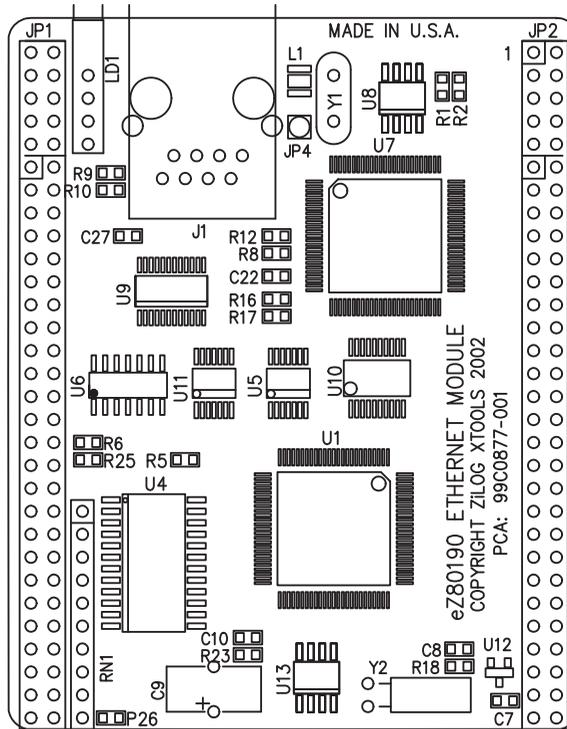
Figure 12. eZ80190 Module—Top Layer

Figure 13 illustrates the bottom layer silkscreen of the eZ80190 Module.
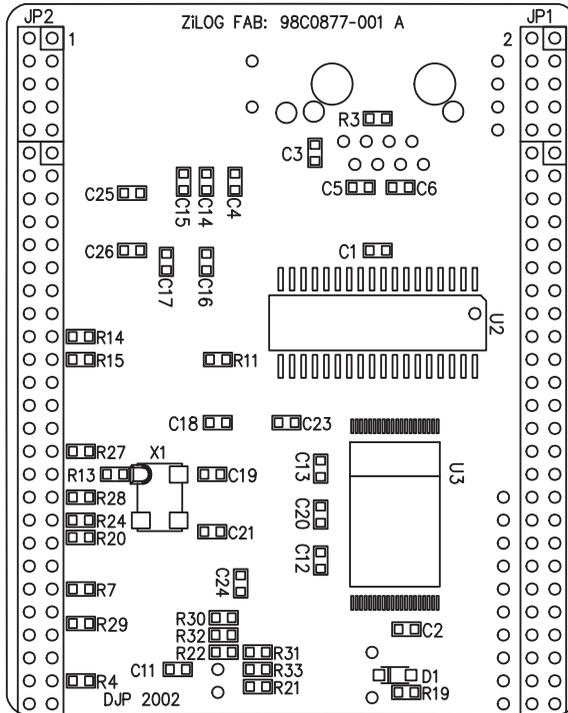
Figure 13. eZ80190 Module—Bottom Layer

Operational Description

The purpose of the eZ80190 Module as a feature of the eZ80190 Development Kit is to provide the application developer with a plug-in tool to evaluate memory and the other features of the eZ80190 device.

Ethernet Media Access Controller

The eZ80190 Module contains a CS8900A Ethernet Media Access Controller (EMAC—combines MAC and PHY functions) which is attached to the data/address bus (A0–A3, D0–D7, $\overline{\text{RD}}$, and $\overline{\text{WR}}$) of the processor. This chip is connected to the processor's $\overline{\text{CS3}}$ Chip Select, and to the PD4 pins for interrupt purposes. Connection of pins PD6 and PD7 for LANACT (wake-up from sleep) and SLEEP is optional and resistor-selectable onboard (see below). Details about the internal registers of the CS8900A EMAC can be found on the Cirrus Logic website at www.cirrus.com.

Ethernet LEDs

There are two green LEDs, a Link LED and a LAN LED, that are located adjacent to each other on the eZ80190 Module. A steady LAN LED (top) indicates received link pulses from the Ethernet. A flashing Link LED (bottom) indicates Traffic (RX or TX) on the LAN.

Ethernet Connector

The eZ80190 Module is equipped with an RJ-45 connector that features integrated magnetics (transformer, common mode chokes). The remaining pins on the onboard RJ-45 connector are not connected.

An RJ-45 loopback connector can be used to verify the correct operation of the Receiver and the Transmitter. Pin assignments for the RJ-45 Ethernet connector are shown in Table 26.

Table 26. Ethernet Connector Pin Assignments

Pin	Function
1	TX+
2	TX–
3	RX+
6	RX–

To connect the eZ80190 Module directly to another host (e.g., to a personal computer), a crossover cable must be used.

The EMAC can be additionally protected by placing an ESD protection array on the module at U8. This array can be either of the LCDA15C-6 (Semtech) or ESDA25B1 (ST Microelectronics) devices.

GPIO Pins for Enabling LAN Activity, Sleep, Interrupt

GPIO input bit PD4 serves as an active High interrupt input for the EMAC's INTRQ0 output.

GPIO output bit PD7 can be used to place the EMAC into SLEEP mode. When pulling SLEEP (PD7) Low after enabling HWStandbyE and HWSleepE modes, the chip draws lower current, because only the receiver is operating. A zero-Ohm resistor at position R14 on the eZ80190 Development Kit is required for this function.

If LAN activity is detected, the LANACT signal is pulled Low. The LANACT is connected to GPIO input PD6 and can be used in interrupt edge-detection mode to wake up and reinitialize the Ethernet chip. A zero-Ohm resistor at position R15 on the module is required for this function. In this case, the PD6 pin is not available for GPIO on the I/O connector.

EMAC Access

$\overline{CS3}$ is used for selecting the Ethernet MAC. For 50 MHz operation, set the CS3_CTL register (I/O address B3h) to F8h (7 wait states for I/O). The EMAC requires –IOR to be active for 135 ns and –IOW to be active for 110 ns.

To satisfy proper setup times at 50 MHz, –IOR is delayed by one clock cycle and –IOW is delayed by two clock cycles when $\overline{CS3}$ goes active. To satisfy proper hold times at 50 MHz, the EMAC address and data are latched when $\overline{CS3}$ goes inactive.

eZ80190 Module Memory

The eZ80190 Module contains 512 KB SRAM and 1 MB Flash memory. This addressing structure provides 1.5 MB of contiguous RAM for immediate use.

SRAM Memory

The eZ80190 Module features 512 KB of fast SRAM. Access speed is typically 12 ns or faster, allowing zero-wait-state operation at 50 MHz. With the CPU at 50 MHz, onboard SRAM can be accessed with zero wait states. CS1_CTL (chip select $\overline{CS1}$) is set to 08h (no wait states).

Flash Memory

The Flash Boot Loader, application code, and user configuration data are held permanently in Flash memory.

Internal RAM

The eZ80190 MCU features 8 KB of zero-wait-state internal SRAM. This internal RAM can be mapped anywhere in the 16 MB address space in the address range E000h–FFFFh.

Reset Generator

The onboard Reset Generator Chip is connected to the eZ80190 Reset input pin. It performs reliable Power-On Reset functions, generating a reset pulse with a duration of 200 ms if the power supply drops below 2.93 V. This reset pulse ensures that the board always starts in a defined condition. The RESET pin on the I/O connector reflects the status of the RESET line. It is a bidirectional pin for resetting external peripheral components or for resetting the eZ80190 Development Kit with a low-impedance output (e.g. a 100-Ohm push button).

Real Time Clock

The onboard real-time clock can function when the system power supply is down. An onboard capacitor (GoldCap) or external accumulator/battery serves as a standby power supply. The M41T11 Real-Time-Clock included on the eZ80190 Module contains Binary Coded Decimal (BCD) counting registers for Seconds, Minutes, Hours, Day, Month, Year; it also contains a Century bit and 56 bytes of backed-up RAM. The fully-charged 0.1 F GoldCap bridges power outages with a maximum of 4 hours. The GoldCap, in contrast to a battery or an accumulator, offers an advantage in that service/replacement is not necessary.

The I^2C address of the RTC is D0h for Writes and D1h for Reads.

Details about the internal registers of the M41T11 Real-Time clock can be found on the ST Microelectronics website (www.st.com).

I^2C Bus Software Emulation

The eZ80190 device contains two powerful master/slave mode I^2C bus controllers. The I^2C data (SDA) and clock (SCL) pins on PD1/PD0 and PC1/PC0 GPIO are multiplexed with the UART and SPI functions. To use I^2C bus operation in parallel with console and modem I/O, the module IICSCL/IICSDA pins on connector JP2 can be linked to PA7 (IICSDA) and PA6 (IICSCL) of the eZ80190 device. In this case, an I^2C master-mode software emulation is necessary to access I^2C devices.

Using PA7/PA6 or PC1/PC0 for IICSDA/IICSCL is resistor-selectable on the eZ80190 Module.

DC Characteristics

As different combinations of application modules are loaded onto the eZ80Acclaim!® Development Platform, current requirements change. Please see to reference current consumption values for these different modules.

Flash Loader Utility

The Flash Loader utility resides in the boot sector of Flash memory, located on the eZ80190 Module. The Flash Loader utility allows the user to program application code into Flash memory.

Please refer to the *External Flash Loader Product User Guide* (PUG0012) for more details.

Mounting the Module

When mounting the eZ80190 Module onto the eZ80Acclaim!® Development Platform, check its orientation to the platform to ensure a correct fit. Pin 11 of JP1 on the eZ80190 Module must align with pin 1 of JP1 on the eZ80Acclaim!® Development Platform; Pin 11 of JP2 on the eZ80190 Module must align with pin 1 of JP2 on the eZ80Acclaim!® Development Platform, etc.

Changing the Power Supply Plug

The universal 9VDC power supply offers three different plug configurations and a tool that aids in removing one plug configuration to insert another, as shown in Figure 14.
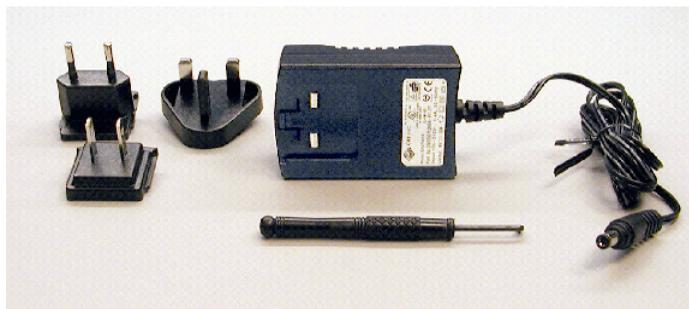
Figure 14. 9VDC Universal Power Supply Components

To exchange one plug configuration for another, perform the following steps:

1. Place the tip of the removal tool into the round hole at the top of the current plug configuration.

2. Press down to disengage the keeper tab and push the plug configuration out of its slot.

3. Select the plug configuration appropriate for your location, and insert it into the slot formerly occupied by the previous plug configuration.

4. Push the new plug configuration down until it snaps into place, as indicated in Figure 15.
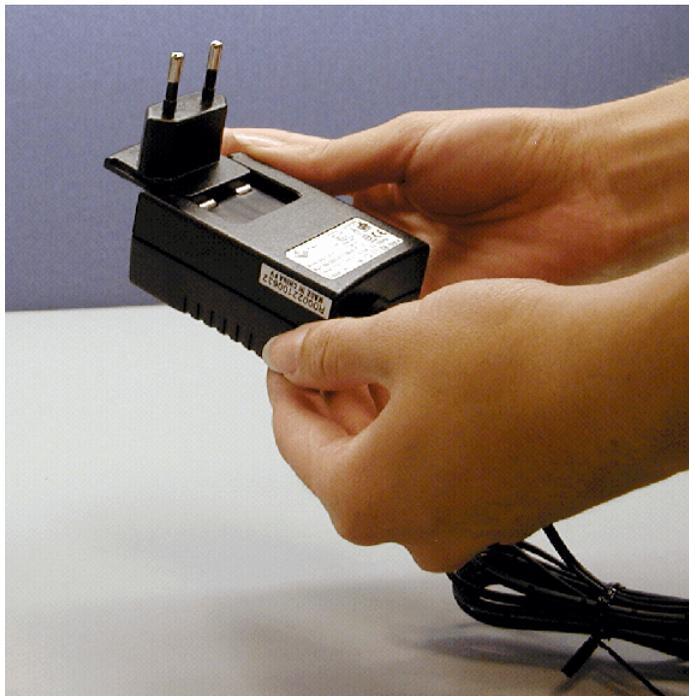
Figure 15. Inserting a New Plug Configuration

ZPAK II

ZPAK II is a debug tool used to develop and debug hardware and software. It is a networked device featuring an Ethernet interface and an RS232 console port. ZPAK II is shipped with a preconfigured IP address that can be changed to suit the user on a local network. For more information about using and configuring ZPAK II, please refer to the *ZPAK II Debug Interface Tool Product User Guide* (PUG0015) and the *eZ80190 Development Kit Quick Start Guide* (QS0004).

ZDI Target Interface Module

The ZDI Target Interface Module provides a physical interface between ZPAK II and the eZ80Acclaim!® Development Platform. The TIM module supports ZDI functions. For more information on using the TIM module or ZDI please refer to the *eZ80190 Development Kit Quick Start Guide* (QS0004) and the *eZ80190 Module Product Specification* (PS0191).

JTAG

Connector P1 is the JTAG connector on the eZ80Acclaim!® Development Platform. JTAG will be supported in the next offering of eZ80® products.

Application Modules

ZiLOG offers the Thermostat Application module, which can be used for evaluating and developing process control and simple I/O applications. The Thermostat Application module is equipped with an LCD display that can be used to display process control and other physical parameters. For additional reading about the Thermostat application, please see the *Java Thermostat Demo Application Note* (AN0104) on zilog.com.

ZDS II

ZiLOG Developer Studio II (ZDS II) Integrated Development Environment is a complete stand-alone system that provides a state-of-the-art development environment. Based on the Windows® Win 98SE/Win2000-SP4/WinXP Professional user interfaces, ZDS II integrates a language-sensitive editor, project manager, C-Compiler, assembler, linker, librarian, and source-level symbolic debugger that supports the eZ80® CPU. For more information about using and configuring ZDS II, please refer to the *ZiLOG Developer Studio II—eZ80Acclaim! User Manual* (UM0144).

Troubleshooting

Overview

Before contacting ZiLOG Customer Support to submit a problem report, please follow these simple steps. If a hardware failure is suspected, contact a local ZiLOG representative for assistance.

Cannot Download Code

If you are unable to download code to RAM using ZDS, make sure to press and release the Reset button on the eZ80Acclaim!® Development Platform prior to selecting **Debug** → **Reset** and then **Debug** → **Go** in ZDS.

No Output on Console Port

The eZ80190 Development Kit is shipped with a Flash Loader utility that is loaded in the protected boot sector of Flash memory (U3). Upon power-up of the eZ80Acclaim!® Development Platform and the eZ80 Web-server-i E-NET Module, the eZ80190 device on the module starts running code from this Flash memory area. This code enables the Console port with settings of 57.6kbps, 8, N, 1.

The Console checks the Receive buffer. If a *space* character is received on the Console port, the Flash Loader utility is enabled and a boot message should be displayed on your connected device. If no message is displayed, check the following:

- Jumper J2 must be ON (IrDA is disabled)

- On Connector J6, the jumper must be removed from pins 6 and 9 (pin names *con_dis* and *GND*).

IrDA Port Not Working

If you plan on using the IrDA transceiver on the eZ80 Webserver-i E-NET Module, make sure the hardware is set up as follows:

- Jumper J2 must be OFF (to enable the control gate that drives the IrDA device)

- Set port pin PD2 Low. When this port pin and Jumper J2 are turned OFF, the IrDA device is enabled.

- Install a jumper on connector J6 across pin names *con_dis* and *GND* to disable the console serial port driver

Difference Between EMAC and IP Address

Media Access Control (MAC)

Each and every Ethernet device interface to the network media (e.g., network adapter, port on a hub) contains a unique MAC address, which is hard-coded into the hardware when it is manufactured. An Ethernet device addresses a host using a unique 48-bit address called its Ethernet address or Media Access Control (MAC) address.

MAC addresses are usually represented as six colon-separated pairs of hex digits, e.g., 6:0:20:11:ac: 85. The first three bytes (e.g., 6-0-20) are the manufacturer's code, which can be used to identify the manufacturer. The last three bytes are the unique station ID or serial number for the interface. This station ID is unique and is associated with a particular Ethernet device. The Data Link layer's protocol-specific header specifies the MAC address of the packet's source and destination. When a packet is sent to all hosts (broadcast), a special MAC address (ff:ff:ff:ff:ff:ff) is used.

MAC addresses uniquely identify each node in a network at the Media Access Control layer, the lowest network layer that directly interfaces with the physical media (e.g., twisted-pair wires).

On a Local Area Network or other network, the MAC address is the computer's unique hardware number. (On an Ethernet LAN, the MAC address is the same as an Ethernet address.) When it is connected to the Internet, a computer (or *host* as the Internet protocol considers it), a correspondence table relates the Internet Protocol (IP) address to the computer's physical (MAC) address on the LAN.

IP Address

An IP address is a 32-bit number that identifies each sender or receiver of information that is sent in packets across the Internet.

An IP address contains two parts: the identifier of a particular network on the Internet, and an identifier of the particular device (which can be a server or a workstation) within that network. On the Internet itself—that is, between the router that moves packets from one point to another along the route—only the network part of the address is examined.

Relationship of the IP Address to the Physical Address

The machine or physical address used within an organization's local area networks can be different than the IP address coming from the Internet. The most typical example is the 48-bit Ethernet address. TCP/IP includes the Address Resolution Protocol (ARP) that lets the administrator create a table that maps IP addresses to physical addresses.

The Ethernet MAC address of the ZPAK II

When connecting the ZPAK II serial port to a PC running HyperTerminal, hold the space bar and reset the ZPAK II.

When HyperTerminal prompts with

```
eZ80>
```

enter e to display the MAC address.

Resolving IP Address/Subnet Mask Conflicts

For running demos properly. the ZPAK II IP address and subnet mask must be properly configured. Please follow the instructions provided in the *eZ80190 Development Kit Quick Start Guide* (QS0004) to set up and run the demos on ZDS II.

Schematic Diagrams

eZ80® Development Platform

Figures 16 through 20 present the schematics of the eZ80® Development Platform.
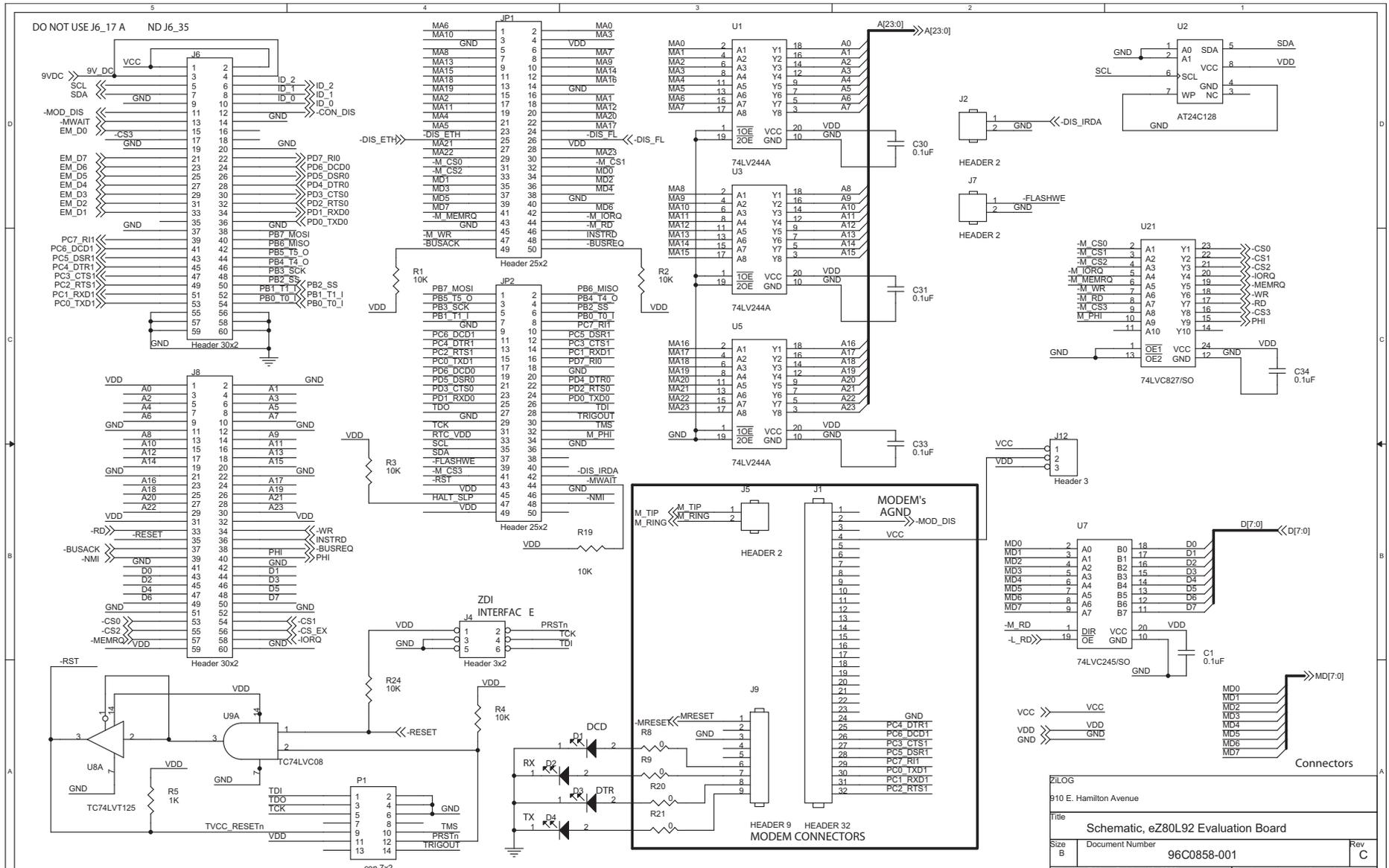
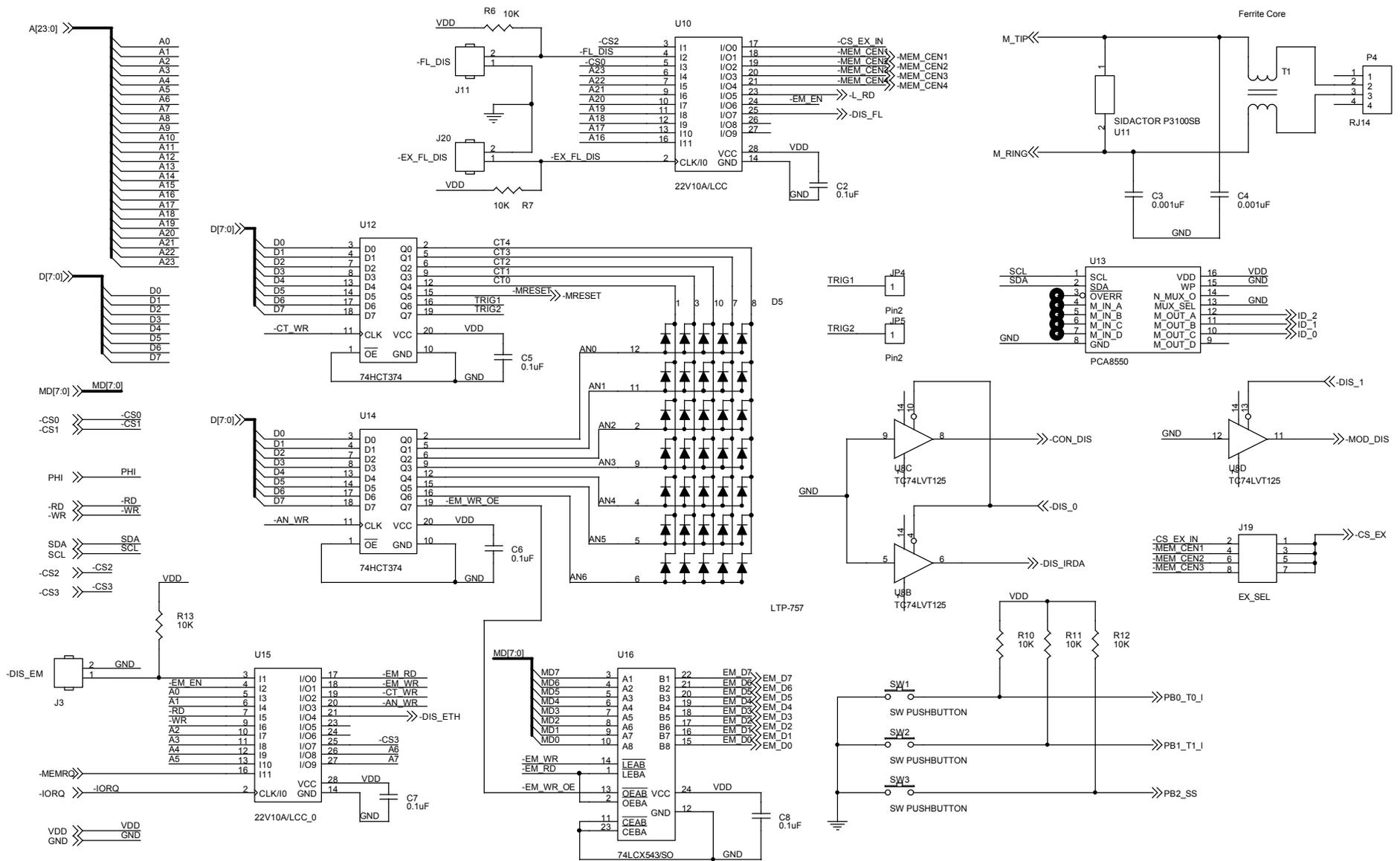
Figure 16. eZ80® Development Platform Schematic Diagram, #1 of 5

Figure 17. eZ80® Development Platform Schematic Diagram, #2 of 5
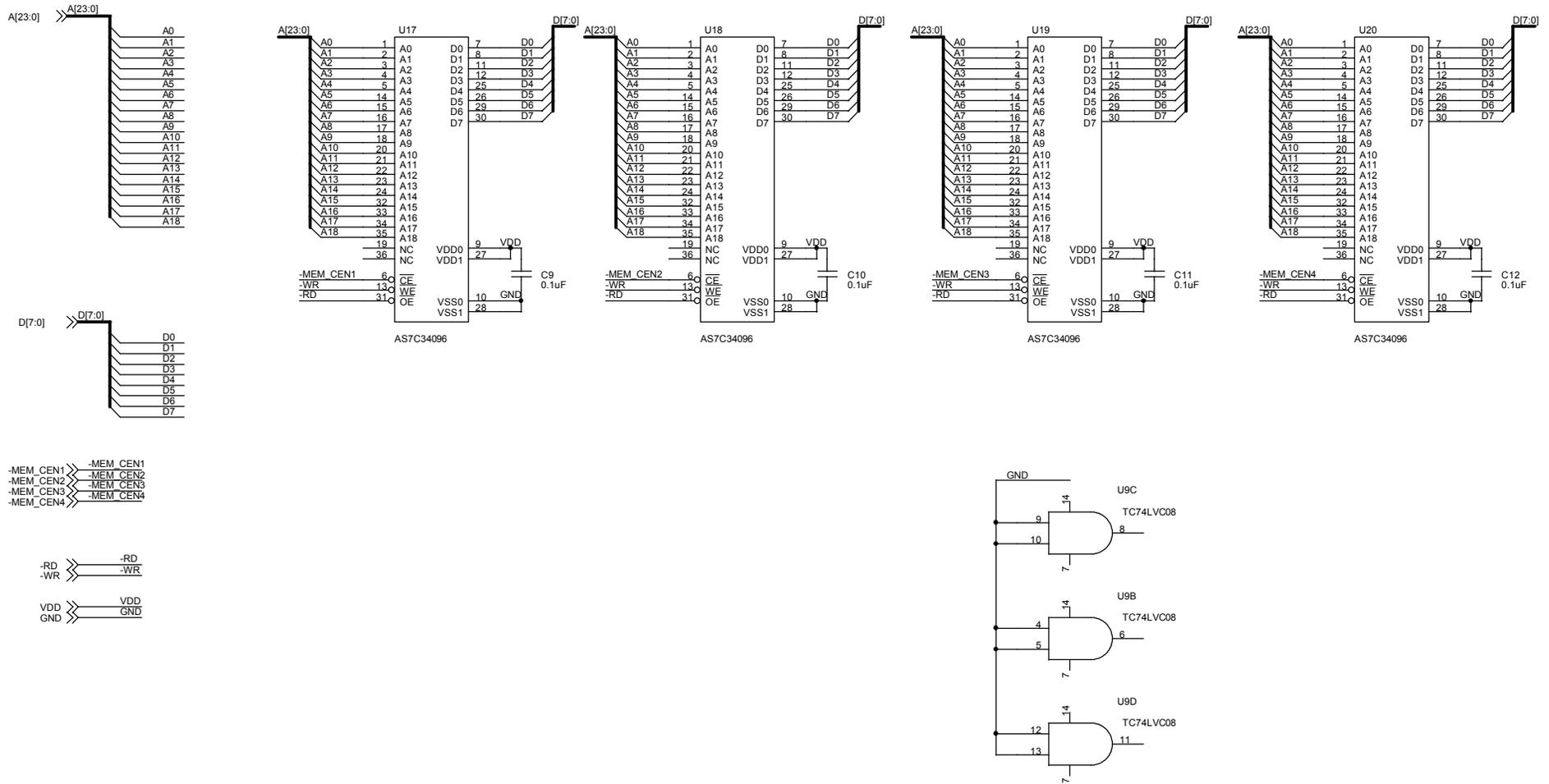
Figure 18. eZ80® Development Platform Schematic Diagram, #3 of 5
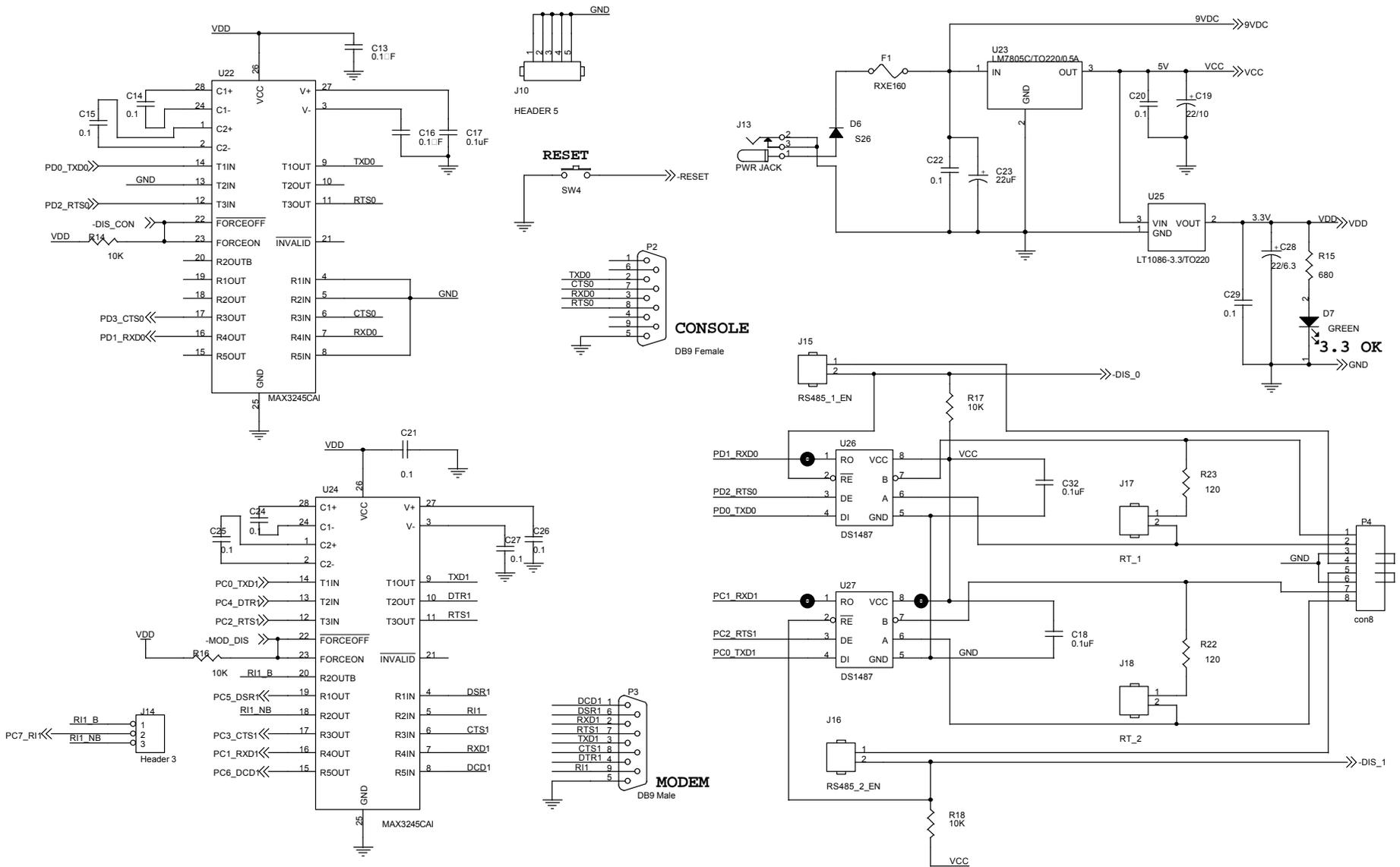
Figure 19. eZ80® Development Platform Schematic Diagram, #4 of 5

MATES WITH AMP = 749268-1
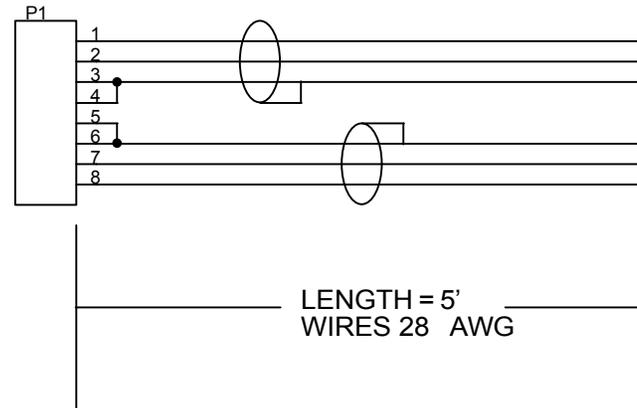
Figure 20. eZ80® Development Platform Schematic Diagram, #5 of 5—RS-485 Cable

eZ80190 Module

Figures 21 through 28 present the schematics of the eZ80190 Module.

ETHIRQ   ETHIRQ   =   PD4
-SLEEP   -SLEEP   PD7
-ACTIVE   -ACTIVE   PD6

0R 0603 R14
0R 0603 R15
don't stuff

X1
OUT   OE
3   1
R13
4k7 0603
50.000MHz, 3.3V
SG-710

PA[0..7]   XIN
PD[0..7]
CLK_OUT
PA[0..7]   PA[0..7]

-WR   -WR
-RD   -RD
-CS[0..3]   -CS[0..3]

-CS0 --> FLASH
-CS1 --> RAM
-CS2 --> ext. IO
-CS3 --> ETH

-MREQ   1
-WR   2
-RD   3
-CS0   4
-CS1   5
-CS2   6
-CS3   7
8
9
A0   10
A1   11
A2   12
A3   13
A4   14
A5   15
A6   16
A7   17
18
19
A8   20
A9   21
A10   22
A11   23
A12   24
A13   25

D[0..7]   D[0..7]
A[0..23]   A[0..23]

-BUSREQ   -BUSREQ
-BUSACK   -BUSACK
-MREQ   -MREQ
CLK_OUT   CLK_OUT

U1
eZ80190
TQFP100

MREQ
WR
RD
CS0
CS1
CS2
CS3
VDD
VSS
A0
A1
A2
A3
A4
A5
A6
A7
VDD
VSS
A8
A9
A10
A11
A12
A13

TEST
PC7/RI1
PC6/DCD1
PC5/DSR1
PC4/DTR1
PC3/SS1/CTS1
PC2/SCK1/RTS1
PC1/SDA1/MOSI1/RxD1
PC0/SCL1/MISO1/TxD1
VSS
VDD
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
ZDA
ZCL
RESET
IORQ
INSTRD
HALT

75 PC7
74 PC6
73 PC5
72 PC4
71 PC3
70 PC2
69 PC1
68 PC0
67
66
65 PB7
64 PB6
63 PB5
62 PB4
61 PB3
60 PB2
59 PB1
58 PB0
57
56 ZDA
55 ZCL
54 -RESET
53 -IOREQ
52 -INSTRD
51 -HALT

PC[0..7]
PB[0..7]   PB[0..7]
PC[0..7]   PC[0..7]
PD[0..7]   PD[0..7]
ZDA   ZDA
ZCL   ZCL
PB[0..7]

A14   26
A15   27
VDD   28
VSS   29
A16   30
A17   31
A18   32
A19   33
A20   34
A21   35
A22   36
A23   37
VDD   38
VSS   39
D0   40
D1   41
D2   42
D3   43
D4   44
D5   45
D6   46
D7   47
VDD   48
VSS   49
NMI   50

A[0..23]
D[0..7]

-RESET   -RESET
-IOREQ   -IOREQ
-INSTRD   -INSTRD
-HALT   -HALT
-NMI   -NMI

R4 1k 0603
-NMI

PC1   PC0
don't stuff
R30 0R 0603
R31 0R 0603

IICSDA   IICSDA   PA7
IICSCL   IICSCL   PA6
0R 0603 R32
0R 0603 R33

C18 1nF 0603
C19 1nF 0603
C20 1nF 0603
place caps close
to pins 97, 8, 38, 48

Figure 21. eZ80190 Module Schematic Diagram, #1 of 8—CPU
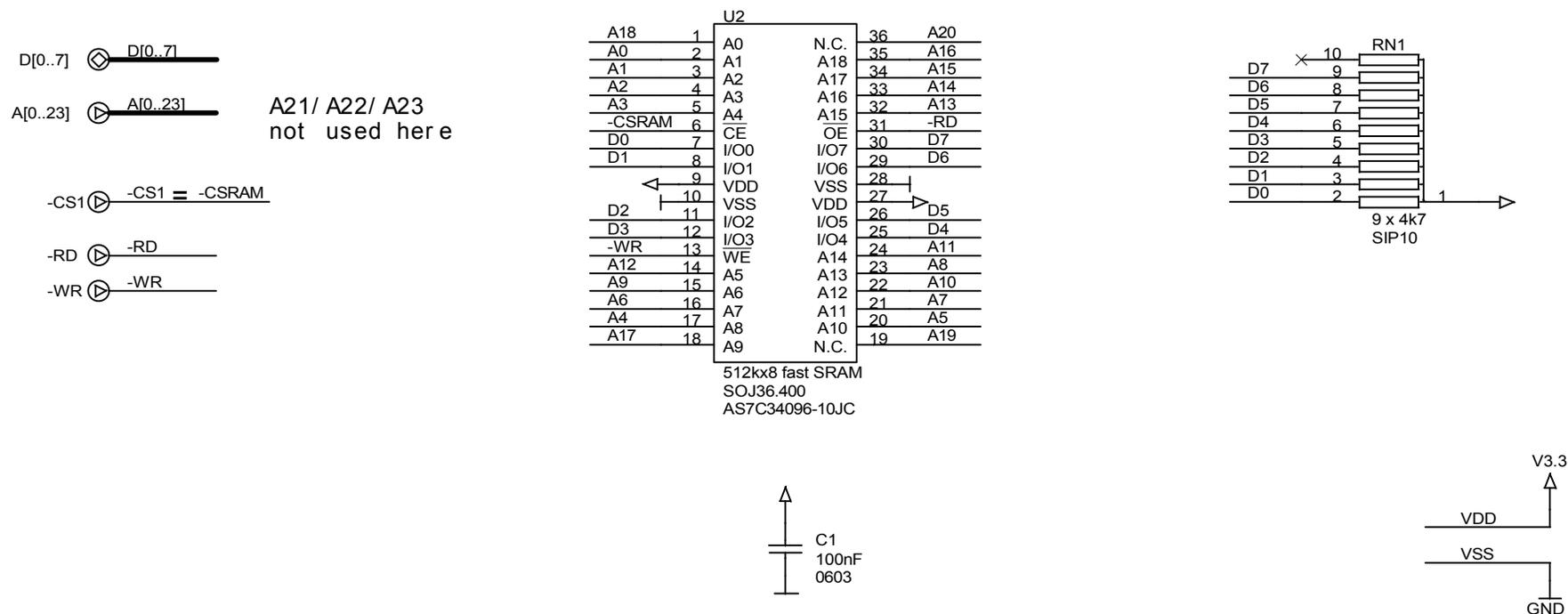
Figure 22. eZ80190 Module Schematic Diagram, #2 of 8—36-Pin SRAM Device

Figure 23. eZ80190 Module Schematic Diagram, #3 of 8—NOR Flash Device
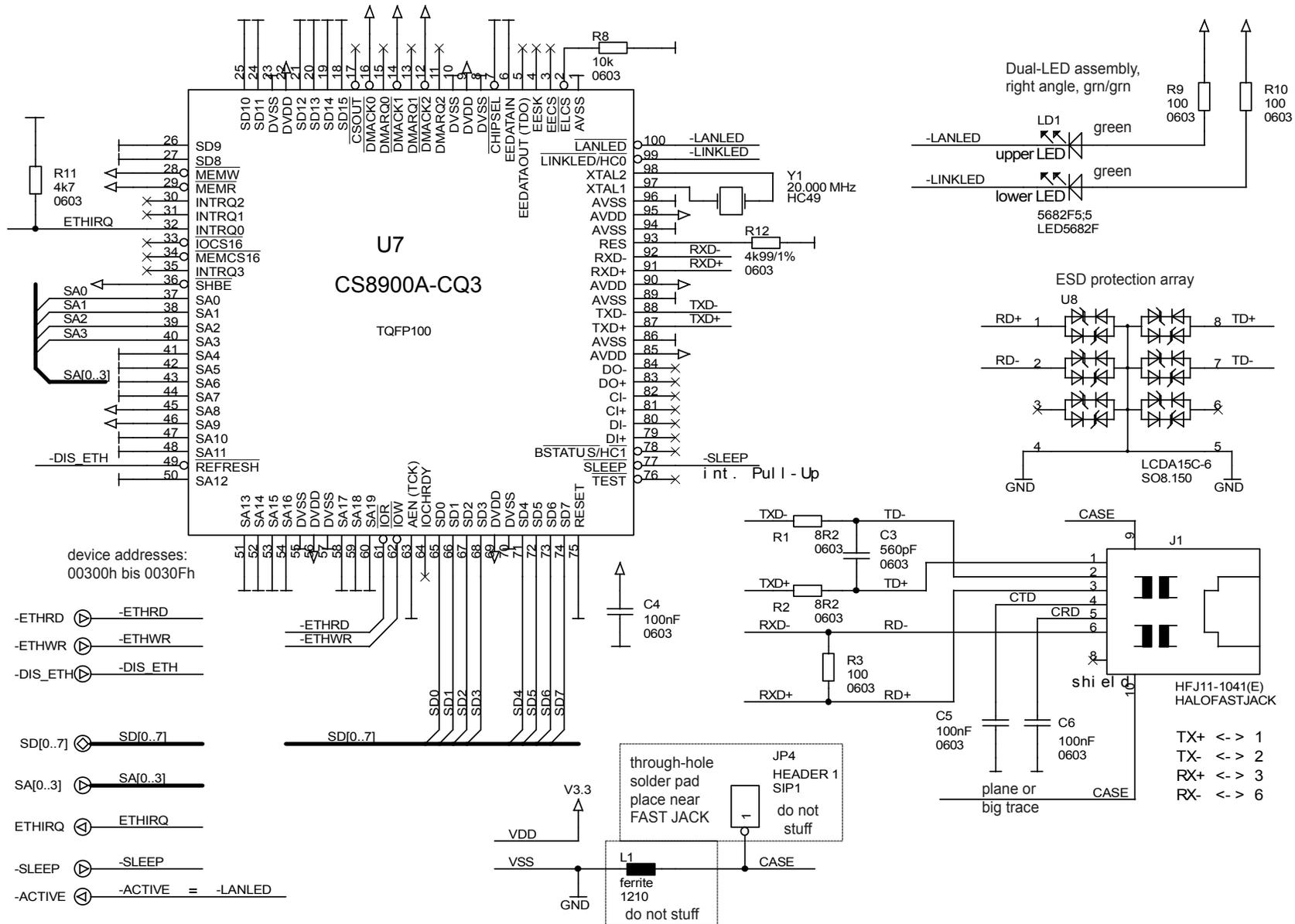
Figure 24. eZ80190 Module Schematic Diagram, #4 of 8—Ethernet Module
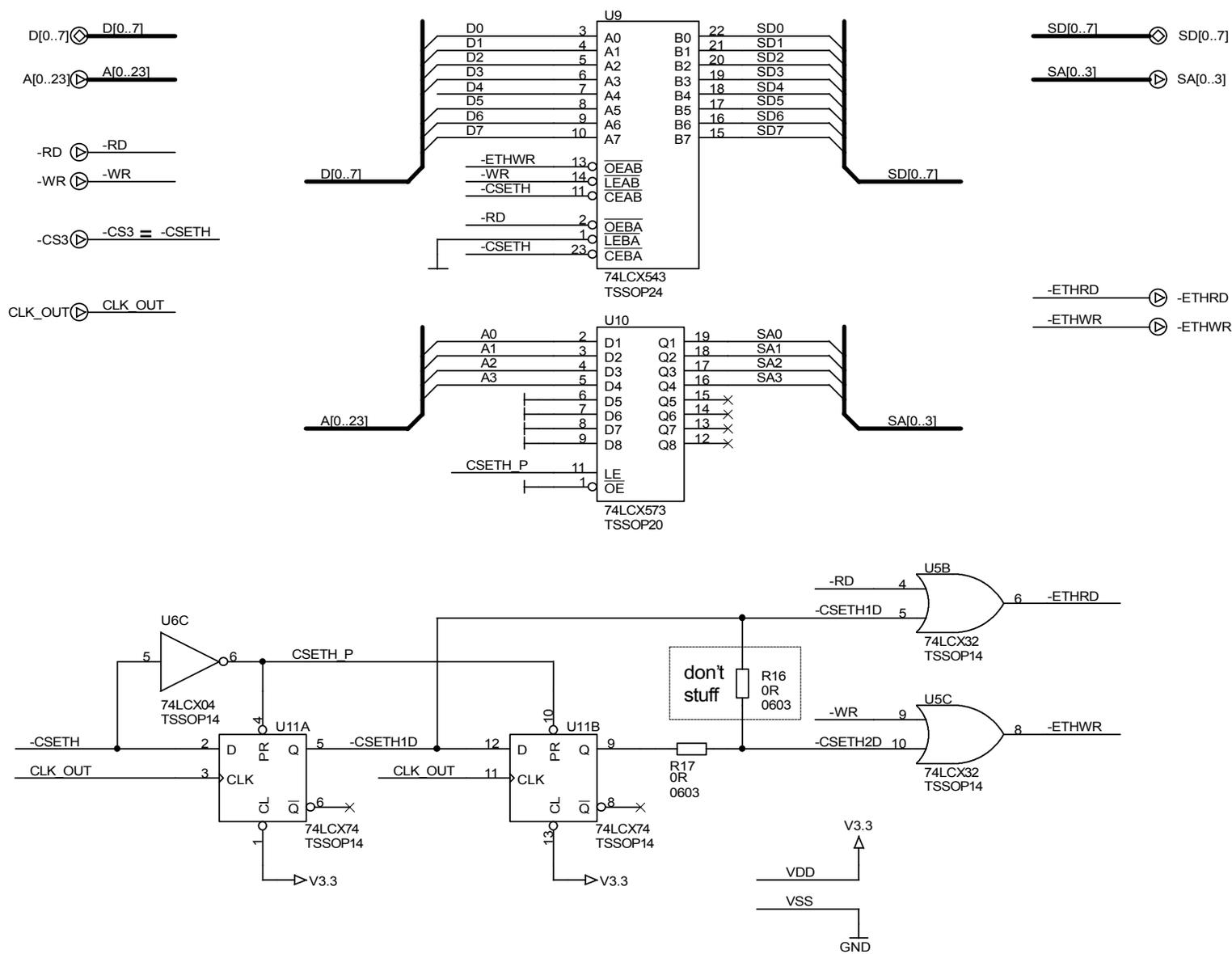
Figure 25. eZ80190 Module Schematic Diagram, #5 of 8—Ethernet Module Logic

power supervisor
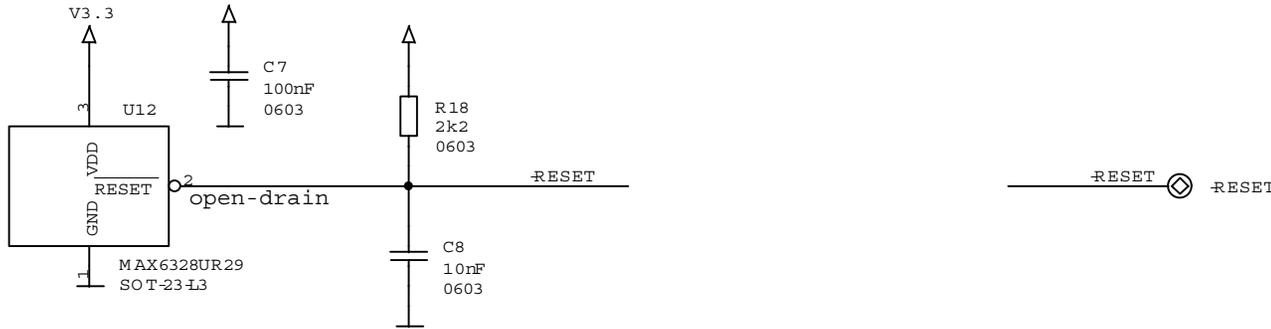
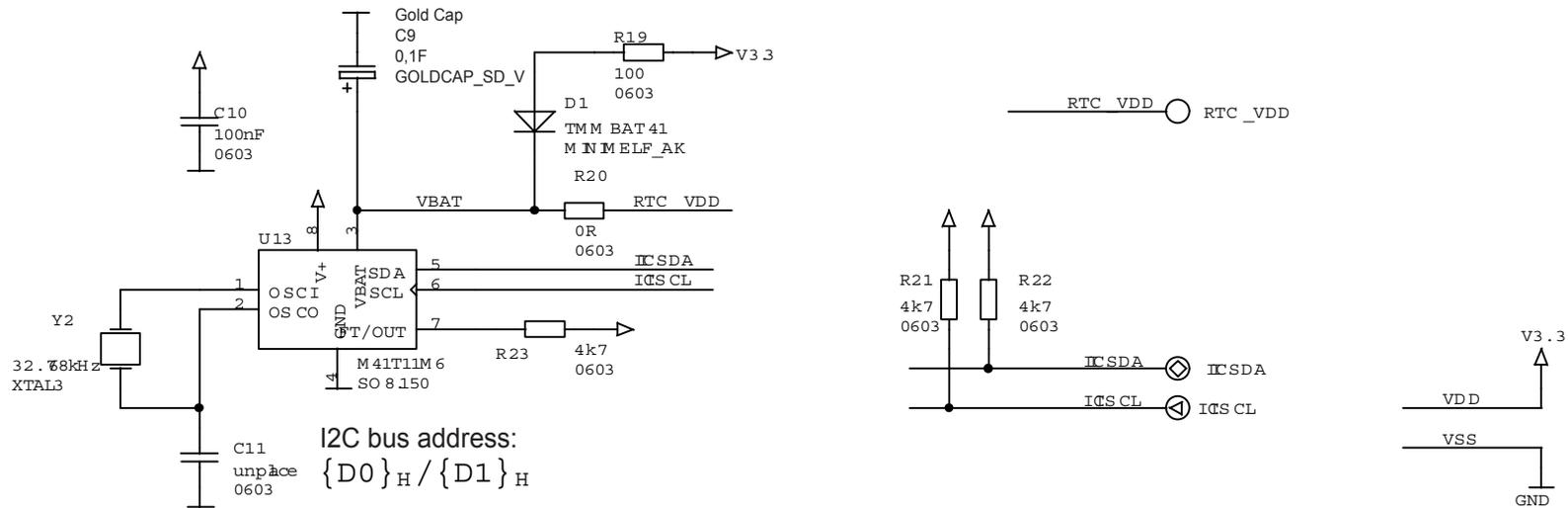
alternative:
Maxim MAX6802UR29D3

real-time clock

I2C bus address:
${D0}_H / {D1}_H$

Figure 26. eZ80190 Module Schematic Diagram, #6 of 8—Ethernet Module Peripherals
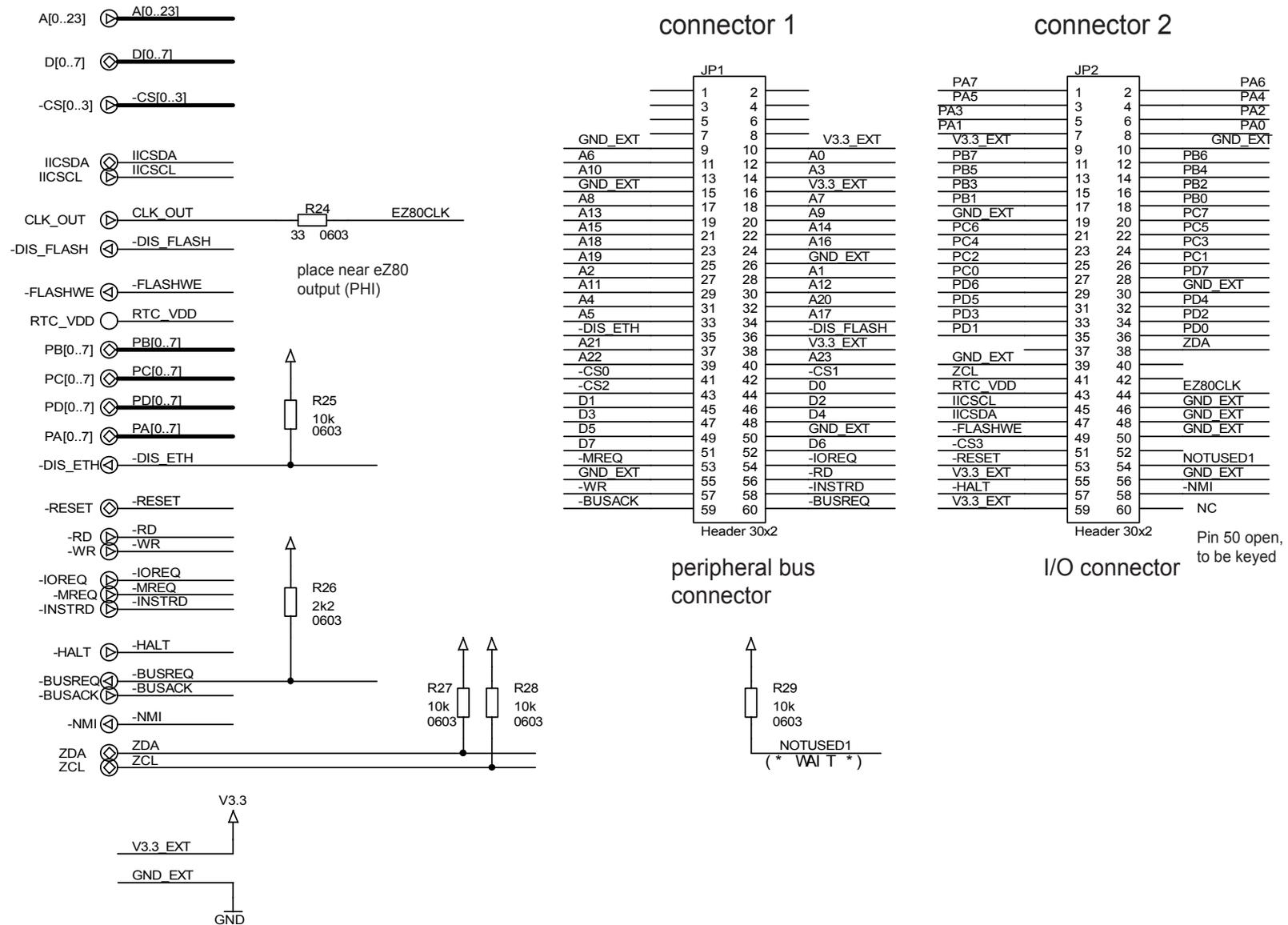
Figure 27. eZ80190 Module Schematic Diagram, #7 of 8—Headers

common power plane

no power supply on board

Input: VDD (= V3.3) = 3.3V –5%
Power: Pmax = tbd
Ptyp = tbd
Current: Imax = tbd
Ityp = tbd

V3.3 | | | | | | | VDD
C12 22uF SMT7343 | C13 22uF SMT7343 | C14 1nF 0603 | C15 100nF 0603 | C16 1nF 0603 | C17 100nF 0603
GND | | | | | | | VSS

common ground plane

PCB1

eZ80190 ethernet module board
98Cxxxx-xxx

U6D
9 8
74LCX04
TSSOP14

U5D
12
13 11
74LCX32
TSSOP14

U6E   unused gates
11 10
74LCX04
TSSOP14

U6F
13 12
74LCX04
TSSOP14
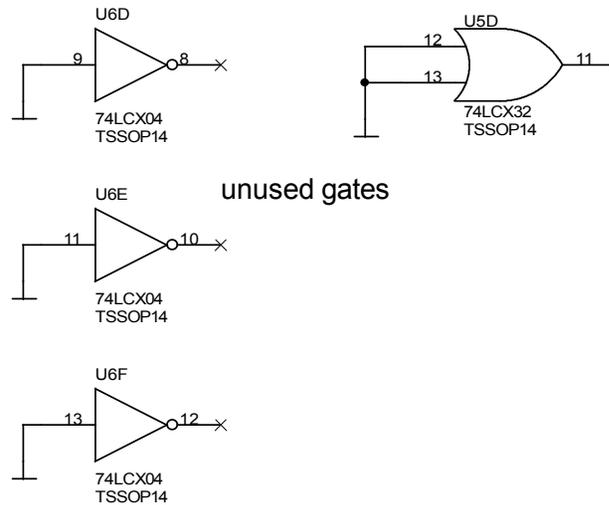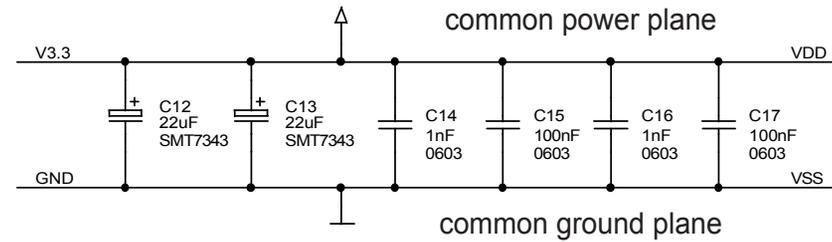
Figure 28. eZ80190 Module Schematic Diagram, #8 of 8—Power Supply

Appendix A

General Array Logic Equations

This appendix shows the equations for disabling the Ethernet signals provided by the U10 and U15 General Array Logic (GAL) devices.

U10 Address Decoder

```
//`define idle    2'b00
//`define state1  2'b01
//`define state2  2'b11
//`define state3  2'b10
// FOR eZ80® Development Platform Rev B
// This PAL generates 4 memory chip selects

module l92_decod(
  nCS_EX,         // Enables Extension Module's Memory
                  // when Low
  nFL_DIS,        // when Low Module Flash is
                  // disabled (nDIS_FL=0),
                  // when High nDIS_FL depends upon
                  // state of nmemenX
  nCS0,
  A7,    //A23
  A6,    //A22
  A5,    //A21
  A4,    //A20
  A3,    //A19
  A2,    //A18
```

```
    A1,              //A17
    A0,              //A16
    nCS2,
    nEX_FL_DIS,      // disables Flash on the expansion
                     // module, when Low
    nEM_EN,          // enables Development Platform LED
                     // and the general-purpose port.
    nDIS_FL,         // disables Module Flash when Low
    nL_RD,           // enables local data bus to be read
                     // by CPU
    nmemen1,
    nmemen2,
    nmemen3,
    nmemen4
    );

input

    nFL_DIS          /* synthesis loc="P4"*/,
    nCS0             /* synthesis loc="P5"*/,
    nCS2             /* synthesis loc="P3"*/, //was 23
    A7               /* synthesis loc="P6"*/,
    A6               /* synthesis loc="P7"*/,
    A5               /* synthesis loc="P9"*/,
    A4               /* synthesis loc="P10"*/,
    A3               /* synthesis loc="P11"*/,
    A2               /* synthesis loc="P12"*/,
    A1               /* synthesis loc="P13"*/,
    A0               /* synthesis loc="P16"*/,
    nEX_FL_DIS       /* synthesis loc="P2"*/;
```

```
//input[7:0]        A;upper part of Address Bus of 190
                    //A23=A7,A22=A6,A21=A5,A20=A4,A19=A3
                    //A18=A2,A17=A1,A16=A0

output
  nCS_EX            /* synthesis loc="P17"*/,//enables
  memory on the
                    // Expansion Module
  nmemen1           /* synthesis loc="P18"*/,//enables
  memory on
                    // the Development Platform
  nmemen2           /* synthesis loc="P19"*/,
  nmemen3           /* synthesis loc="P20"*/,
  nmemen4           /* synthesis loc="P21"*/,
  nEM_EN            /* synthesis loc="P24"*/,//enables
  LED and the
                    // general-purpose port.
  nDIS_FL           /* synthesis loc="P25"*/,
  nL_RD             /* synthesis loc="P23"*/
  ;

wire nCS_EX,
  nmemen1,
  nmemen2,
  nmemen3,
  nmemen4;

//wire MOD_DIS =
  ((nmemen1==0)|(nmemen2==0)|(nmemen3==0)|(nmemen4==0)
  );//if any
                    //of the signals is Low,
```

```
                    //Flash on the Module will be
                    //disabled if nDIS_FL is High

     wire nEXP_EN = ~((nCS0==0)&(A7==0)&(A6==1));//
       expansion module
                    //Flash enabled if this is 0

     //wire nDIS_FL = (nFL_DIS) ? ~nEXP_EN : ~(nFL_DIS);

     wire nDIS_FL = nFL_DIS & nEXP_EN; //if either of them
       is 0 Flash is
                    //disabled

     assign nCS_EX = (nEX_FL_DIS) ? nEXP_EN :
       ~(nEX_FL_DIS);
     assign nL_RD =
       ~((nmemen1==0)|(nmemen2==0)|(nmemen3==0)|(nmemen4==0
       )|(nEM_EN==0)|(nCS_EX==0));
     assign nmemen4 =
       ~((nCS2==0)&({A7,A6,A5,A4,A3}==5'h17));
     assign nmemen3 =
       ~((nCS2==0)&({A7,A6,A5,A4,A3}==5'h16));
     assign nmemen2 =
       ~((nCS2==0)&({A7,A6,A5,A4,A3}==5'h15));
     assign nmemen1 =
       ~((nCS2==0)&({A7,A6,A5,A4,A3}==5'h14));
     assign nEM_EN =
       ~((nCS2==0)&({A7,A6,A5,A4,A3,A2,A1,A0}==8'h80));
     endmodule
```

U15 Address Decoder

```
     `define   anode   8'h00
```

```
`define    cathode 8'h01
`define    latch   8'h02
// FOR eZ80® Development Platform Rev B
// This PAL generates signals that control Expansion
  Module
// access, LED and the general-purpose port.
// This device is a GAL22LV10-5JC (5ns tpd) or
  equivalent with
// Package = 28 pin PLCC
//
//

module l92_em_pal(
  nDIS_EM,
  nEM_EN,
  A0,
  A1,
  A2,
  A3,
  A4,
  A5,
  A6,
  A7,
  nRD,
  nCS,
  nWR,
  nMEMRQ,
  nIORQ,
  nEM_RD,
  nEM_WR,
```

```
         nAN_WR,
         nCT_WR,
         nDIS_ETH
         );

input    nDIS_EM /* synthesis loc="P3"*/,
  nEM_EN   /* synthesis loc="P4"*/,
  A0       /* synthesis loc="P5"*/,
  A1       /* synthesis loc="P6"*/,
  A2       /* synthesis loc="P10"*/,
  A3       /* synthesis loc="P11"*/,
  A4       /* synthesis loc="P12"*/,
  A5       /* synthesis loc="P13"*/,
  A6       /* synthesis loc="P27"*/,
  A7       /* synthesis loc="P26"*/,
  nIORQ    /* synthesis loc="P2"*/,
  nRD      /* synthesis loc="P7"*/,
  nCS      /* synthesis loc="P25"*/, //CS3 for CS9800
  nWR      /* synthesis loc="P9"*/,
  nMEMRQ   /* synthesis loc="P16"*/;

output
  nEM_RD   /* synthesis loc="P17"*/,
  nEM_WR   /* synthesis loc="P18"*/,
  nCT_WR   /* synthesis loc="P19"*/,
  nAN_WR   /* synthesis loc="P20"*/,
  nDIS_ETH /* synthesis loc="P21"*/;

parameter anode=8'h00;
parameter cathode=8'h01;
```

General Array Logic Equations

```
parameter latch=8'h02;



wire [7:0] address={A7,A6,A5,A4,A3,A2,A1,A0};

assign nEM_WR =
  ~((nDIS_EM==1)&(nWR==0)&(nEM_EN==0)&(address==latch)
  );
assign nEM_RD =
  ~((nDIS_EM==1)&(nRD==0)&(nEM_EN==0)&(address==latch)
  );

assign nAN_WR =
  ~((nDIS_EM==1)&(nWR==0)&(nEM_EN==0)&(address==anode)
  );
assign nCT_WR =
  ~((nDIS_EM==1)&(nWR==0)&(nEM_EN==0)&(address==cathod
  e));

assign nDIS_ETH = ~(nCS);
endmodul
```

Customer Support

For answers to technical questions about the product, documentation, or any other issues with ZiLOG's offerings, please visit ZiLOG's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit ZiLOG's Technical Support at http://support.zilog.com.