Voltage Detector with Delay Circuit and Manual Reset

FEATURES

- Accuracy ± 0.8%
- Low Power Consumption
  0.6 µA (Detect at V_{DF} = 1.8 V, V_{IN} = 1.62 V)
  0.7 µA (Release at V_{DF} = 1.8 V, V_{IN} = 1.98 V)
- Detect Voltage Range 1.5 V – 5.5 V in 0.1 V increments
- Operating Voltage Range 0.7 V – 6.0 V
- Detect Voltage Temperature Drift ±50 ppm/^{0}C
- Output Configuration CMOS (Version C) or N-channel Open Drain (N Version)
- Preprogrammed Release Delay Time
- Manual Reset Input
- Active High or Active Low Reset Output
- Operating Ambient Temperature - 40 + 85^{0}C
- Packages : USPN-4, SSOT-24, and SOT-25
- EU RoHS Compliant, Pb Free

APPLICATIONS

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

DESCRIPTION

The IXD5127 are highly precise, low power consumption, CMOS voltage detectors, with manual reset input and built-in delay circuit, manufactured using laser trimming technology.

It maintains high accuracy, low power consumption, and accurate release delay time over the full operation temperature range.

Manual reset input allows IXD5127 to generate reset at any desirable moment.

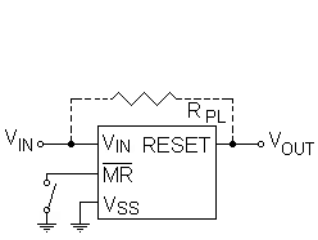
With low power consumption and high accuracy, this series is suitable for precision mobile equipment.

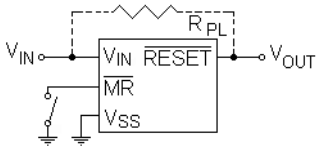
The IXD5127 in ultra small packages are ideally suited for high-density PC boards.

The IXD5127 is available in both CMOS and N-channel open drain output configurations.

This detector is available in USPN-4, SSOT-24, and SOT-25 packages.

TYPICAL APPLICATION CIRCUIT

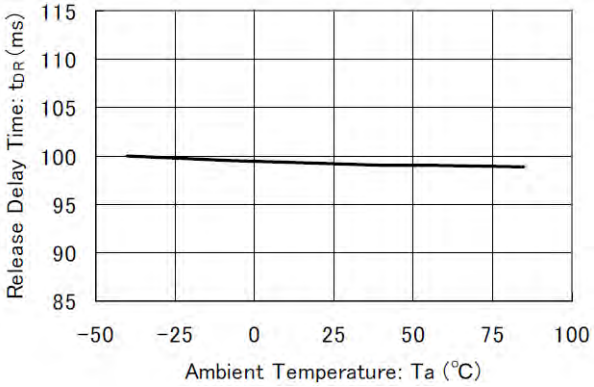




Pull-up Resistor R_{PL} used with N-ch

TYPICAL PERFORMANCE CHARACTERISTIC

Release Delay Time vs. Ambient Temperature
IXD5127x27Bx
V_{IN} = V_{DFL} x 0.9 →V_{DFL} x 1.1, $\overline{MR}$ - Open



ABSOLUTE MAXIMUM RATINGS

PARAMETER			SYMBOL	RATINGS	UNITS
Input Voltage			V_{IN}	– 0.3 ~ +6.5	V
$\overline{MR}$ Input Voltage			V_{MR}	– 0.3 ~ +6.5	V
Output Current			I_{OUT}	20	mA
Output Voltage	CMOS Output		V_{RST}	– 0.3 ~ V_{IN} + 0.3 ≤ 6.5	V
	N-channel Open Drain			– 0.3 ~ +6.5	
Power Dissipation		USPN-4	P_D	100	mW
		SOT-25		250	
		SSOT-24		150	
Operating Temperature Range			T_{OPR}	– 40 ~ + 85	^{0}C
Storage Temperature Range			T_{STG}	– 55 ~ +125	^{0}C

All voltages are in respect to V_{SS}

ELECTRICAL OPERATING CHARACTERISTICS

For N-channel open drain configuration R_{PULL} = 100 kΩ, V_{PULL} = V_{IN} Ta = 25 ^{0}C

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
Operating Voltage	V_{IN}	$V_{DF(T)}$ [1] = 1.5 – 5.5 V, $\overline{MR}$ - Open		0.7[2]		6.0	V	
Detect Voltage	V_{DF}	V_{IN} = 1.0 – 6.0 V		E-1[3]			V	①
Hysteresis Width	V_{HYS}			V_{DFL} x 0.02	V_{DFL} x 0.05	V_{DFL} x 0.08	V	①
Supply Current1[3]	I_{SS1}	V_{IN} = V_{DFL} x 0.9, $\overline{MR}$ - Open	V_{IN} = 1.5 – 1.8 V,		0.6	1.4	µA	②
			V_{IN} = 1.9 – 3.0 V		0.7	1.6		
			V_{IN} = 3.1 – 5.5 V		1.0	1.9		
Supply Current2[3]	I_{SS2}	V_{IN} = V_{DF} x 1.1[4] $\overline{MR}$ - Open	V_{IN} = 1.5 – 1.8 V,		0.7	1.6	µA	②
			V_{IN} = 1.9 – 3.0 V		0.8	1.9		
			V_{IN} = 3.1 – 5.5 V		1.1	2.35		
Detect Voltage Temperature Characteristics	$\frac{\Delta V_{DF}}{V_{DF} * \Delta T_{OPR}}$	- 40 ^{0}C ≤ T_{OPR} ≤ 85 ^{0}C			± 50		ppm/^{0}C	①
Detect Delay Time[6]	t_{DF}	V_{IN} = V_{DFL} x 1.1 → V_{DFL} x 0.9, $\overline{MR}$ - Open				100[9]	µs	④
Release Delay Time[7]	t_{DR}	V_{IN} = V_{DFL} x 0.9 → V_{DFL} x 1.1, $\overline{MR}$ - Open		E-2[8]			ms	④
$\overline{MR}$ LOW Level Voltage	V_{MRL}	V_{DFL} x 1.1 ≤ V_{IN} ≤ 6.0 V		0		0.3	V	⑤
$\overline{MR}$ HIGH Level Voltage	V_{MRH}	V_{DFL} x 1.1 ≤ V_{IN} ≤ 6.0 V		1.0		6.0	V	⑤
$\overline{MR}$ Pull-up Resistance	R_{MR}			0.4	0.8	3.0	MΩ	⑥
$\overline{MR}$ Pulse Width	T_{MR}	V_{IN} = 6.0 V		150			ns	⑦
$\overline{RESET}$ Output Current IXD5118xxxA – E versions only	I_{OUT1}	V_{RST} = 0.5 V, $\overline{MR}$ - Open N-channel MOSFET	V_{IN} = 0.7 V	0.014	0.2		mA	③
			V_{IN} = 1.0 V	0.5	1.6			
			V_{IN} = 2.0 V, $V_{DF(T)}$ > 2.0 V	4.4	7.0			
			V_{IN} = 3.0 V, $V_{DF(T)}$ > 3.0 V	7.0	9.0			
			V_{IN} = 4.0 V, $V_{DF(T)}$ > 4.0 V	8.5	11.0			
			V_{IN} = 5.0 V, $V_{DF(T)}$ > 5.0 V	9.0	12.0			
	I_{OUT2}[5]	V_{IN} = 6.0V, V_{RST} = 5.5 V, $\overline{MR}$ - Open P-channel MOSFET	V_{IN} = 6.0 V		-4.5	-3.0	mA	③
$\overline{RESET}$ Leakage Current IXD5118xxxA – E versions only	I_{LEAK}	IXD5127CxxA - E (P-channel)	V_{IN} = V_{DFL} x 0.9, V_{RST} = 0 V, $\overline{MR}$ - Open		-0.01		µA	③
		IXD5127NxxA - E (N-channel)	V_{IN} = V_{RST} = 6.0 V, $\overline{MR}$ - Open		0.01	0.15		
RESET Output Current IXD5118xxxF – K versions only	I_{OUT1}	V_{RST} = 0.5 V, $\overline{MR}$ - Open N-channel MOSFET	V_{IN} = 1.65 V, $V_{DF(T)}$ = 1.5 V	0.5	1.6		mA	③
			V_{IN} = 2.0 V, $V_{DF(T)}$ ≤ 1.8 V	4.4	7.0			
			V_{IN} = 3.0 V, $V_{DF(T)}$ ≤ 2.7 V	7.0	9.0			
			V_{IN} = 4.0 V, $V_{DF(T)}$ ≤ 3.6 V	8.5	11.0			
			V_{IN} = 5.0 V, $V_{DF(T)}$ ≤ 4.6 V	9.0	12.0			
			V_{IN} = 6.0 V	9.0	12.0			
	I_{OUT2}[5]	V_{IN} = 6.0V, V_{RST} = 5.5 V, $\overline{MR}$ - Open P-channel MOSFET	V_{IN} = 0.7 V		-0.07	-0.01	mA	③
			V_{IN} = 1.0 V		-0.4	-0.9		
			V_{IN} = 2.0 V, $V_{DF(T)}$ > 2.0 V		-2.0	-1.3		
			V_{IN} = 3.0 V, $V_{DF(T)}$ > 2.0 V		-3.0	-1.8		
			V_{IN} = 4.0 V, $V_{DF(T)}$ > 2.0 V		-4.0	-2.5		
			V_{IN} = 5.0 V, $V_{DF(T)}$ > 2.0 V		-4.5	-3.0		

ELECTRICAL OPERATING CHARACTERISTICS (CONTINUED)

Ta = 25 ^{0}C

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
RESET Leakage Current IXD5118xxxF – K versions only	I_{LEAK}	IXD5127CxxA - E (P-channel)	V_{IN} = V_{DFL} x 0.9, V_{RST} = 0 V, $\overline{MR}$ - Open		0.01	0.15	µA	③
		IXD5127NxxA - E (N-channel)	V_{IN} = V_{RST} = 6.0 V, $\overline{MR}$ - Open		-0.01			

NOTE:

1) $V_{DF(T)}$ is a nominal detect voltage
2) Minimum voltage, at which V_{RST} remains below 0.3 V for IXD5127xxxA – E versions or above 0.4 V for IXD5127xxxF - K versions
3) Please refer to the table named Voltage Chart
4) V_{IN} = 6.0 V at $V_{DF(T)}$ = 5.5 V
5) IXD5127C version only
6) A time between V_{IN} = V_{DFL} and V_{RST} = V_{DFL} × 0.45 when V_{IN} falls.
7) A time between V_{IN}=V_{DFL}+V_{HYS} and V_{RST}=V_{DFL} × 0.55 when V_{IN} rises.
8) Please refer to the table named Release Delay Time
9) 200 µs for IXD5127NxxF – K versions

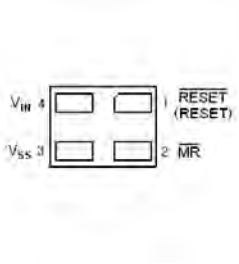
Voltage Chart

NOMINAL DETECT VOLTAGE (V)	DETECT VOLTAGE (V) E-1		NOMINAL DETECT VOLTAGE (V)	DETECT VOLTAGE (V) E-1	
$V_{DF(T)}$	V_{DFL} or V_{DFH}		$V_{DF(T)}$	V_{DFL} or V_{DFH}	
	MIN.	MAX		MIN.	MAX.
1.50	1.4880	1.5120	3.60	3.5712	3.6288
1.60	1.5872	1.6128	3.70	3.6704	3.7296
1.70	1.6864	1.7136	3.80	3.7696	3.8304
1.80	1.7856	1.8144	3.90	3.8688	3.9312
1.90	1.8848	1.9152	4.00	3.9680	4.0320
2.00	1.9840	2.0160	4.10	4.0672	4.1328
2.10	2.0832	2.1168	4.20	4.1664	4.2336
2.20	2.1824	2.2176	4.30	4.2656	4.3344
2.30	2.2816	2.3184	4.40	4.3648	4.4352
2.40	2.3808	2.4192	4.50	4.4640	4.5360
2.50	2.4800	2.5200	4.60	4.5632	4.6368
2.60	2.5792	2.6208	4.70	4.6624	4.7376
2.70	2.6784	2.7216	4.80	4.7616	4.8384
2.80	2.7776	2.8224	4.90	4.8608	4.9392
2.90	2.8768	2.9232	5.00	4.9600	5.0400
3.00	2.9760	3.0240	5.10	5.0592	5.1408
3.10	3.0752	3.1248	5.20	5.1584	5.2416
3.20	3.1744	3.2256	5.30	5.2576	5.3424
3.30	3.2736	3.3264	5.40	5.3568	5.4432
3.40	3.3728	3.4272	5.50	5.4560	5.5440
3.50	3.4720	3.5280			

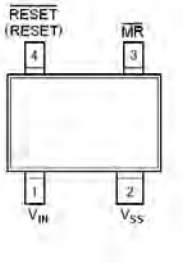
Release Delay Time

TYPE	RELEASE DELAY TIME (ms) E-2		
	t_{DR}		
	MIN.	TYP.	MAX.
IXD5127CxxA/IXD5127NxxA	42.5	50	57.5
IXD5127CxxB/IXD5127NxxB	85	100	115
IXD5127CxxC/IXD5127NxxC	170	200	230
IXD5127CxxD/IXD5127NxxD	340	400	460
IXD5127CxxE/IXD5127NxxE	680	800	920
IXD5127CxxF/IXD5127NxxF	42.5	50	57.5
IXD5127CxxG/IXD5127NxxG	85	100	115
IXD5127CxxH/IXD5127NxxH	170	200	230
IXD5127CxxJ/IXD5127NxxJ	340	400	460
IXD5127CxxK/IXD5127NxxK	680	800	920

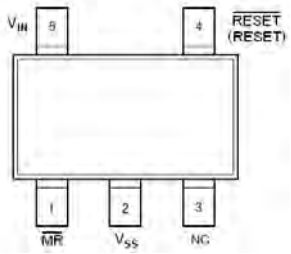
PIN CONFIGURATION



USPN-4
(BOTTOM VIEW)



SSOT-24
(TOP VIEW)



SOT-25
(TOP VIEW)

PIN ASSIGNMENT

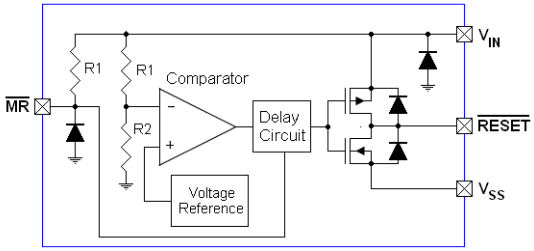
PIN NUMBER			PIN NAME	FUNCTIONS
USPN-4	SSOT-24	SOT-25		
1	4	4	$\overline{RESET}$/RESET	Output Voltage ($\overline{RESET}$ Active "LOW"[1], RESET – Active "HIGH"[2])
2	3	1	$\overline{MR}$	Manual Reset Input ("HIGH" or "OPEN" State – Normal Operations, "LOW" – Forced Reset
3	2	2	V_{SS}	Ground
4	1	5	V_{IN}	Power Input
		3	NC	No internal Connect

NOTE

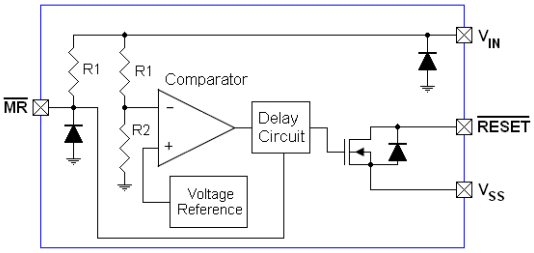
1) Type IXD5127xxxA – E versions
2) Type IXD5127xxxF – K versions

BLOCK DIAGRAMS

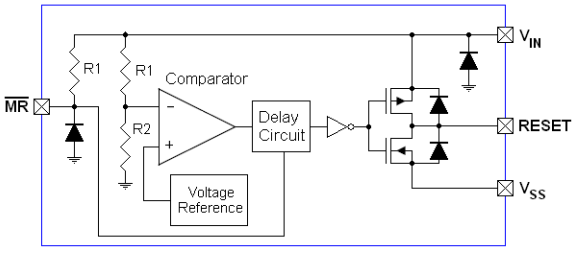
XD5127CxxA - E



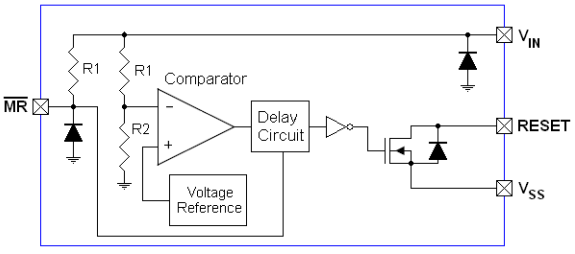
IXD5127NxxA - E



IXD5127CxxF - K

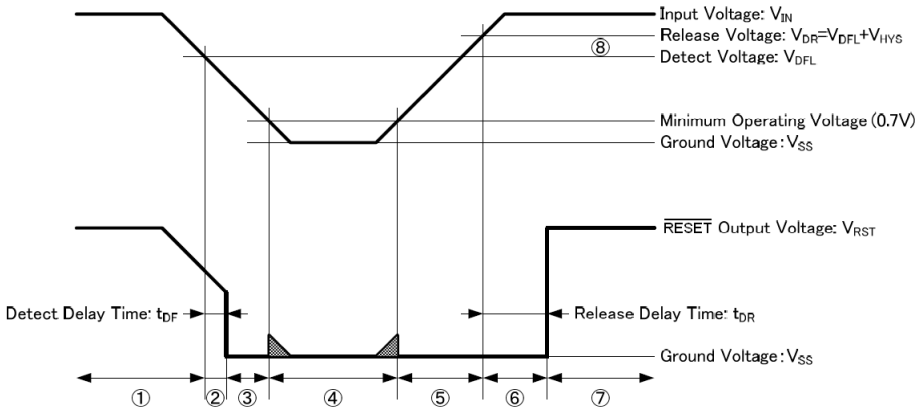


IXD5127NxxF – K



Diodes inside the circuits are ESD protection diodes and parasitic diodes.

BASIC OPERATION



The timing diagram shown below exlains operation of the IXD5127xxxA - E in a typical application circuit.

① At the initial state, an input voltage V_{IN} is higher than the detect voltage V_{DFL}, and output voltage V_{RST} is equal to the input voltage V_{IN}. In the case of N-channel open drain architecture, the $\overline{RESET}$ pin is in a high-impedance state, and the output voltage V_{RST} is equal to the pull-up voltage.

②, ③ After the elapse of the Detect Delay Time t_{DF} that starts when the input voltage V_{IN} falls below the detect voltage V_{DFL}, an output voltage V_{RST} becomes equal to the ground voltage V_{SS} (detection state).

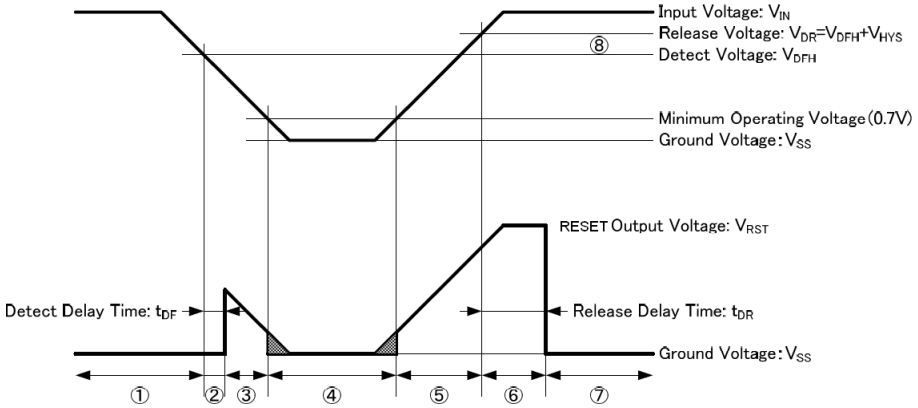
④ If the input voltage V_{IN} drops below minimum operating voltage of 0.7 V, the output goes into undefined state. In case of N-channel open drain output architecture, an output voltage V_{RST} may be equal to the pull-up voltage.

⑤ If input voltage V_{IN} is above minimum operating voltage of 0.7 V, but less than the release voltage V_{DR}, the output voltage V_{RST} is at the ground level.

⑥ The delay circuit keeps the output voltage V_{RST} at the ground level until the Release Delay Time t_{DR} from the moment, when the input voltage V_{IN} becomes higher than the release voltage V_{DR}, elapses.

⑦ After the Release Delay Time t_{DR} elapses, the output voltage V_{RST} becomes equal to the input voltage V_{IN} (release state). In the case of N-channel open drain architecture, the $\overline{RESET}$ pin goes into high impedance state, and an output voltage V_{RST} becomes equal to the pull-up voltage.

⑧ The difference between the release voltage V_{DR} and the detect voltage V_{DFL} is the hysteresis width V_{HYS}.



The timing diagram shown below explains operation of the IXD5127xxxF - K in a typical application circuit.

① At the initial state, when an input voltage V_{IN} is higher than the detect voltage V_{DFH}, an output voltage V_{RST} is equal to the ground voltage V_{SS}.

②③ After the elapse of the Detect Delay Time t_{DF} that starts, when the input voltage V_{IN} falls below the detect voltage V_{DFH}, the output voltage V_{RST} is equal to the input voltage V_{IN} (detection state). In the case of N-channel

open drain architecture, the RESET pin is in a high-impedance state, and the output voltage V_{RST} is equal to the pull-up voltage.

④ If the input voltage V_{IN} falls below the minimum operating voltage of 0.7 V, the output goes into undefined state.

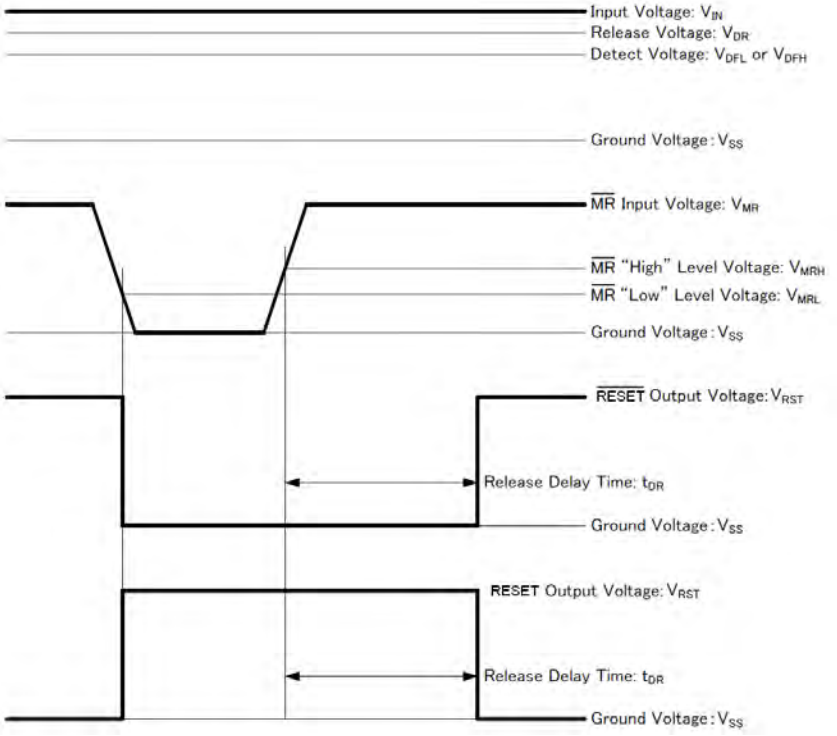
⑤ When the input voltage V_{IN} is above the minimum operating voltage of 0.7V, but below the release voltage V_{DR}, the output voltage V_{RST} is equal to the V_{IN} voltage. In the case of N-channel open drain architecture, the RESET pin is in a high-impedance state, and the output voltage V_{RST} is equal to the pull-up voltage.

⑥ The delay circuit keeps the output voltage V_{RST} at the V_{IN} level until the Release Delay Time t_{DR} from the moment, when the input voltage V_{IN} becomes higher than the release voltage V_{DR}, elapses.

⑦ After the Release Delay Time t_{DR} elapses, the output voltage V_{RST} becomes equal to the ground voltage V_{SS} (release state).

⑧ The difference between the release voltage V_{DR} and the detect voltage V_{DFH} is the hysteresis width V_{HYS}.

The timing diagram shown below explains operation of the $\overline{MR}$ pin.



Signal applied to the $\overline{MR}$ pin can forcibly change the state of the RESET ($\overline{RESET}$) pin output.

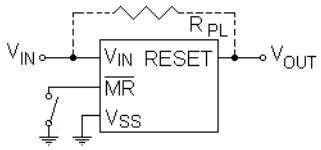
If the $\overline{MR}$ pin voltage V_{MR} falls equal or below "LOW" threshold level, RESET ($\overline{RESET}$) pin output change state to the detect state, even if V_{IN} voltage remains above detect voltage V_{DF}.

After the $\overline{MR}$ input voltage, V_{MR}, changes state from "LOW" to "HIGH," the output pin remains in the detection state during the Release Delay Time t_{DR}. After the Release Delay Time t_{DR} elapses, the output pin changes state to the release one.

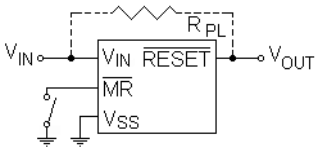
NOTE:

1) The output voltage in the release state is as shown below by product type.
   IXD5127CxxA – E types - V_{IN}
   IXD5127NxxA – E types - V_{PULL}
   IXD5127xxxF – K types - Ground voltage (V_{SS})
2) The output voltage in the detect state is as shown below by product type.
   IXD5127xxxA – E types - Ground voltage (V_{SS})
   IXD5127CxxF – K types - V_{IN}
   IXD5127NxxF – K types - V_{PULL}
3) A pull-up resistor (R_{MR}) is built-in between the $\overline{MR}$ pin and the V_{IN} pin, and thus, if a voltage below V_{IN} is applied to the $\overline{MR}$ pin, current will flow from the V_{IN} to the $\overline{MR}$ pin.
4) The $\overline{MR}$ pin input voltage should be within the range from V_{SS} to 6.0 V.

TYPICAL APPLICATION CIRCUIT



IXD5127xxxF - K



IXD5127xxxA - E

LAYOUT AND USE CONSIDERATIONS

1. The IC may malfunction if absolute maximum ratings are exceeded.
2. High impedance V_{IN} power supply may cause IC malfunction, if V_{IN} voltage falls below minimum operating level due current consumption, when IC output changes state. In addition, output voltage at “High” state reflects every variations of V_{IN} voltage.
3. High impedance V_{IN} power supply may cause IC oscillations, if voltage drop at power supply’s internal resistance exceeds IC hysteresis.
4. Note that a rapid and high amplitude fluctuation of the V_{IN} pin voltage, as well as a power supply noise, may cause a wrong IC operation. The capacitor between VIN and GND pins should be used to minimize noise impact.
5. Output voltage In N channel open drain configuration depends on pull-up resistance, as well as on/off resistance of the N-channel MOSFET (see block diagrams above).

   For IXD5127NxxA – E versions with $\overline{\text{RESET}}$ pin active LOW, output voltage during detection

   $$V_{OUT} = V_{PULL} / (1 + R_{PULL} / R_{ON}),$$

   where V_{PULL} is a pull up voltage and R_{ON} is an N-channel MOSFET on-resistance, which can be calculated as V_{RST} / I_{OUT1} from electrical characteristics.

   For example:

   To get $V_{OUT} \leq 0.1V$ at detect state, with $R_{ON} = 0.5/4.4 \times 10^{-3} = 114\ \Omega$ (max) at $V_{IN} = 2.0$ V and $V_{PULL} = 3.0$ V, pull-up resistor value should be

   $$R_{PULL} = (V_{PULL} / V_{OUT} - 1) \times R_{ON} = (3 / 0.1\text{-}1) \times 114 \geq 3.3\ k\Omega\ .(1)$$

   Note that decreasing V_{IN} voltage increases R_{ON} resistance, so minimum expected V_{IN} voltage should be used for calculations..

   At releasing state $V_{OUT} = V_{PULL}/(1 + R_{PULL} / R_{OFF})$, where $R_{OFF} = V_{OUT}/I_{LEAK} = 40\ M\Omega$ (min) for N-channel MOSFET in off state.

   Therefore, in this case, pull-up resistor should be

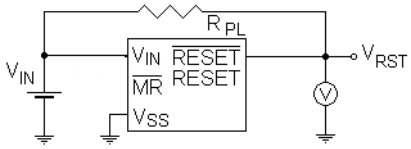
   $$R_{PULL} = (V_{PULL}/V_{OUT}\text{-}1) \times R_{OFF} = (3/2.99 - 1) \times 40 \times 10^6 \leq 133\ k\Omega\ (2)$$

   to get $V_{OUT} \geq 2.99$ V at $V_{PULL} = 3.0$ V.

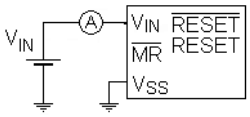
   For IXD5127NxxF – K versions with RESET pin active HIGH, output voltage during detect state should be calculated using equation (2), while output voltage during release state should be calculated using equation (1), because for these parts N-channel MOSFET is in opposite state compared to example shown above.

TEST CIRCUITS

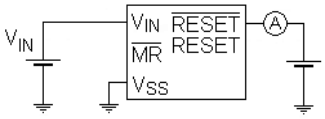
Circuit ①



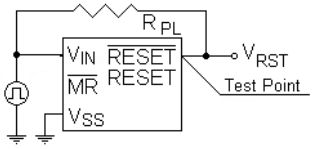
Circuit ②



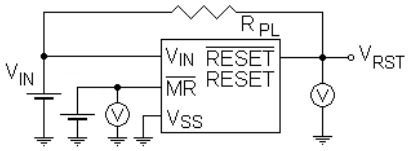
Circuit ③



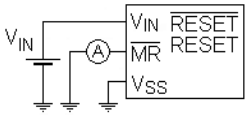
Circuit ④



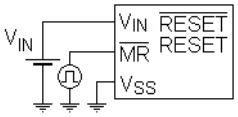
Circuit ⑤



Circuit ⑥



Circuit ⑦



Pull-up Resistor R_{PL} = 100 kΩ is used for IXD5127N version only

ORDERING INFORMATION

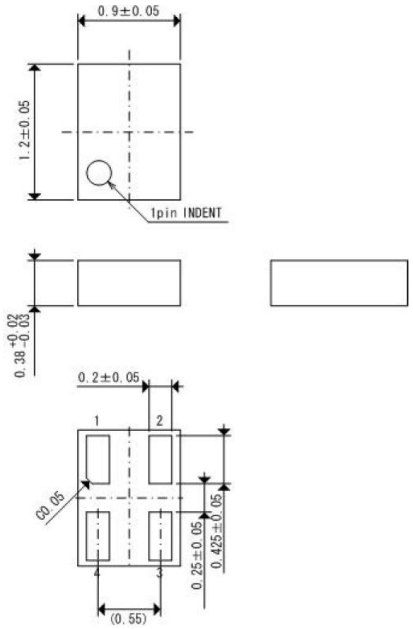
IXD5127①②③④⑤⑥-⑦

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-channel Open Drain Output
②③	Detect Voltage (V_{DF})	15 - 55	Detect Voltage Range: 1.5 V～5.5 V, e.g. 3.2 V - ② = 3, ③ = 2
④	Options	A	$\overline{\text{RESET}}$ – Active LOW, Release Delay Time – 50 ms
		B	$\overline{\text{RESET}}$ – Active LOW, Release Delay Time – 100 ms
		C	$\overline{\text{RESET}}$ – Active LOW, Release Delay Time – 200 ms
		D	$\overline{\text{RESET}}$ – Active LOW, Release Delay Time – 400 ms
		E	$\overline{\text{RESET}}$ – Active LOW, Release Delay Time – 800 ms
		F	RESET – Active HIGH, Release Delay Time – 50 ms
		G	RESET – Active HIGH, Release Delay Time – 100 ms
		H	RESET – Active HIGH, Release Delay Time – 200 ms
		J	RESET – Active HIGH, Release Delay Time – 400 ms
		K	RESET – Active HIGH, Release Delay Time – 800 ms
⑤⑥-⑦(*)	Packages (Order Unit)	7R-G	USPN-4 (5000/Reel)
		NR-G	SSOT-24 (3000/reel)
		MR-G	SOT-25 (3000/Reel)

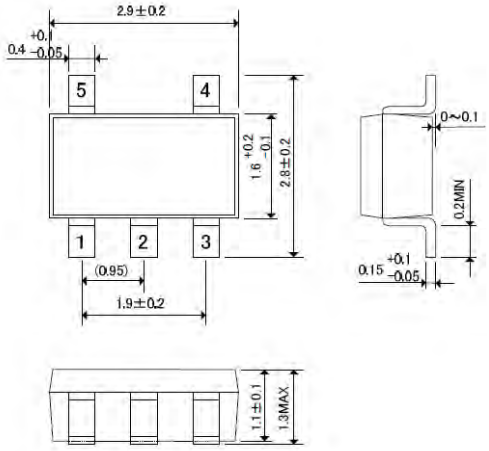
NOTE:
The "-G" suffix denotes Halogen and Antimony free as well as being fully RoHS compliant.

PACKAGE DRAWING AND DIMENSIONS

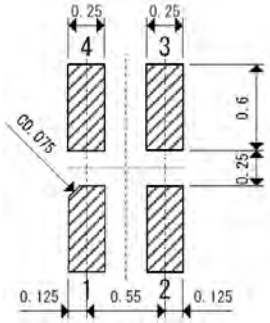
USPN-4, Units: mm



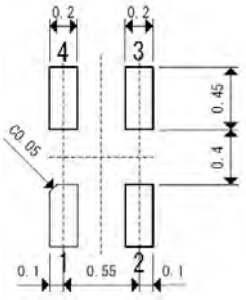
SOT-25, Units: mm



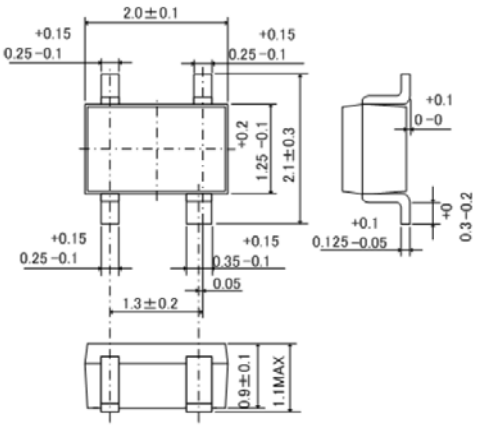
USPN-4 Reference Pattern Layout, Units: mm



USP-4 Reference Metal Mask Design

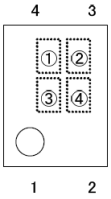


SSOT-24, Units: mm



MARKING

USPN-4



①- Represents product series and output configuration

MARK	OUTPUT CONFIGURATION	PRODUCT SERIES
F	CMOS	IXD5127Cxxxxx-G
H	N-channel	IXD5127Nxxxxx-G

② - Represents detect voltage

MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)	
A	1.5	1.6	K	2.9	3.0	T	4.3	4.4
B	1.7	1.8	L	3.1	3.2	U	4.5	4.6
C	1.9	2.0	M	3.3	3.4	V	4.7	4.8
D	2.1	2.2	N	3.5	3.6	X	4.9	5.0
E	2.3	2.4	P	3.7	3.8	Y	5.1	5.2
F	2.5	2.6	R	3.9	4.0	Z	5.3	5.4
H	2.7	2.8	S	4.1	4.2	0	5.5	-

③- Represents detect voltage range and release delay time/detect state output logic

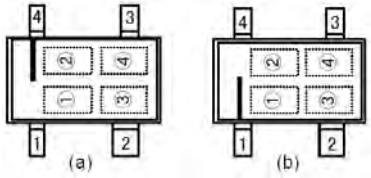
MARK	DETECT VOLTAGE	RELEASE DELAY TIME/OUTPUT LOGIC	PRODUCT SERIES
A	Odd Value	50 ms/Active Low	IXD5127x15Axx-G – IXD5127x55Axx-G
B		100 ms/Active Low	IXD5127x15Bxx-G – IXD5127x55Bxx-G
C		200 ms/Active Low	IXD5127x15Cxx-G – IXD5127x55Cxx-G
D		400 ms/Active Low	IXD5127x15Dxx-G – IXD5127x55Dxx-G
E		800 ms/Active Low	IXD5127x15Exx-G – IXD5127x55Exx-G
F		50 ms/Active High	IXD5127x15Fxx-G – IXD5127x55Fxx-G
H		100 ms/Active High	IXD5127x15Gxx-G – IXD5127x55Gxx-G
K		200 ms/Active High	IXD5127x15Hxx-G – IXD5127x55Hxx-G
L		400 ms/Active High	IXD5127x15Jxx-G – IXD5127x55Jxx-G
M		800 ms/Active High	IXD5127x15Kxx-G – IXD5127x55Kxx-G
N	Even Value	50 ms/Active Low	IXD5127x16Axx-G – IXD5127x54Axx-G
P		100 ms/Active Low	IXD5127x16Bxx-G – IXD5127x54Bxx-G
R		200 ms/Active Low	IXD5127x16Cxx-G – IXD5127x54Cxx-G
S		400 ms/Active Low	IXD5127x16Dxx-G – IXD5127x54Dxx-G
T		800 ms/Active Low	IXD5127x16Exx-G – IXD5127x54Exx-G
U		50 ms/Active High	IXD5127x16Fxx-G – IXD5127x54Fxx-G
V		100 ms/Active High	IXD5127x16Gxx-G – IXD5127x54Gxx-G
X		200 ms/Active High	IXD5127x16Hxx-G – IXD5127x54Hxx-G
Y		400 ms/Active High	IXD5127x16Jxx-G – IXD5127x54Jxx-G
Z		800 ms/Active High	IXD5127x16Kxx-G – IXD5127x54Kxx-G

④ - Represents production lot number

0 to 9, A to Z, and inverted 0 to 9, A to Z repeated. (G, I, J, O, Q, W excluded.)

MARKING (CONTINUED)

SSOT-24



Products with CMOS output configuration are shipped in the package with the orientation bar on the top (a), while products with N-channel configuration are shipped with orientation bar on the bottom (b).

① - Represents product series and detect voltage range/output configuration

MARK	OUTPUT CONFIGURATION	DETECT VOLTAGE	RELEASE DELAY TIME/OUTPUT LOGIC	PRODUCT SERIES
5	CMOS	Odd Value	50 ms/Active Low	IXD5127x15Axx-G – IXD5127x55Axx-G
6			100 ms/Active Low	IXD5127x15Bxx-G – IXD5127x55Bxx-G
7			200 ms/Active Low	IXD5127x15Cxx-G – IXD5127x55Cxx-G
8			400 ms/Active Low	IXD5127x15Dxx-G – IXD5127x55Dxx-G
9			800 ms/Active Low	IXD5127x15Exx-G – IXD5127x55Exx-G
A			50 ms/Active High	IXD5127x15Fxx-G – IXD5127x55Fxx-G
B			100 ms/Active High	IXD5127x15Gxx-G – IXD5127x55Gxx-G
C			200 ms/Active High	IXD5127x15Hxx-G – IXD5127x55Hxx-G
D			400 ms/Active High	IXD5127x15Jxx-G – IXD5127x55Jxx-G
E			800 ms/Active High	IXD5127x15Kxx-G – IXD5127x55Kxx-G
F		Even Value	50 ms/Active Low	IXD5127x16Axx-G – IXD5127x54Axx-G
H			100 ms/Active Low	IXD5127x16Bxx-G – IXD5127x54Bxx-G
K			200 ms/Active Low	IXD5127x16Cxx-G – IXD5127x54Cxx-G
N			400 ms/Active Low	IXD5127x16Dxx-G – IXD5127x54Dxx-G
P			800 ms/Active Low	IXD5127x16Exx-G – IXD5127x54Exx-G
R			50 ms/Active High	IXD5127x16Fxx-G – IXD5127x54Fxx-G
S			100 ms/Active High	IXD5127x16Gxx-G – IXD5127x54Gxx-G
T			200 ms/Active High	IXD5127x16Hxx-G – IXD5127x54Hxx-G
U			400 ms/Active High	IXD5127x16Jxx-G – IXD5127x54Jxx-G
V			800 ms/Active High	IXD5127x16Kxx-G – IXD5127x54Kxx-G
0	N-channel	Odd Value	50 ms/Active Low	IXD5127x15Axx-G – IXD5127x55Axx-G
1			100 ms/Active Low	IXD5127x15Bxx-G – IXD5127x55Bxx-G
2			200 ms/Active Low	IXD5127x15Cxx-G – IXD5127x55Cxx-G
3			400 ms/Active Low	IXD5127x15Dxx-G – IXD5127x55Dxx-G
4			800 ms/Active Low	IXD5127x15Exx-G – IXD5127x55Exx-G
5			50 ms/Active High	IXD5127x15Fxx-G – IXD5127x55Fxx-G
6			100 ms/Active High	IXD5127x15Gxx-G – IXD5127x55Gxx-G
7			200 ms/Active High	IXD5127x15Hxx-G – IXD5127x55Hxx-G
8			400 ms/Active High	IXD5127x15Jxx-G – IXD5127x55Jxx-G
9			800 ms/Active High	IXD5127x15Kxx-G – IXD5127x55Kxx-G
A		Even Value	50 ms/Active Low	IXD5127x16Axx-G – IXD5127x54Axx-G
B			100 ms/Active Low	IXD5127x16Bxx-G – IXD5127x54Bxx-G
C			200 ms/Active Low	IXD5127x16Cxx-G – IXD5127x54Cxx-G
D			400 ms/Active Low	IXD5127x16Dxx-G – IXD5127x54Dxx-G
E			800 ms/Active Low	IXD5127x16Exx-G – IXD5127x54Exx-G
F			50 ms/Active High	IXD5127x16Fxx-G – IXD5127x54Fxx-G
H			100 ms/Active High	IXD5127x16Gxx-G – IXD5127x54Gxx-G
K			200 ms/Active High	IXD5127x16Hxx-G – IXD5127x54Hxx-G
L			400 ms/Active High	IXD5127x16Jxx-G – IXD5127x54Jxx-G
M			800 ms/Active High	IXD5127x16Kxx-G – IXD5127x54Kxx-G

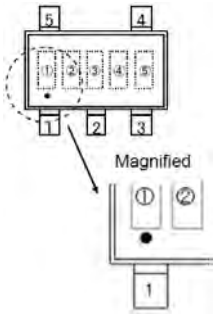
② - Represents detect voltage

MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)	
A	1.5	1.6	K	2.9	3.0	T	4.3	4.4
B	1.7	1.8	L	3.1	3.2	U	4.5	4.6
C	1.9	2.0	M	3.3	3.4	V	4.7	4.8
D	2.1	2.2	N	3.5	3.6	X	4.9	5.0
E	2.3	2.4	P	3.7	3.8	Y	5.1	5.2
F	2.5	2.6	R	3.9	4.0	Z	5.3	5.4
H	2.7	2.8	S	4.1	4.2	0	5.5	-

③④ - Represents production lot number: 01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ、B1～ZZ repeated. (G, I, J, O, Q, W excluded.)

MARKING (CONTINUED)

SOT-25



①- Represents product series and output configuration

MARK	OUTPUT CONFIGURATION	PRODUCT SERIES
5	CMOS	IXD5127Cxxxxx-G
6	N-channel	IXD5127Nxxxxx-G

② - Represents detect voltage

MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)	
A	1.5	1.6	K	2.9	3.0	T	4.3	4.4
B	1.7	1.8	L	3.1	3.2	U	4.5	4.6
C	1.9	2.0	M	3.3	3.4	V	4.7	4.8
D	2.1	2.2	N	3.5	3.6	X	4.9	5.0
E	2.3	2.4	P	3.7	3.8	Y	5.1	5.2
F	2.5	2.6	R	3.9	4.0	Z	5.3	5.4
H	2.7	2.8	S	4.1	4.2	0	5.5	-

③ - Represents detect voltage range and release delay time/detect state output logic

MARK	DETECT VOLTAGE	RELEASE DELAY TIME/OUTPUT LOGIC	PRODUCT SERIES
A	Odd Value	50 ms/Active Low	IXD5127x15Axx-G – IXD5127x55Axx-G
B		100 ms/Active Low	IXD5127x15Bxx-G – IXD5127x55Bxx-G
C		200 ms/Active Low	IXD5127x15Cxx-G – IXD5127x55Cxx-G
D		400 ms/Active Low	IXD5127x15Dxx-G – IXD5127x55Dxx-G
E		800 ms/Active Low	IXD5127x15Exx-G – IXD5127x55Exx-G
F		50 ms/Active High	IXD5127x15Fxx-G – IXD5127x55Fxx-G
H		100 ms/Active High	IXD5127x15Gxx-G – IXD5127x55Gxx-G
K		200 ms/Active High	IXD5127x15Hxx-G – IXD5127x55Hxx-G
L		400 ms/Active High	IXD5127x15Jxx-G – IXD5127x55Jxx-G
M		800 ms/Active High	IXD5127x15Kxx-G – IXD5127x55Kxx-G
N	Even Value	50 ms/Active Low	IXD5127x16Axx-G – IXD5127x54Axx-G
P		100 ms/Active Low	IXD5127x16Bxx-G – IXD5127x54Bxx-G
R		200 ms/Active Low	IXD5127x16Cxx-G – IXD5127x54Cxx-G
S		400 ms/Active Low	IXD5127x16Dxx-G – IXD5127x54Dxx-G
T		800 ms/Active Low	IXD5127x16Exx-G – IXD5127x54Exx-G
U		50 ms/Active High	IXD5127x16Fxx-G – IXD5127x54Fxx-G
V		100 ms/Active High	IXD5127x16Gxx-G – IXD5127x54Gxx-G
X		200 ms/Active High	IXD5127x16Hxx-G – IXD5127x54Hxx-G
Y		400 ms/Active High	IXD5127x16Jxx-G – IXD5127x54Jxx-G
Z		800 ms/Active High	IXD5127x16Kxx-G – IXD5127x54Kxx-G

④⑤ - Represents production lot number 01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ、B1～ZZ repeated.

(G, I, J, O, Q, W excluded.)

Customer Support

To share comments, get your technical questions answered, or report issues you may be experiencing with our products, please visit Zilog's Technical Support page at http://support.zilog.com. To learn more about this product, find additional documentation, or to discover other fac-ets about Zilog product offerings, please visit the Zilog Knowledge Base at http:// zilog.com/kb or consider participating in the Zilog Forum at http://zilog.com/forum. This publication is subject to replacement by a later edition. To determine whether a later edition exists, please visit the Zilog website at http://www.zilog.com.

Warning: DO NOT USE THIS PRODUCT IN LIFE SUPPORT SYSTEMS.

LIFE SUPPORT POLICY ZILOG'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF ZILOG CORPORATION.

As used herein Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.